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THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

7D20 PROGRAMMABLE DIGITIZER

WITH OPTIONS

SERVICE

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

070-3858-01
Product Group 42

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http://manoman.sqhill.com

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INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

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SEND TO: **TEKTRONIX, INC.**
LAB SCOPES SOFTWARE MAINTENANCE
P.O. BOX 500 DEL. STA. 39-285
BEAVERTON, OREGON 97077

7D20 PROGRAMMABLE DIGITIZER SOFTWARE/FIRMWARE PERFORMANCE REPORT

A

7D20 PROGRAMMABLE DIGITIZER SERIAL # _____

VERSION LINE OF 7D20 DISPLAY WHEN ID KEY IS PRESSED TEK/7D20 _____

B

COMPANY NAME: _____

USER: _____

ADDRESS: _____

CITY: _____ STATE: _____ ZIP: _____

PHONE: _____ EXTENSION: _____

FORM SUBMITTED BY: _____ DATE: _____

C

REASON FOR REPORT:

☐ Software/Firmware Error
☐ Documentation Error
☐ Suggested Enhancement

IS THE ERROR REPRODUCIBLE?

☐ Yes ☐ No
☐ Intermittent

D

SYSTEM DESCRIPTION: (Hardware, software, firmware and host related to the problem)

MAINFRAME _____ MAINFRAME SERIAL # _____

E

DESCRIPTION OF PROBLEM:

LIST ENCLOSURES:

INTERNAL USE ONLY
(DO NOT WRITE BELOW THIS LINE)

F

ACTION TAKEN:

RESPONDER: DATE OF RESPONSE:

DATE RECEIVED _____

SFPR # _____

SFPR LOG

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INSTRUCTIONS FOR COMPLETING THE SOFTWARE/FIRMWARE PERFORMANCE REPORT

I. Please type or print clearly. Use a separate Software/Firmware Performance Report (SFPR) for each problem.

II. SECTION (A)
Fill in the serial number of the 7D20 PROGRAMMABLE DIGITIZER. Press the ID key on the 7D20 and copy the entire line of Version information, beginning with TEK/7D20.

III. SECTION (B)
Use your complete company mailing address. Please include the name and phone number of the person reporting the error. Also, be sure to fill in the name of the person submitting the SFPR.

IV. SECTION (C)
Check the reason for report and whether the error is reproducible. We cannot properly evlauate the problem if we have difficulty in reproducing the error.

V. SECTION (D)
Give a complete description of the system configuration on which the problem occurred. Please include related peripherals, interfaces, options, and operating system.

VI. SECTION (E)
Describe the problem completely. Include any information which might help in evaluating the error with the SFPR. If you have determined a procedure to avoid the error condition, please include this procedure. If this problem prevents you from accomplishing any useful work with the product, please state this fact. Be sure to include with the SFPR any information (programs, listings, hard copies, etc.) which will help us duplicate your problem.

VII. SECTION (F)
This section is for use by Tektronix Lab Scopes Software Maintenance personnel. DO NOT WRITE IN THIS SPACE.

VIII. Mail **all** copies of the Software/Firmware Performance Report to:

TEKTRONIX, INC.
LAB SCOPES SOFTWARE MAINTENANCE
P.O. BOX 500 DEL. STA. 39-285
BEAVERTON, OREGON 97077

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RELATED DOCUMENTATION

The tabbed "ACCESSORIES" page at the rear of this manual lists the Tektronix part numbers for all Standard Accessories provided with this product.

Also, Section 1, General Information, contains a brief basic-content description for the following publications.

MANUALS (Standard Accessories)

7D20 Operators
7D20 Service

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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

IN THIS MANUAL

Static-Sensitive Devices

This symbol indicates where applicable cautionary or other information is to be found.

AS MARKING ON EQUIPMENT

DANGER—High voltage.

Protective ground (earth) terminal.

ATTENTION—refer to manual.

WARNINGS

POWER SOURCE

This product is intended to operate in a mainframe connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

GROUNDING THE PRODUCT

This product is grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, plug the mainframe power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective-ground connection by way of the grounding conductor in the mainframe power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating), can render an electric shock.

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DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an atmosphere of explosive gasses.

DO NOT REMOVE COVERS OR PANELS

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

DO NOT OPERATE WITHOUT COVERS

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

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SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

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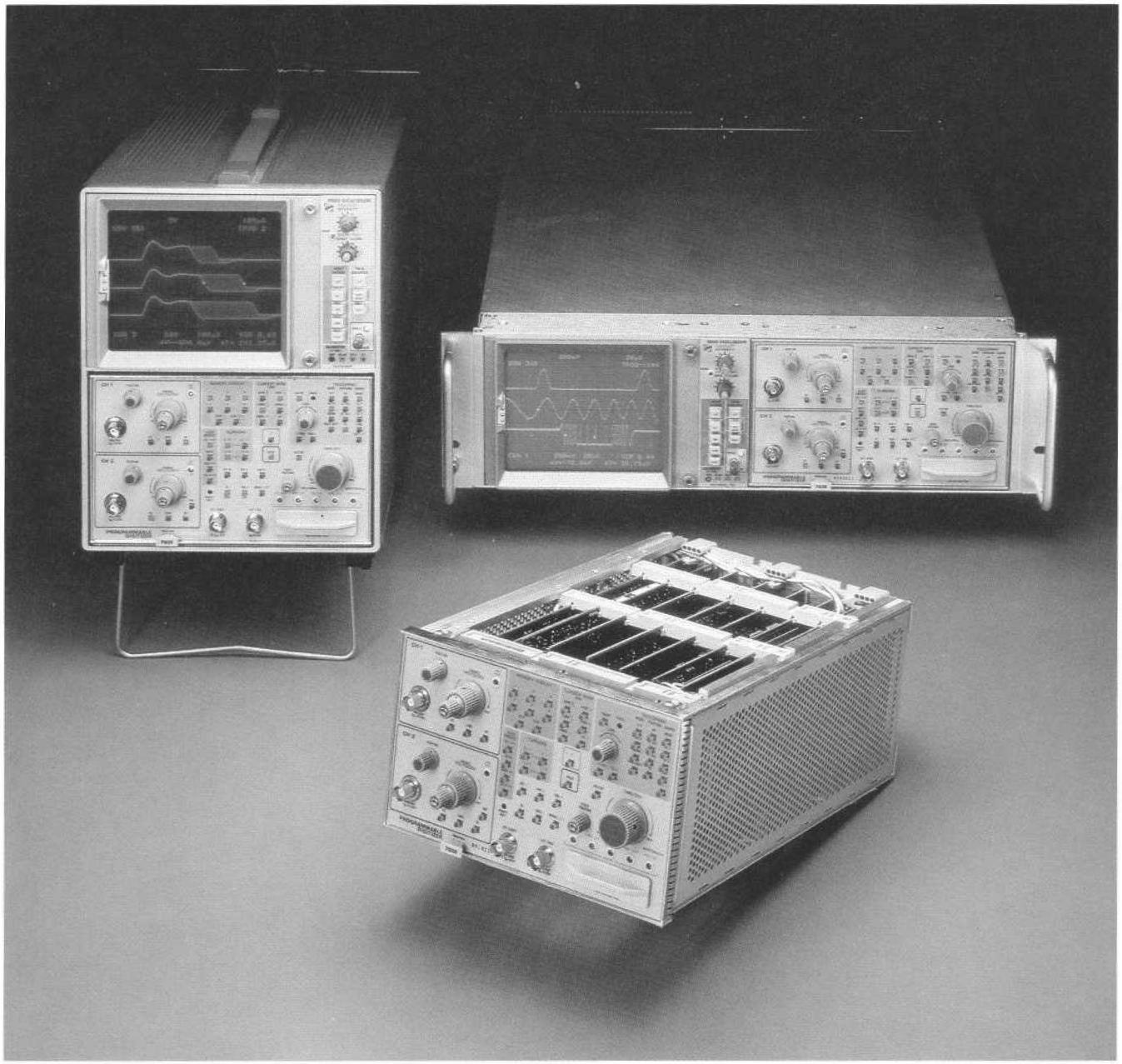

7D20 FEATURES

The 7D20 Programmable Digitizer is designed to enhance the capabilities of 7000-series oscilloscope mainframes. Multiple waveform storage, crt readout, two cursors for point-to-point measurements, pre- and post-trigger viewing, store and recall of up to six front-panel settings, and signal averaging to reduce noise are just a few of the features this three-wide plug-in unit provides.

Waveform storage using digital memory eliminates the need for a storage crt, and allows viewing information that occurred prior to a triggering event. Six waveforms can be stored and displayed at the same time for easy comparison.

A complete alphanumerical display of cursor waveform information and measurement values, time base and amplitude settings, trigger position, displayed waveform number, prompts and error messages, and a master menu that allows you to choose seldom used features easily and quickly.

The master menu offers a convenient way to enable special functions such as the STORE and RECALL of front-panel settings as well as allowing you to branch-out to other menus. The test menu is designed to assist in troubleshooting the 7D20 in the event of a failure. The SELF TEST may be implemented at any time to ensure user confidence. The other selections allow service personnel to diagnose faults to the component level.

Complete control of the 7D20's functions may be controlled via the IEEE-488 interface. Commands, waveforms, and alphanumeric text messages may be sent or received via the front-panel port.

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GENERAL INFORMATION

This section is the first place to look for information concerning your 7D20 Programmable Digitizer. Here we describe the basic content of the operators and service manuals which are standard accessories to your new instrument. We also include a brief general description of the 7D20 and explain how to install it in a host mainframe for operation. In this section we give the electrical, environmental, and physical characteristics and specifications of the 7D20, list the standard and recommended accessories, and provide a dimensional drawing of the instrument. Should you have need to repackage the instrument for shipment, that information is also included.

TECHNICAL MANUALS

Both an operators and a service manual are supplied with your 7D20 as standard accessories. The following information outlines the content of these manuals.

Operators Manual

The operators manual for the 7D20 contains six sections of information to explain the operation of your instrument. The content of the operators manual is described below:

SECTION 1—GENERAL INFORMATION contains an instrument description along with information for installing the 7D20 into a host mainframe. We make a special note regarding rackmounting and another about compatibility considerations. This section also provides a complete list of the 7D20 electrical, environmental, and physical specifications and characteristics. It also lists standard and recommended accessories, and gives instructions for packaging the instrument for shipment.

SECTION 2—OPERATING INSTRUCTIONS provides a general overview of the instruments capabilities, controls and connector information, a series of get acquainted exercises, and detailed operating information.

SECTION 3—OPERATIONAL THEORY provides additional information about the operation of the 7D20 digitizer. This section discusses the more technical aspects of the digitizing techniques used by the 7D20 and gives the algorithms used for waveform averaging and enveloping.

SECTION 4—GPIB contains a general description of the GPIB interface, address selection information, description of the instrument status following power-up, and descriptions of the commands and messages which can be transferred over the GPIB. The section also provides a command language index.

SECTION 5—APPLICATIONS illustrates how your 7D20 can be used in a variety of situations. In this section we combine the 7D20 with other Tektronix products for some unique and interesting digital storage application possibilities.

SECTION 6—INSTRUMENT OPTIONS contains descriptions of available options.

Service Manual

Your service manual contains eight sections of information pertaining to the servicing needs of your 7D20. The following is a brief overview of this manual's contents.

WARNING

The following service instructions are for use by qualified personnel only. To avoid personal injury, do not perform any service other than that contained in operating instructions unless you are qualified to do so. Refer to Operators Safety Summary and Service Safety Summary prior to performing any service.

SECTION 1—GENERAL INFORMATION contains an instrument description along with information for installing the 7D20 into a host mainframe. We make a special note regarding rackmounting and another about compatibility considerations. This section also provides a complete list of the 7D20 electrical, environmental, and physical specifications and characteristics. It also lists standard and recommended accessories, and gives instructions for packaging the instrument for shipment.

SECTION 2—THEORY OF OPERATION provides a basic block diagram description of the 7D20 along with general and specific circuit analysis that may be useful for servicing the instrument.

SECTION 3—MAINTENANCE describes routine and corrective maintenance procedures with detailed instructions for replacing assemblies, subassemblies, and individual parts. Included in this section are full instructions for troubleshooting the 7D20 using internal diagnostic routines and signature analysis.

SECTION 4—CHECKS AND ADJUSTMENTS is divided into three separate parts: Part I—Functional Check Procedure used to verify that the major functions of the instrument perform properly. Part II—Performance

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Check Procedure used to verify that this instrument meets the applicable electrical specifications in Section 1. Part III—Adjustment Procedure provides an adjustment procedure to ensure that this instrument is performing at peak capabilities and meets or exceeds the listed electrical specifications at the time of adjustment under the specified conditions. These three parts provide for verification of the qualitative integrity of the product, its performance relating to specifications in Section 1, and the optimization of its performance respectively.

SECTION 5—INSTRUMENT OPTIONS contains descriptions of available options and provides a table for locating any option information found elsewhere within the manual.

SECTION 6—REPLACEABLE ELECTRICAL PARTS provides the information necessary to order replaceable parts and assemblies.

SECTION 7—DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS includes detailed circuit schematics, locations of assembled boards within the instrument, voltage and waveform information and circuit board component locators. Signature analysis troubleshooting charts and tables also are included within this section.

SECTION 8—REPLACEABLE MECHANICAL PARTS provides information necessary for ordering mechanical parts and includes exploded-view drawings which identify individual parts and assemblies within the 7D20.

INSTALLATION

The 7D20 is a three-compartment wide, Tektronix 7000-series plug-in unit. To install the 7D20 in a host mainframe, align the grooves in the top and bottom of the instrument with the guides at the top and bottom of the plug-in compartment of the mainframe. Then, push the 7D20 in until its front panel is flush with the front panel of the host mainframe. In four-compartment mainframes, the preferred position for installation is in the three right hand compartments. This leaves the left vertical compartment available for other 7000-series plug-in units.

Installation in any mainframe requires that the 7D20 display output be adjusted to compensate for the calibration tolerances of the host mainframe. The procedure for doing this is given in the section 2 of the Operators Manual.

NOTE

Switch off the mainframe power before removing or installing the 7D20.

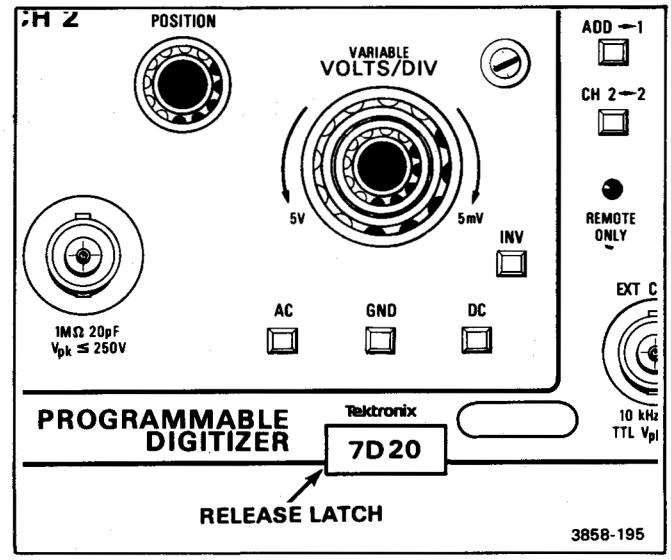

Figure 1-1. 7D20 Release Latch.

To remove the 7D20 from its host mainframe, pull the release latch (see Fig. 1-1) to disengage it from the mainframe. Pull straight out to remove the 7D20 from the plug-in compartment.

RACKMOUNT MAINFRAMES

A special option (Option 20) is available for TEKTRONIX R7603 Oscilloscope (rackmount) mainframes that enable you to make GPIB connections at the rear of the mainframe. The option includes a special cable which must be installed in the 7D20 for this purpose. This cable is also available separately and can be ordered as an optional accessory.

COMPATIBILITY

The 7D20 is compatible with all Tektronix 7000-series mainframes except the 7104. Because of the small area and fixed pattern of the 7D20 readout, the display from the 7D20 can cause permanent reduction in the crt microchannel plate gain, permanently reducing the writing rate of the 7104. Any crt damage caused by use of the 7D20 in the 7104 will not be covered under the instrument warranty.

PACKAGING FOR SHIPMENT

If this instrument is to be shipped for long distances by commercial transportation, we recommend that it be packaged in the original manner. The carton and packaging material in which your instrument was shipped should be saved and used for this purpose.

Also, if this instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag to the instrument showing the following: Owner of the instrument (with address), the name of the person at your firm who can be contacted, complete instrument type and serial number, and a description of the service

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required. Include any self test failure information you have available.

If the original packaging is unfit for use or not available, package the instrument as follows:

1. Obtain a corrugated cardboard shipping carton with a 200-pound test strength and having inside dimensions at least six inches greater than the instrument dimensions. This allows for cushioning.
2. Wrap the instrument with polyethylene sheeting or equivalent material to protect the finish of the instrument.
3. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between the carton and the instrument, allowing three inches on each side.
4. Seal the carton with shipping tape or with an industrial stapler.
5. Mark the address of the Tektronix Service Center and your return address on the carton in one or more prominent locations.

SPECIFICATIONS

The electrical characteristics listed in Table 1-1 apply when the following conditions are met: (1) Adjustment of the instrument must have taken place at an ambient temperature between +20° and +30° C, (2) the instrument and its host mainframe must be allowed a 20-minute warm-up period, (3) all specifications are valid at an ambient temperature of 0° to +45° C, unless otherwise stated, (4) the instrument must be in an environment that meets the limits described in Table 1-2.

Any applicable conditions not listed above are expressly stated as part of that characteristic. Environmental characteristics are listed in Table 1-2 and Physical characteristics are listed in Table 1-3.

TABLE 1-1
Electrical Characteristics

Characteristic	Performance Requirement
VERTICAL	
Deflection Factor (Volts/Div)	
Calibration Range	5 mV/Div to 5 V/Div in 1,2,5 sequence.
Gain Ratio Accuracy	Within 2% with AQR GAIN adjusted at 10 mV/Div.
Uncalibrated (Variable)	Continuously variable; VARIABLE extends deflection factor to at least 12.5 VOLTS/DIV
Vertical Linearity (1 kHz square wave)	0.12 Div or less expansion or compression of a center screen 2 Div signal positioned anywhere within the ±4 division graticule area.
Invert Deflection Factor Ratio	1:1 within 1%.
Common Mode Rejection Ratio (using ADD, INVERT)	At least 10:1, dc to 25 MHz.
Bandwidth (1 μs to 50 ns/div)	Dc to 70 MHz.
AC Coupled Low-Frequency Bandwidth	10 Hz or less.
Risetime (ETD)	5 ns or less (6 div signal centered on screen).
Overdrive Recovery	1 ms or less to recover within 1 div with the VOLTS/DIV set at 5 mV and an overdrive signal of ±1.5 V.

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TABLE 1-1 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement
Maximum Input Voltage	
DC Coupled (DC+Peak AC)	250 V, 1 kHz or less.
AC Coupled (DC+Peak AC)	400 V, 1 kHz or less.
Input R and C	
Resistance	1 MΩ ±1%.
Capacitance	Approximately 20 pF.
Signal Isolation between Channels (8 Div Ref)	100:1 up to 20 MHz.
Noise (Full scale = 10.24 Divisions)	Mean value of 50 measurements taken at 0.02 Division increments.
10 mV/Div to 5 V/Div	55 dB Full Scale/RMS Noise.
5 mV/Div	52 dB Full Scale/RMS Noise.
Phase Match Between Channels	2 Degrees at 10 MHz.

TRIGGER

Sensitivity	Triggering Frequency Range	Minimum Vertical Signal Required		
		Internal	Ext.	Ext÷10
AC Coupled	30 Hz—30 MHz 30 MHz—70 MHz	0.4 Div 1.0 Div	60 mV 150 mV	0.6 V 1.5 V
AC LF REJ	50 kHz—30 MHz 30 MHz—70 MHz	0.4 Div 1.0 Div	60 mV 150 mV	0.6 V 1.5 V
AC HF REJ	30 Hz—30 kHz	0.4 Div	60 mV	0.6 V
DC HF REJ	DC—30 kHz	0.4 Div	60 mV	0.6 V
DC	DC—30 MHz 30 MHz—70 MHz	0.4 Div 1.0 Div	60 mV 150 mV	0.6 V 1.5 V
Max Signal		±6 Div	±1.0 V	±10 V
P-P	30 Hz—200 Hz 200 Hz—30 MHz 30 MHz—70 MHz	2.0 Div 0.6 Div 1.2 Div	300 mV 90 mV 200 mV	3.0 V 0.9 V 2.0 V
Programmed Trigger Levels				
Resolution		0.05 Div.	7.8 mV	78 mV
Nominal Range		+6.35 Div. -6.4 Div.	+0.992 V -1.000 V	+9.92 V 10.00 V

Accuracy	
Internal	±(5% of programmed level +0.25 Div.)
External	±(8% of programmed level x 156 mV +100 mV)
External÷10	±(12% of programmed level x 1560 mV +1000 mV)

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TABLE 1-1 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement
Ext Trigger Input	
Resistance	1 MΩ, ±10%.
Capacitance	Approximately 20 pF.
Maximum Input Voltage (DC + Peak AC)	250 V (1 kHz or less).

DIGITIZER

Acquisition Window	Nominally ±5 Div from center graticule line.		
Resolution			
Vertical	Nominally 0.04 Div.		
Horizontal	TIME/DIV	Points/Waveform	Resolution
	EXT, 20s—500μs	1024	0.01 Div.
	200μs—2μs	820	0.0125 Div.
	1μs—50 ns	1024	0.01 Div.
Stored Timing Accuracy			
1 Cursor	±0.1% of reading +0, −1 sample interval ±300 ps.		
2 Cursors	±0.1% of reading ±600 ps.		
Digitizer Maximum Sample Rate	40 megasamples/second.		
Digitizing Modes			
Equivalent Time	1 μs/div through 50 ns/div.		
Extended Real-Time	200 μs/div to 2 μs/div.		
Real-Time	50 ms/div to 500 μs/div.		
Roll	20 s/div to 100 ms/div and EXTernal CLOCK.		
External Clock			
Input Frequency (MAX)	≤10 kHz.		
TTL	≤5 Vpk.		

GPIB INTERFACE

Functions Implemented (As Per IEEE 488-1978)	Description:
SH1	Complete Source Handshake.
AH1	Complete Acceptor Handshake.
T5	Talk Function Complete (no secondary addressing).
L3	Listen Function Complete (no secondary addressing).
SR1	Complete Service Request Capability.
RL1	Complete Remote/Local Capability.
PP0	No Parallel Poll Capability.
DC1	Complete Device Clear Capability.
DT1	Complete Device Trigger Capability.
C0	No Controller Capability.

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TABLE 1-2
Environmental Characteristics

Characteristics	Information
Temperature (External Ambient Mainframe Temperature)	
Operating	0 to +40°C in 7403N/7603 without fan (fan kit is available). 0 to +45°C in other 7000-series mainframes.
Storage	−55° C to +75° C.
Altitude	
Operating	15,000 feet (4.6 Km).
Nonoperating	To 50,000 feet (15.2 Km).
Vibration	
Operating	Tested to MIL-T-28800C SECT. 4.5.5.3.1 Type 2, Class 5, Style E&F.
Shock	Tested to MIL-T-28800C SECT. 4.5.5.4.1 Type 2, Class 5, Style E&F.
Bench Handling	Tested to MIL-T-28800C SECT. 4.5.5.4.3 Type 2, Class 5, Style E&F.
Transportation	National Safe Transit Association, Preshipment Test Procedure.
Vibration and Bounce (packaged product)	NSTA, PROJECT 1 A-B-1.
Drop (packaged product)	NSTA, PROJECT 1 A-B-2.

TABLE 1-3
Physical Characteristics

Characteristics	Information
Net Weight	Approximately 8.5 lb, 3.9 Kg.
Dimensions	See Figure 1-2.

STANDARD ACCESSORIES

1 ea..... Operators Manual
1 ea.....Service Manual

For more detailed information, refer to the tabbed Accessories page at the rear of this manual.

OPTIONAL ACCESSORIES (not included)

The following accessories are available for use with the 7D20. Refer to the tabbed Accessories page at the rear of this manual for more detailed information.

1 ea..... Circuit-Board Extender
3 ea..... 7000-series Plug-In Flexible Extenders
1 ea.....Internal GPIB Cable for use with R7603 Option 20

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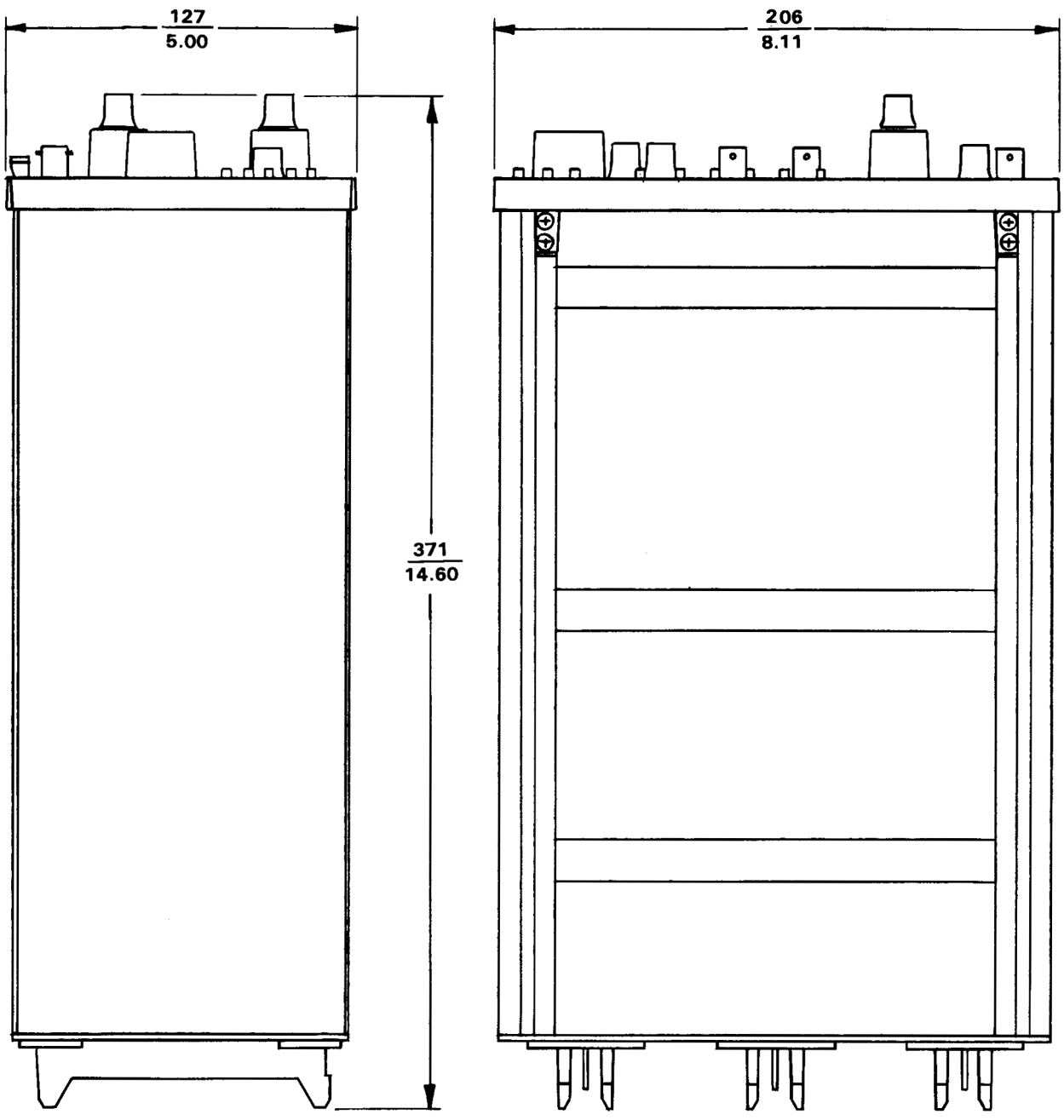

Figure 1-2. Dimensional Drawing.

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THEORY OF OPERATION

This section of the manual describes the circuitry in the 7D20 Programmable Digitizer plug-in. It is divided into two parts: Block Diagram Description and Detailed Circuit Operation. Detailed schematic diagrams are given in Section 7, of this manual.

BLOCK DIAGRAM DESCRIPTION

The following description presents an overview of the operation of the 7D20. Figure 2-1 is an overall block diagram of the plug-in. The numbers enclosed in diamonds within each block in Figure 2-1 indicate the schematic diagrams associated with the block. Some blocks also include the figure number of a detailed block diagram of the block in the detailed circuit descrption. A discussion of the operation of the charge coupled devices (CCDs) and the Time Base modes is included at the end of the block diagram description. This background information will help in understanding the detailed description of circuit operation.

OVERALL BLOCK DIAGRAM DESCRIPTION

The 7D20 Programmable Digitizer is essentially an analog to digital to analog converter (see Fig. 2-1). Input signals are applied to the Preamplifier circuitry through the CH 1 or CH 2 input connector, or both. The Preamplifier circuitry attenuates the input signal according to the setting of the front-panel VOLTS/DIV switch. It then amplifies the signal, converts it into a differential signal and applies it to the CCD circuitry.

The Charge Coupled Device (CCD) circuitry takes analog samples of the input signal, which are then converted into digital values. (See the following discussion of the operation of the CCDs.) The CCD circuitry receives its timing and synchronization information from the Time Base circuitry. The digitized samples are applied to the Memory circuitry.

The Memory circuitry contains the waveform memory (WFM), control and synchronization circuitry. The WFM is used to store acquired waveform data from the CCD circuitry A-to-D converter, and is also a source of data for display on the mainframe crt. In addition, the microprocessor takes data from the WFM to perform operations such as waveform averaging, GPIB data transfer, cursor measurements and storage of data for readout displays.

The Display circuitry receives digital display data from the WFM and converts it to analog display signals, which drive the mainframe vertical and horizontal display amplifiers to produce the mainframe crt display. The Display circuitry produces four types of displays: Y vs. time, X-Y, readout and cursor. Display setup information from the microprocessor determines the display mode. Timing signals from the Time Base circuitry synchronize the Display with the Memory access time slots.

The Display circuitry also allows waveforms displayed in the Y vs. time mode to be expanded, compressed, offset and magnified horizontally without modifying the contents of the WFM.

The Trigger circuitry generates the trigger gate signals (TGE and $\overline{\text{TGE}}$), which provide a trigger reference point to the Time Base circuitry for the acquired data. It can produce a trigger gate from four different trigger signal sources: Ch 1 input signal, Ch 2 input signal, line trigger and external trigger signal. The trigger source, coupling, mode, level and slope can be selected from the front panel or externally programmed. The Trigger board (A10) also contains the horizontal display signal output amplifier, a blanking signal amplifier and the sweep gate circuit.

The Time Base circuitry provides the basic timing for the 7D20. It generates a number of clock and control signals, which are used within the Time Base, CCD, Memory and Display circuitry to control the timing of waveform acquisition and display. These signals control the rate at which the CCDs sample the signal, and which of these samples are subsequently stored in the waveform memory (WFM). The Time Base circuitry receives setup and control information from the microprocessor, and in turn transmits trigger and timing data back to the microprocessor for use in setting up and controlling the Memory and Display circuitry. (See the discussion of the four Time Base modes at the end of this block diagram description.)

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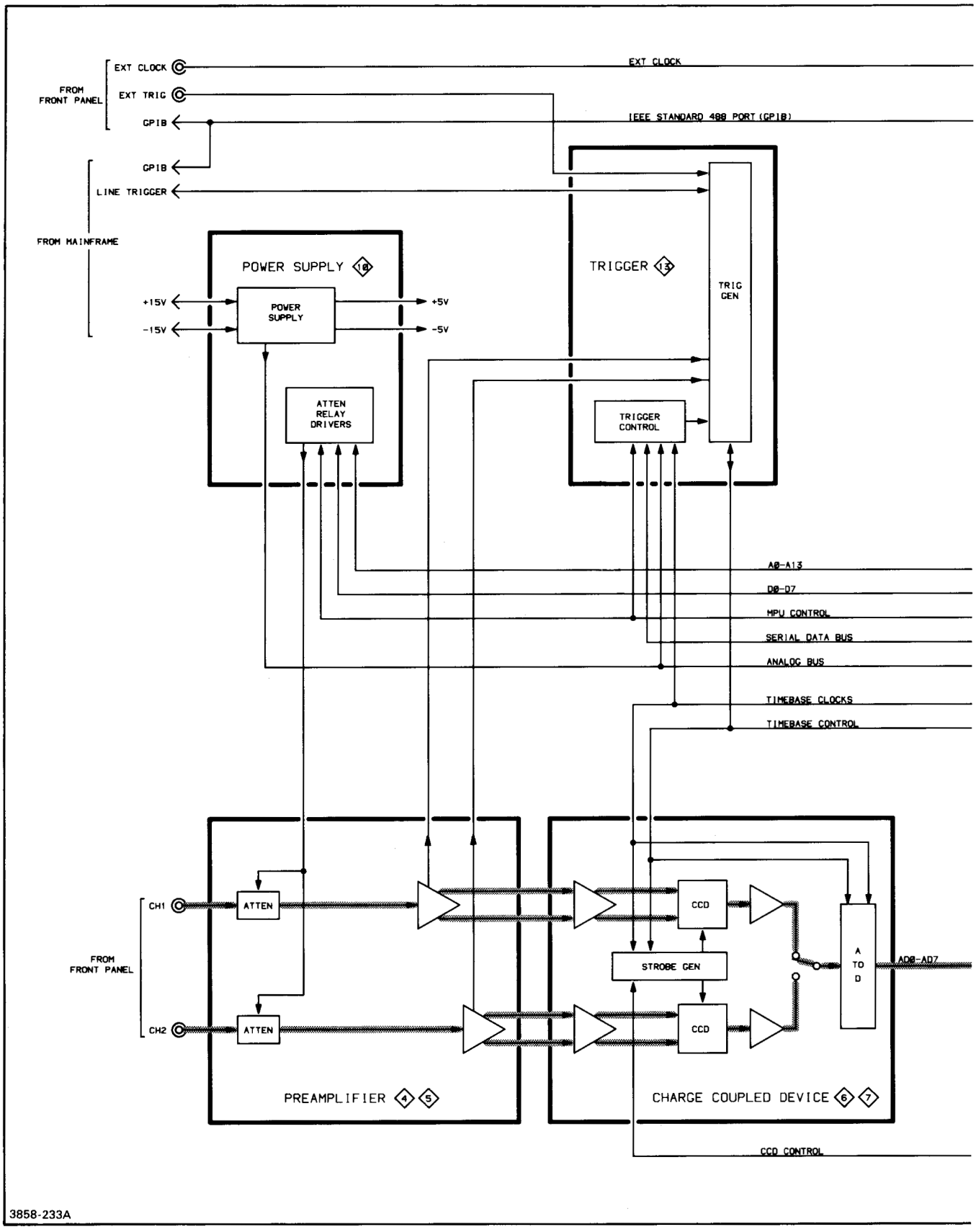

Figure 2-1. 7D20 Overall block diagram.

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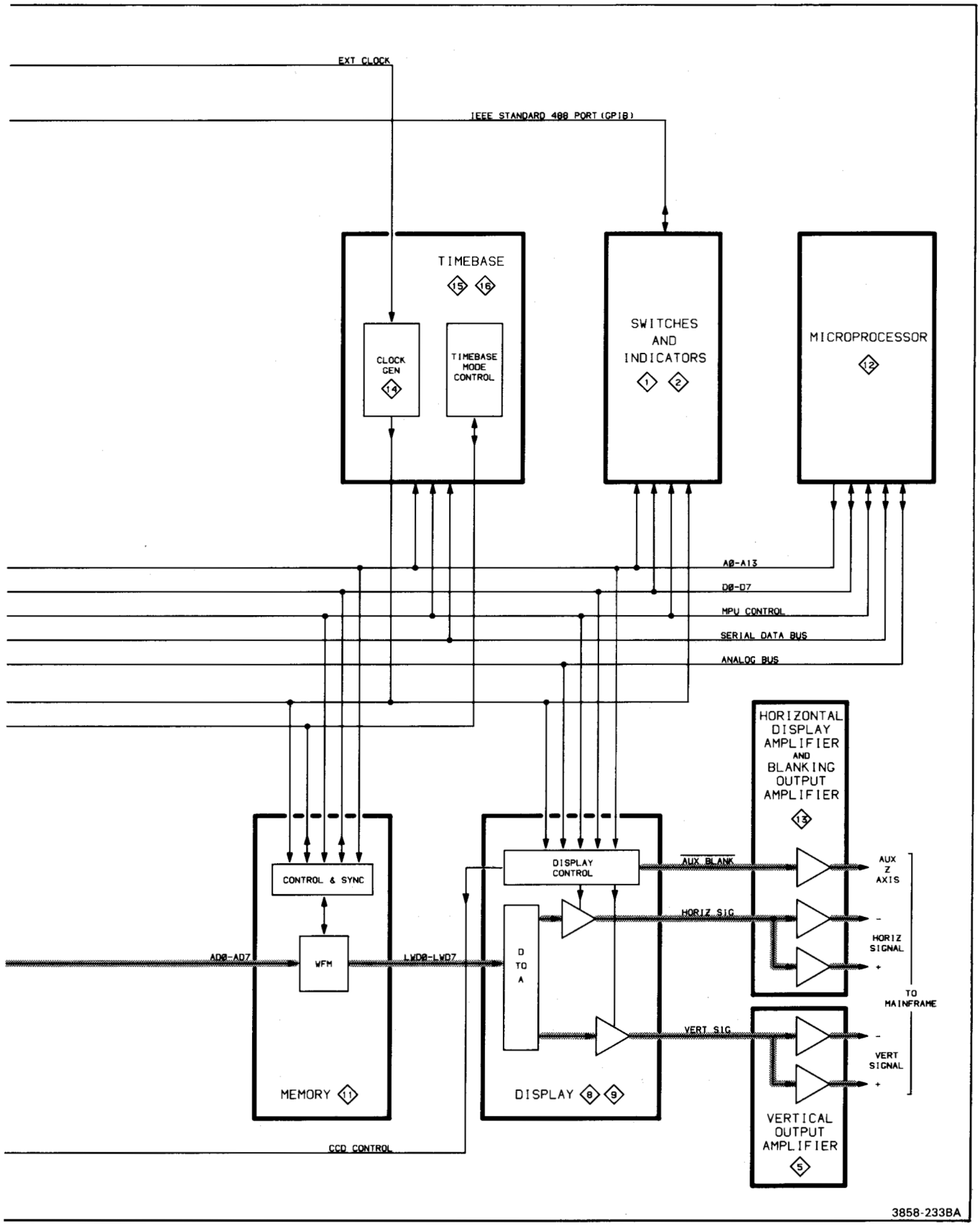

Figure 2-1 (cont). 7D20 Overall block diagram.

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The Microprocessor circuitry controls the setup of the 7D20 for its various modes of operation, and initiates the acquisition and display of waveforms. It also performs calculations such as signal averaging and delta-time measurements, and controls the self diagnostics and GPIB interface firmware.

The Microprocessor circuitry produces and receives five major groups of signals: address lines (A0-A13), data lines (D0-D7), control lines, serial data lines and analog bus lines. The control lines include the read/write controls lines, hardware selects and interrupts. The serial data lines include the serial data bus and its accompanying control signals. The analog bus includes two lines for receiving analog information from the various circuits in the 7D20 for use in self test and Probe Coding detection.

The Power Supply converts the +15 V and −15 V mainframe power supplies to +5 V and −5 V power supplies to power the 7D20 logic and analog circuitry. In addition, the Power Supply board (A7) houses drivers for the relays on the Ch 1 and Ch 2 Attenuator boards (A12 and A13).

CHARGE COUPLED DEVICE (CCD) OPERATION

A charge coupled device (CCD) is an analog shift register. Each CCD used in the 7D20 contains two analog shift registers (see Fig. 2-2) that are driven in parallel: Channel A samples the minus side of the differential input signal; Channel B samples the plus side of the signal.

On each sampling clock to a channel, a sample is taken of the signal. This sample is then stored in the first cell of the analog shift register. On subsequent clocks, this sample is passed from cell to cell, until it is applied to the output amplifier and subsequently to an analog-to-digital (A-to-D) converter.

The CCD circuitry is operated in two modes: simultaneous differential sampling and alternate differential sampling. In the roll, real-time digitizing (RD) and equivalent time digitizing (ETD) time base modes (see the following discussion of the Time Base modes), the two channels of the CCD are clocked at the same rate and phase. The two channels of the CCD thus simultaneously sample the plus and minus sides of the differential preamplifier output signal.

In the extended real-time digitizing (ERD) mode, the clock signal to channel B is shifted one-half clock cycle with respect to the clock signal to channel A. The two CCD channels thus take alternate samples of the preamplifier output signal, one sample being taken every half clock cycle. This technique permits the real-time sampling bandwidth of the 7D20 to be extended in the ERD mode.

TIME BASE MODES

The Time Base circuitry has four basic modes of operation: roll, real-time digitizing (RD), extended real-time digitizing (ERD) and equivalent time digitizing (ETD). The setting of the TIME/DIV switch determines the mode of operation of the Time Base. In the roll, real-time

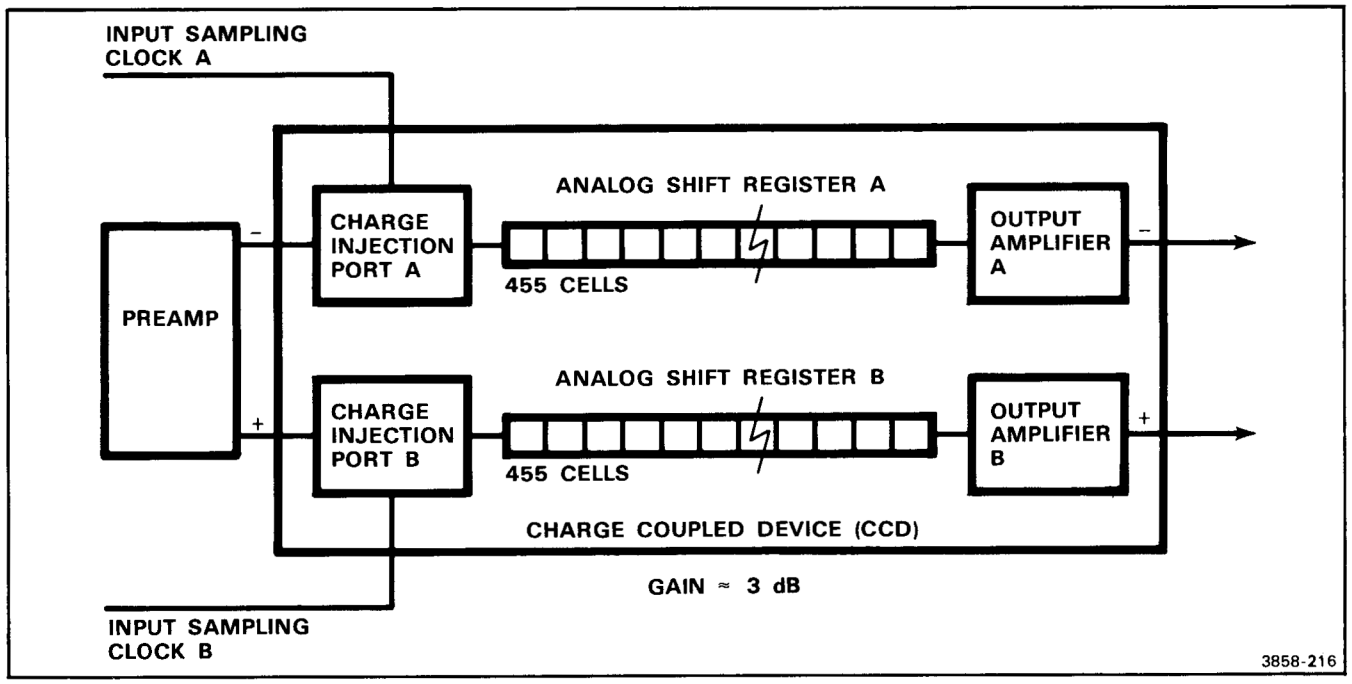

Figure 2-2. Simplified block diagram of Charge Coupled Device (CCD).

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TABLE 2-1
Summary of Time Base Modes

Time Base Mode	Time/Div Range	Fast In-Slow-Out	Real Time	Samples Acquired/Div/ Acquisition Cycle	Samples Displayed/Div
Roll	EXT CLK 20 s to 100 ms	No	Yes	100	100
Real-Time Digitizing	50 ms to 500 μs	No	Yes	100	100
Extended Real-Time Digitizing	200 μs to 2 μs	Yes	Yes	80	80
Equivalent Time Digitizing	1 μs 500 ns 200 ns 100 ns 50 ns	Yes	No	20 10 4 2 1	100

digitizing, and extended real-time digitizing modes, an entire waveform is captured during one acquisition cycle; in the equivalent time digitizing mode, a composite waveform is built up from samples taken during a number of acquisition cycles in a manner similar to that used in conventional sampling plug-ins. Table 2-1 summarizes the features of these four Time Base Modes.

The roll mode (see Fig. 2-3A) creates a display on the mainframe crt similar to that of a strip chart recorder. In this mode, the CCD circuitry continuously samples the input signal at a 400 kHz rate. Selected samples are then stored in a 1K block of the WFM at a rate determined by the sample counter. For example, at a time/division setting of 0.1 s/division, samples are stored in the WFM at a rate of 1 kHz:

$$\frac{0.1\text{ s}}{1\text{ Division}} \times \frac{1\text{ Division}}{100\text{ Samples}} = \frac{1\text{ s}}{1000\text{ Samples}} \quad \text{or 1 kHz}$$

Thus, every 400th sample that the CCD takes is stored in the WFM.

When the 1023rd memory location is filled, the Memory circuitry wraps around to location 0, such that the WFM is treated as an infinitely long register. The Display circuitry scans the WFM continuously, changing the start point in the WFM for each new display cycle. The crt display is continuously updated with the 1024 most recently acquired samples, thus producing a strip-chart effect.

In the roll mode, a trigger is not required when the front-panel TRIGGERING MODE is set for P-P, AUTO or NORM, since the WFM is continuously being filled with new waveform information, which is in turn being displayed on the crt. In the HOLD NEXT mode, however, waveform acquisition can be halted a selected number of samples following a trigger event. The acquired waveform is then held in the WFM (see the following discussion of the post-trigger count).

In the real-time digitizing (RD) mode (see Fig. 2-3B), the CCD also continuously samples the input signal at a 400 kHz rate, and stores selected samples of the signal in a 1K block of the WFM, again at a rate determined by the sample counter. When a trigger occurs, the storage of waveform samples continues until a preset post-trigger count is reached, at which time signal acquisition is halted. Compensation for the 455-sample delay through the CCD is included in the post-trigger count. The amount of post-trigger selected determines which portion of the signal is stored in the WFM with respect to the trigger event. Once the waveform has been stored in the WFM, the time base is reset and another waveform is acquired. This waveform, however, is stored in a second 1K block of WFM. While the second waveform is being acquired, the first waveform is displayed on the crt. This process is repeated continuously, switching back and forth between the two 1K blocks of WFM, such that the most recently acquired portion of the signal is always displayed.

In the extended real-time digitizing (ERD) mode (see Fig. 2-4A), a selected portion of the signal is first captured in the CCD, then written into the WFM. In this case, the two CCD channels continuously sample the input signal at a rate determined by the time/division setting. When the trigger event occurs, the CCD continues to sample the signal for a preset number of post-trigger counts, at which point sampling is halted. The samples held in the CCD are then written into a 1K block of WFM at a 400 kHz rate. Once the waveform is stored in WFM, the time base is reset and another waveform is acquired. As with the RD mode, the second waveform is written into another 1K block of the WFM, and the Display circuitry displays the most recently acquired waveform.

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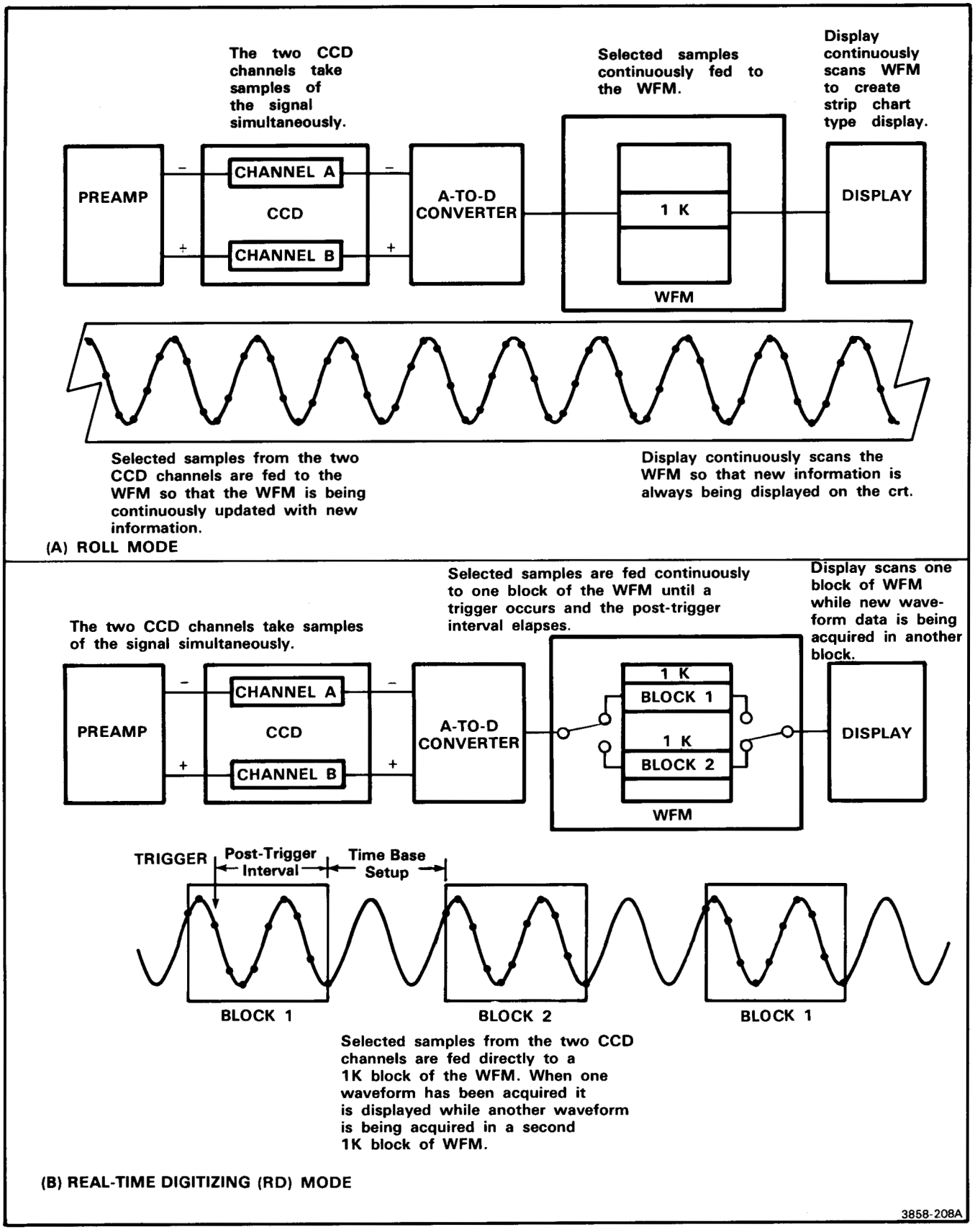

Figure 2-3. Non-Fast In, Slow-Out Time Base Modes: (A) Roll Mode; (B) Real-Time Digitizing (RD) Mode.

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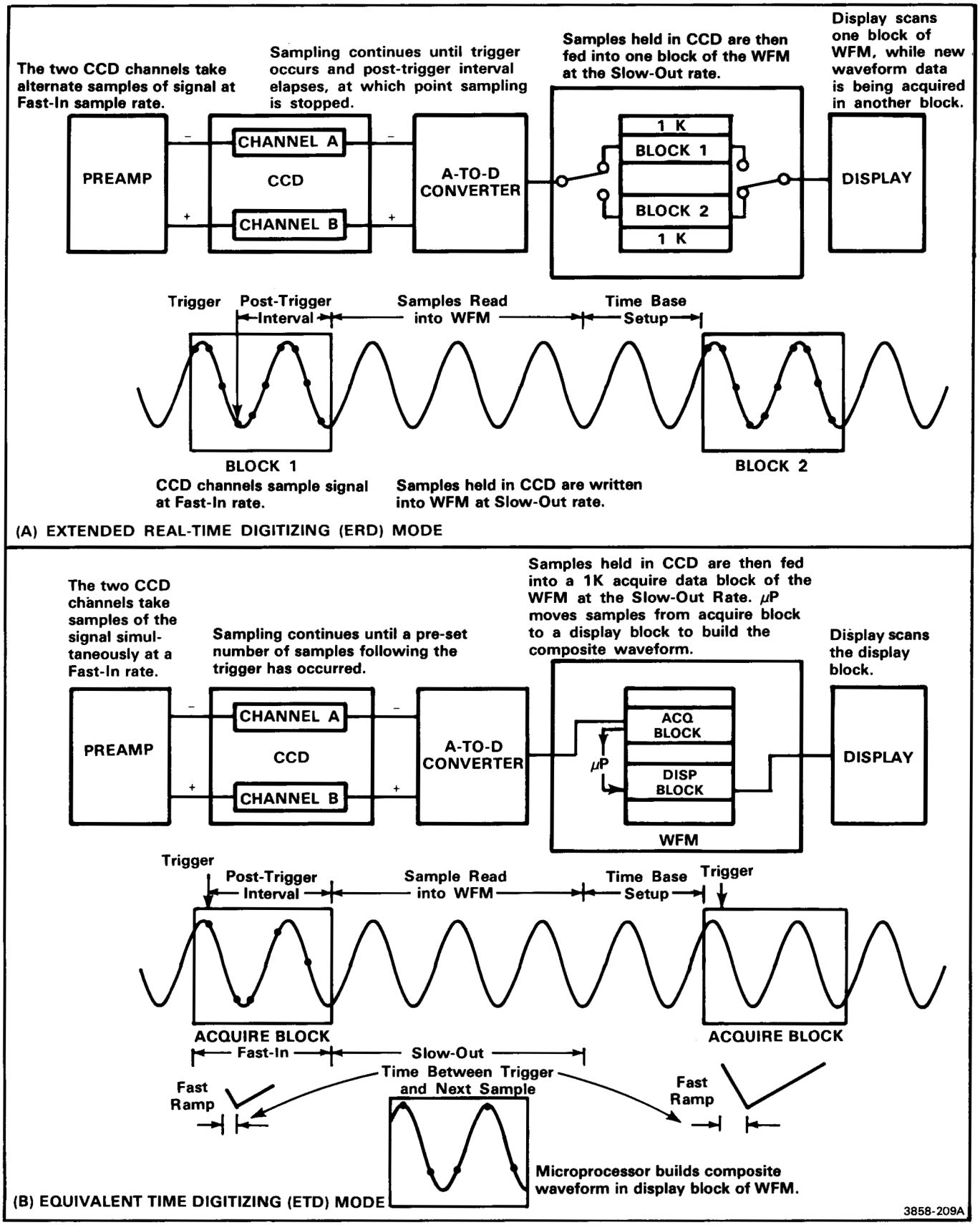

Figure 2-4. Fast-In, Slow-Out Time Base Modes: (A) Extended Real-Time Digitizing (ERD) Mode; (B) Equivalent Time Digitizing (ETD) Mode.

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As the time/division settings are increased in the ERD mode, the CCD samples the signal at a much faster rate than the acquired waveform is written into memory. This mode of signal acquisition is thus called fast-in, slow-out.

Also, the two CCD channels sample the signal in a slightly different manner in the ERD mode. In the roll, RD and equivalent time digitizing modes, the two CCD channels take a sample of the signal simultaneously on the leading edge of the phase clock. In the ERD mode, the two CCD channels take alternate samples of the signal, channel A taking a sample on the leading edge of the phase clock and channel B a sample on the trailing edge. This technique is used to increase the real-time signal acquisition capability of the 7D20. Since the portion of the waveform that can be captured in this mode is dependent on the combined length of the two channels of the CCD (910 samples), the time resolution in this mode is reduced from 100 samples per division to 80 samples per division.

In the equivalent time digitizing (ETD) mode (see Fig. 2-4B), a composite waveform is built up in a 1K block of the WFM from a number of waveform acquisition cycles. As with the ERD mode, the CCD samples the signal at a fast rate, then writes the samples held in the CCD into WFM at a slower rate. In the ETD mode, however, only a limited number of samples are taken during each acquisition cycle (see Table 2-2). On subsequent acquisiion cycles, more samples are taken until an accurate composite representation of the waveform is built up in the WFM.

TABLE 2-2
Sample Acquisition in the ETD Mode

TIME/DIV	No. Points Added to Display/ Acquisition Cycle
1 μs	204 or 205
500 ns	102 or 103
200 ns	40 or 41
100 ns	20 or 21
50 ns	10 or 11

In order to determine where to store the samples in the WFM with respect to samples taken during other acquisition cycles, the Time Base measures the time interval between the trigger event and the next sample taken with the fast ramp time interpolator. The phase clock and the signal being measured are asynchronous, so a complete representation of the signal is built up after a number of acquisition cycles.

Since a number of acquisition cycles are required to create a waveform in the ETD mode, it is only usable when measuring repetitive signals.

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TABLE 2-3
Signal Name Dictionary

SIGNAL NAME	DESCRIPTION	LOCATED ON DIAGRAM*
A0-A13	Address Bus—Microprocessor address bus; distributed generally throughout the 7D20.	1,2,3,8,10,11,15
AAGSS	Acquire Address Generator Single Step—Increments the acquire address generator by one count.	11
AAGSSEE	Acquire Address Generator Single Step Enable—Enables the single step fuction of the acquire address generator.	11
AA0-AA9	Acquire Address Bus—Generated by acquire address generator; indictes where in the WFM that acquired data is to be stored.	11
ABUS1 and ABUS2	Analog Buses—Two analog buses that carry analog test and diagnostic information from various circuits in the 7D20 to the MPU board.	3,5,7,9,10,13
ABCCDE	Analog Bus CCD Enable—Enables CCD test signal multiplexer on the CCD board.	3,7,8
ABDISPA, ABDISPB and ABDISPC	Analog Bus Display—Selects which signals from the display board are to be applied to the Analog Bus.	8,9
ABDISPE	Analog Bus Display Enable—Enables the analog bus multiplexer on the Display board.	8,9
ACQ	Acquire—Causes the display/acquire address multiplexer to select acquire addresses when the line is high and display addresses when the line is low.	11
AD0-AD7	A-to-D Data—Digitized sample data from the CCD circuitry A-to-D converter.	3,7,11
ADD	Add—Causes the CH 1 and CH 2 signals to be added together at the input to the CCD output amplifier.	3,8,11
ASA	Acquire Start Address—Causes starting acquire address to be loaded into the acquire address generator.	11
AW	Acquire Write—Indicates to the Memory circuitry that a digitized sample is available to be written into the WFM; derived from AWCK.	11
AWCK	Acquire Waveform Clock—Indicates to the Memory that a digitized sample is available to be written into the WFM.	3,11,14
AWCKE	Acquire Waveform Clock Enable—Enables the acquire waveform clock generator on the Time Base board.	14,15
AUXBLANK	Auxiliary Blanking—Causes the crt beam to be blanked (becomes the AUX Z AXIS signal).	3,8,13

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TABLE 2-3 (CONT)
Signal Name Dictionary

SIGNAL NAME	DESCRIPTION	LOCATED ON DIAGRAM*
AUX Z AXIS	Auxiliary Z Axis—Signal to the mainframe that controls the blanking of the crt beam (derived from AUXBLANK).	13
BLOCK	Block—Enables writing into the block register on the Memory board.	11
CA	Column Address (Memory Board)—Indicates the presence of a column address.	11
CA, CB and CC	Compression (Display Board)—Selects compression factor of Y-data amplifier.	8,9
CHBLNK	Character Blanking—Causes blanking of crt when a beam is positioned to a blanking field while in the readout mode of the Display circuitry.	8
CH1/CH2	Channel 1/Channel 2—Controls the switching of the CCD output amplifier from the channel 1 signal to the channel 2 signal.	3,7,14
CLR	Clear—Buffered reset line.	12
CS	Chip Select—Enables the EAROM on the MPU board for a read or a write.	12
D0-D7	Data Bus—Microprocessor data bus; distributed generally throughout the 7D20.	2,3,8,10,11,12
DA0-DA9	Display Address—Generated by the display address generator; indicates where in the WFM that waveform data to be displayed is located.	11
DAGSSE	Display Address Single Step Enable—Enables the single step function of the display address generator on the Memory board.	11
DISPINTR	Display Interrupt—Inhibits the Memory from sending data from the WFM to the Display board, interrupts the μp at end of display cycle, and is used to create the sweep gate & holdoff signals.	8,11,12,13
DISPLAY LENGTH COUNTER SINGLE STEP	Display Length Counter Single Step—Increments the display length counter on the Display board one count.	8
DOTS	Dots—Enables the dots mode of the Display circuitry, when low, and the vector mode when high.	8,9
DSA	Display Start Address—Causes the display start address to be loaded into the display address generator (Memory board).	11
E	E—Microprocessor address/data timing signal.	12
EA, EB and EC	Expansion—Selects expansion factor of Display circuitry Y-data amplifier.	8,9

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TABLE 2-3 (CONT)
Signal Name Dictonary

SIGNAL NAME	DESCRIPTION	LOCATED ON DIAGRAM*
EDRD	End Fast Ramp Down—Causes an additional phase clock cycle to be inserted between the trigger and STG during self test of the fast ramp circuit on the Time Base board.	15,16
EHO	End Holdoff—Indicates the end of the 1024 count holdoff period that occurs at the beginning of each acquire waveform cycle of the Time Base.	15,16
ENDACQ	End Acquire—Indicates to the Memory that the last of the digitized samples have been sent to the WFM.	3,11,15
END DISPLAY CYCLE	End Display Cycle—Resets the display length counter on the Display board.	8
ERD	Extended Real-Time Digitizing—Enables the extended real-time digitizing time base mode.	14,15
EXTCLK	External Clock—External clock signal applied to the time base via the front-panel EXT CLOCK connector.	3,14
EXT CK POLARITY	External Clock Polarity—Selects the polarity of the external clock signal that is applied to the sample clock multiplexer on the Time Base board. This signal is the same as PCKMC it is only used in the EXT CK timebase mode. PCKMC is relevant only in the ERD & ETD timebase modes.	14,15
EXTEN	External Enable—Causes data and addresses from the microprocessor to be output to the various circuits of the 7D20.	12
EXT TRIG	External Trigger—External trigger signal applied to the trigger board via the front-panel EXT TRIG connector.	13
FAST RAMP	Fast Ramp Bus—Fast ramp data from the Time Base board that is sent to the MPU board via the serial data bus.	15,16
FI	Fast In—Enables the fast-in phase of signal acquisition in the ERD and ETD time base modes.	3,6,15
FISO and FISO	Fast-In, Slow-Out—Enables the fast-in, slow-out signal acquisition technique used in ERD and ETD time base modes.	13,14
FISOB	Fast-In, Slow-Out Buffered—Buffered version of FISO.	3,6,13
FPSEL	Front-Panel Select—Enables front-panel functions to be selected.	2,3,12
FREERUN	Freerun—Enables the freerun mode of the trigger circuit.	12,13
GENSELA and GENSELB	General Select—Enable lines from the MPU board that enable various circuits to decode address and other control lines.	11,12,15 8,10,12

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TABLE 2-3 (CONT)
Signal Name Dictionary

SIGNAL NAME	DESCRIPTION	LOCATED ON DIAGRAM*
GPIBINT	GPIB Interrupt—Indicates to the MPU board that the GPIB interface controller is requesting service.	2,3,12
GPIBSEL	GPIB Select—Enables the GPIB interface controller.	2,3,12
GSA	General Select A—Enables the Memory board to decode addresses from the microprocessor; derived from the GENSELA line.	11
HORIZ POS	Horizontal Position—Selects a preset horizontal position for the X-axis amplifier on the Display board.	8,9
HOLDOFF	Holdoff—Mainframe interface signal for use with storage mainframes.	13
INEX	Internal External—Selects the hardware port address decoder on the MPU board.	12
INIT	Initialize—Causes the time-base acquire control circuitry to be initialized at the beginning of an acquire waveform cycle.	15
INS	Input Strobe—Enables the phase clock signal to be supplied by the phase clock multiplexer on the Time Base board.	14,15
KEYSEL	Key Select—Causes the setting of the front-panel pushbutton switches to be sent to the MPU board.	1,2
KNOBSEL	Knob Select—Causes the settings of the front-panel knobs to be sent to the MPU board.	1,2
LA, LB, LC and LD	Latch—Selects the time with respect to the Memory circuitry time slots, when the LATCK is enabled.	11
LATCK	Latch Clock—Causes data to be latched to the outputs of the self test latches on the Memory board.	11
LATEN	Latch Enable—Causes the address on the MPU board address bus to latched into the address latch.	11
LINE TRIG	Line Trigger—Line trigger source from the mainframe.	13
LOAD	Load—Causes the preset count to be loaded into post-trigger counter on the Time Base board.	15
LWD0-LWD7	Latched Waveform Data—Waveform data that is carried from the Memory to the Display circuitry.	3,8,11
MA0-MA7	Memory Address Bus—Addresses for locations in the WFM on the Memory board.	11
MAGCLK	Magnifier Clock—Clock signal that increments the horizontal D-to-A converter to produce 10 times magnification of the horizontal display (HMAG).	3,8,11
MD0-MD7	Memory Data Bus—Data lines into the WFM.	11

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TABLE 2-3 (CONT)
Signal Name Dictionary

SIGNAL NAME	DESCRIPTION	LOCATED ON DIAGRAM*
MEA	Memory End Acquire—Indicates that the acquire address generator in the Memory circuitry has reached its maximum count.	3,11,15
MWFM	Memory Waveform Memory—Enables the WMEMSEL line.	12
OFFSET	Offset—Enables the offset DAC on the Display board.	8,9
PCK and PCK	Phase Clock—Time Base signal that controls the clocking of the Time Base and CCD circuitry.	14,15,17
PCKE and PCKE	Phase Clock ECL—Time Base signal that controls the clocking of the CCD circuitry; derived from PCK and PCK. Also used by the trigger for self test.	3,6,13,14
PCKMA, PCKMB and PCKMC	Phase Clock Multiplexer—Selects the output from the phase clock multiplexer circuit on the Time Base board. PCKMC is the same signal as EXT CK polarity. PCKMC is used in the ERD & ETC time base modes, while EXT CK polarity is relevant only in the EXT CK time base mode.	14,15
POWERON	Power On—Indicates that the 7D20 is powered up.	12
PRWS	Microprocessor Read, Write Select—Enables μp access to WFM during the acquire timeslots when row, and display timeslots when high.	11
PWRDN	Power Down—Indicates to the MPU board that the 7D20 is powering down.	3,10,12
Q	Q—Microprocessor address/data timing signal.	12
RA	Row Address—Indicates the presence of a row address.	11
RAS	Row Address Select—Causes the WFM devices on the Memory board to read a row address.	11
RC1-RC4 RR1-RR4	Relay Control—Controls the relays on the attenuator boards.	3,4,10
RECALL	Recall—Causes data stored in the electrically erasable ROM portion of the EAROM on the MPU board to the written into the RAM portion of the device.	12
REFRESH	Refresh—Enables the refresh function of the Memory board.	11
REMOTE	Remote—Indicates that the 7D20 is being remotely controlled; causes front-panel REMOTE indicator to light.	1,2
R/W	Read/Write (Memory Board)—Controls the read and write functions of the Memory board.	11
RMA	Read Memory Address—Causes WFM address to be latched into self test latch.	11

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TABLE 2-3 (CONT)
Signal Name Dictionary

SIGNAL NAME	DESCRIPTION	LOCATED ON DIAGRAM*
RMD	Read Memory Data—Causes WFM data to be latched into self test latch.	11
SC	Start Conversion—Initiates the A-to-D conversion of the CCD output circuitry A-to-D converter.	3,7,14
SCKB and SCKC	Sample Clock—Selects sample clock decade on Time Base board.	14,15
SCKMA, SCKMB and SCKMC	Sample Clock Multiplexer—Selects output of sample clock multiplexer on Time Base board.	14,15
SCK1, SCK2 and SCK3	Serial Data Clocks—Three clock signals that the microprocessor generates to synchronize the transfer of data between the MPU board and the other circuits in the 7D20.	3,5,12,13,15
SDI	Serial Data In—Serial data from the microprocessor that is used to set-up various circuits in the 7D20.	3,5,12,13,15
SDO	Serial Data Out—Serial data from various circuits in the 7D20 that is transmitted to the microprocessor.	3,12,13,15
SDS	Serial Data Strobe—Writes serial data into serial data latches in various circuits in the 7D20.	3,5,12,13,15
SELEN	Select Enable—Enables hardware ports on MPU board to be addressed.	12
START DISPLAY CYCLE	Start Display Cycle—Enables the display length counter on the Display board.	8
SNOR	Initiates the storage of the data in the RAM portion of the MPU board EAROM into the ROM portion of the device.	12
SO	Slow Out—Initiates the slow out phase of signal acquisition for the Time Base circuitry.	14,15
SSRST	Single Sweep Reset—Resets the single sweep circuit.	
SINGLE SWEEP READ INDICATOR	Single Sweep Ready Indicator—Indicates the Trigger circuit is reset and ready to accept a single sweep trigger.	13
STG	Synchronized Trigger Gate—Indicates to the post-trigger counter on the Time Base board that a valid trigger has been received.	15,16
STORE	Store—Causes data in the RAM portion of the EAROM on the MPU board to be stored in the electrically erasable ROM portion of the device.	12
SWEEP GATE	Sweep Gate—Mainframe interface signal.	13

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TABLE 2-3 (CONT)
Signal Name Dictionary

SIGNAL NAME	DESCRIPTION	LOCATED ON DIAGRAM*
TGE and TGE	Trigger Gate ECL—Trigger signal that the trigger circuitry generates.	3,13,16
TGT	Trigger Gate TTL—TTL compatible version of TGE-goes high when triggered.	16
TGP	Trigger Gate Pulse—Indicates when the a trigger occurs; derived from TGE and TGE.	15,16
TRIG'D	Triggered—Lights the front panel TRIG'D light.	1,2
TRIGRST	Trigger Reset—Causes the trigger circuitry to reset at the beginning of an acquire waveform cycle. It is the complement of EHO.	3,13,15,16
VSCK	Valid Sample Clock—Indicates that a valid sample is available from the CCD circuit; clocks the Time Base post-trigger counter.	14,15
WD0-WD7	Waveform Data Bus—Data lines out of the WFM.	11
W/R	Write/Read—Microprocessor signal that selects either a write or a read operation.	2,3,11,12
WMEMSEL	Waveform Memory Select—Enables the Memory to receive data from or transmit data to the microprocessor.	11,12
WMS and WMS	Waveform Memory Select—Enables the Memory to receive data from or transmit data to the microprocessor; derived from WMEMSEL.	11
XCK	X Data Clock—A clock derived from 400kHz (2) used to clock the X data MPX/Latch and control logic.	8
XD0-XD9	X-Axis Display Bus—Digitized X-axis data that is applied to the X-axis DAC on the Display board.	8,9
XY0 and XY1	X-Y Bus—The two least significant bits of the X-axis location in the cursor display mode of the Display circuitry.	8
X10 CLOCK	X10 Clock—Clocks the display length counter in the horizontal magnifier mode; Same as MAG CK.	8
X2 CLOCK	X2 Clock—Clocks the display length counter.	8
X1 CLOCK	X1 Clock—Clocks the display length counter.	8
YD0-YD7	Y-Axis Display Bus—Digitized Y-axis data that is applied to the Y-axis DAC on the Display board.	8,9
820 GAIN COMP	820 Gain Compensation—Changes gain of the X-axis DAC on the Display board in the ERD time base mode.	8,9
820/1024	820/1024—Selects either 820 or 1024 counts for the Display board display length counter, depending on the time base mode used.	8

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DETAILED CIRCUIT OPERATION

This part of the Theory of Operation section provides a detailed description of the electrical operation of the 7D20. Complete schematic diagrams are provided in Section 7, Diagrams and Circuit Board Illustrations. The number enclosed in a diamond preceding a block of text indicates the schematic diagram of the circuitry being discussed. Shaded borders on the schematic diagram indicate the major circuits on the diagrams. The titles of these major circuits correspond to the titles in the following circuit descriptions. The number of the self-diagnostic test that relates to a particular circuit is also given along with the circuit name.

TEKTRONIX DRAFTING CONVENTION

Logic symbols on the schematics are drawn according to the function that the device performs in its particular application. This convention occasionally results in some deviations from the manufacturer's assigned symbology, even though the device's electrical operation is identical. An example of this would be an AND gate (all inputs high—output high; any input low—output low) drawn as an OR gate for low inputs (any input low—output low; all inputs high—output high). For individual device characteristics, refer to the manufacturer's data book.

1 SWITCH BOARD

The front-panel Switch circuitry is located on the Switch board (A1). It transmits the front-panel pushbutton and knob-switch settings to the microprocessor.

PUSHBUTTON SWITCHES

The front-panel pushbutton switches are wired into a 7 by 8 matrix. The microprocessor scans the front-panel pushbutton setting approximately every 20 ms.

Each row of switches is connected to a buffer segment of 8-bit buffer U330. Nominally, these buffers are each connected to +5 V through a 4.7 kΩ resistor. Each column of pushbuttons is connected to an output of decoder U320. In order to read the settings of the pushbuttons, the microprocessor sets the $\overline{\text{KEYSEL}}$ line low (through U335 on the LED board—A2), which enables U320 and U330. It then uses address lines A0, A1 and A2 (also from the microprocessor) to set each of the U320 Y open collector outputs low in sequence. When Y0 is low, for example, each pushbutton switch in column zero that is engaged pulls the input to its respective buffer low. The microprocessor then reads the outputs of U330 through the data bus (D0-D7), interpreting the lows as an engaged pushbutton switch.

KNOB SWITCHES

The front-panel TIME/DIV, CH 1 VOLTS/DIV and CH 2 VOLTS/DIV knob switches use binary-coded contacts to select the switch settings. Each contact is connected to the microprocessor via inverting multiplexer U420 and U320. As with the pushbutton switches, each contact on the knob-switches is nominally held at +5 V. When a contact is closed, its associated input to U420 and U320 is set to 0 V. The microprocessor reads the knob settings through the data bus (D0-D7). A low on the $\overline{\text{KNOBSEL}}$ line (through U335 on the LED board, A2) enables U420 and U320. Address line A3 then selects which contacts are connected to the data bus. For example, depending on the state of line A3, either S130 (VOLTS/DIV) or S430 (TIME/DIV) controls the four output lines of U420.

2 LED BOARD

The front-panel LEDs, variable controls and the GPIB connectors are located on the LED board (A2).

LEDs

Seven 8-bit shift registers (U140, U500, U100, U110, U120, U130 and U310) control the front-panel LEDs. Data is supplied to the shift registers via the microprocessor data bus (D0-D6). The reset (pin 9) and the B input (pin 2) of each shift register are wired to +5 V. Each time the clock input (pin 8) receives a positive-going edge, the data at pin 2 is clocked into the shift register.

Dual decoder U335 supplies the clock signal for the shift registers through its Y3 output. The channel 2 enable (pin 14) of U335 is wired to ground, which permanently enables it. When the W/$\overline{\text{R}}$ and A4 lines are high, the microprocessor then toggles the front panel select ($\overline{\text{FPSEL}}$) line to clock the shift registers.

To read the front-panel pushbutton switches and knob switches on the Switch board, the W/$\overline{\text{R}}$ line is set low. The A4 and $\overline{\text{FPSEL}}$ line then activates either the knob select ($\overline{\text{KNOBSEL}}$) or key select ($\overline{\text{KEYSEL}}$) lines (see the switch board discussion).

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GPIB INTERFACE

The 7D20 can communicate with peripheral test equipment and processors via the bi-directional general purpose interface bus (GPIB). GPIB information can be transmitted through either the front-panel IEEE STD 488 PORT connector (J650) or internal connector (P120). An internal cable (R7603 option 20) is required between P120 on the LED board (A2) and P120 on the Trigger board (A10) in order to use the mainframe, rear-panel GPIB interface.

GPIB interface controller U720 handles the handshaking between the microprocessor data bus (D0-D7) and address bus (A0-A2), and the GPIB bus. Bi-directional buffers U430, U730 and U735 buffer the data between the data bus and GPIB bus, and U720. The GPIB select ($\overline{\text{GPIBSEL}}$) line from the microprocessor controls the chip enable (pin 3) input to U720. The W/$\overline{\text{R}}$ and A4 lines control the write enable (pin 4) and DBIN (pin 5) inputs to U720. The $\overline{\text{GPIBSEL}}$ and W/$\overline{\text{R}}$ lines control the enabling of U430 and the selection of the data transmission direction, respectively.

3 INTERCONNECT

The interconnect diagram 3 shows wiring between circuit boards, and the accompanying signal names. The Interconnect Functional Block Diagram in diagram 17 shows the functional relationship of these signals to the major circuits in the 7D20. Diagram 3 is thus useful for tracing signals through the various boards and connectors in the plug-in. Diagram 17 is useful for determining the routing of signals within the plug-in.

Table 2-3 provides a summary of the signals in the 7D20 and a brief description of the function of each.

4 CH 1 AND CH 2 ATTENUATOR

The Channel 1 and Channel 2 Attenuator circuitry is located on Attenuator assemblies A12 and A13, and Preamp board A4. It contains a two-decade attenuator circuit, an impedance converter amplifier circuit and a step attenuator circuit. Identical signal input and attenuator circuitry is provided for each input channel; therefore, only the Channel 1 circuitry (assembly A12) is discussed in the following description.

SIGNAL INPUT AND DECADE ATTENUATOR (Self Tests 53 and 58)

Attenuator assembly A12 is a hybrid circuit that contains relays, precision (laser trimmed) resistors and compensation capacitors. It provides an input connector for the Channel 1 signal and decade attenuation (÷1, ÷10 and ÷100) of the signal.

The relays on the assembly are permanent magnet, latching relays; a pair of coils controls each relay. One coil controls one state of the relay and the other coil controls the other state. For example, when RC3 is in its low state, a positive-going gate applied to CR1211 causes the relay to assume its ÷1 state; a positive-going gate on CR1212 causes it to assume its ÷10 state. Since these relays are bistable, they only need to be activated for a short time to cause them to change states. They then remain in that state until activated again, at which time they switch to their alternate state.

NOTE

A low selects an RC line; a high selects an RR line. Only one RC and one RR line can be selected at a time for each channel.

TABLE 2-4
Signal Input and Attenuator Relay Control

LOW	RC1	RC2	RC3	RC4
HIGH				
RR1	AC(Ch 2)	SIG(Ch 2)	÷1(Ch 2)	÷1/÷10(Ch 2)
RR2	DC(Ch 2)	GND(Ch 2)	÷10/÷100(Ch 1)	÷100 (Ch 2)
RR3	AC(Ch 1)	SIG(Ch 1)	÷1(Ch 1)	÷1/÷10(Ch 1)
RR4	DC(Ch 1)	GND(Ch 1)	÷10/÷100(Ch 2)	÷100(Ch 1)

NOTE

A low selects an RC line; a high selects an RR line. Only one RC and one RR line can be selected at a time for each channel.

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The relays are configured in a matrix (see Fig. 2-5). The microprocessor controls the relay control lines (RR1 through RR4 and RC1 through RC4) via multiplexers located on the Power Supply board (see diagram 10).

Each attenuator has two relays that control ÷10 (decade) attenuators. The two decade relays thus allow ÷1, ÷10 and ÷100 signal attenuation. Table 2-4 shows the state of the relay control lines for the various states of the relays and the front-panel switches.

The Attenuator assembly also contains a latching-relay that selects dc or ac coupling, and another latching-relay that grounds the input to the preamplifier through a 50 Ω resistor. For self test purposes, a test signal can be applied to the preamplifier circuit through Q1230 and R1222, when $\overline{ICS}$ is in its low (active) state.

Many Tektronix probes contain resistors, which are used to indicate the attenuation of the probe on the crt readout display. This resistance is connected to the oscilloscope via the probe coding ring on the BNC connector. When the probe is connected to the oscilloscope, the probe coding ring connects to a probe coding line (PC1 for Channel 1 and PC2 for Channel 2), which is in turn connected to the analog bus (ABUS) via multiplexer U230 (see diagram 5). The microprocessor monitors the ABUS during normal operation and determines the probe attenuation by measuring the voltage across the prboe resistor. The probe attenuation factor is used to set the readout scale factor.

IMPEDANCE CONVERTER AMPLIFIER

The impedance converter amplifier circuit current-amplifies the input signal and provides unity voltage gain. DMOS FET Q1012 (operating in a source-follower mode) amplifies the high frequency component of the signal. Operational amplifier U1100 provides low-frequency signal amplification and stability for the circuit. Complementary amplifier Q1010 and Q1021 provides further current amplification and a single-ended output. Q913 and Zener diode VR1000 set the bias on Q1012. Q1020 is a current source for the circuit.

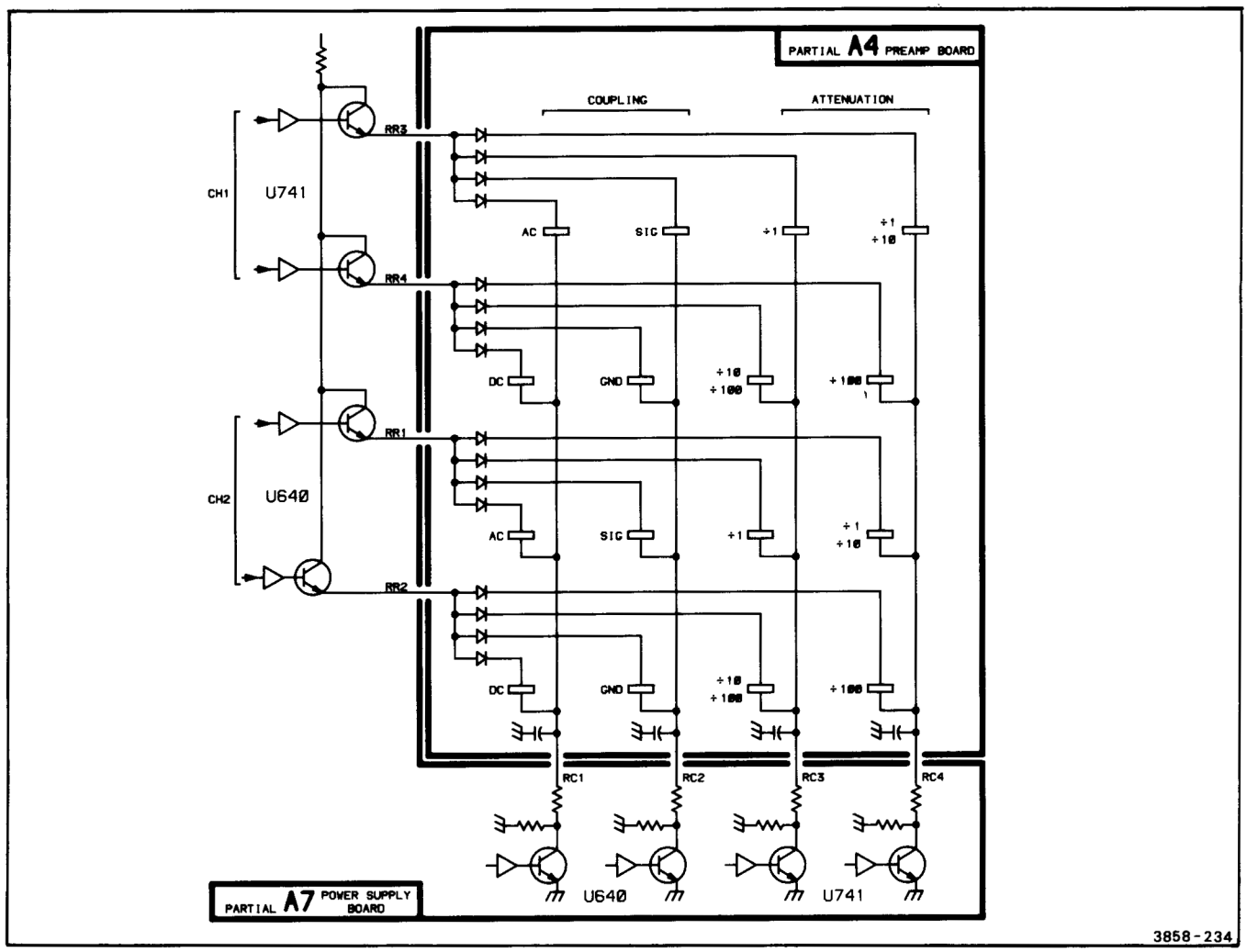

Figure 2-5. Simplified schematic diagram of attenuator board's relay controls.

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Feedback network R1010, R1013, R1002 and the LF Gain 1 adjustment (R1003) provide feedback gain control for the amplifier. Step Bal 1 adjustment R902 sets the dc level at the junction of R1011 and R1012, and thus allows the balance of the step attenuator to be adjusted. Signal feedback through C1100 reduces substrate capacitive loading in U1100. Variable capacitor C1020 provides high frequency gain adjustment. Variable capacitor C1011 provides input capacitance compensation.

Diode CR1110 provides overvoltage protection for positive-going peaks; diodes CR1111 and CR1021, and the base-emitter junction of Q1020 provide overvoltage protection for negative-going peaks.

STEP ATTENUATOR (Self Tests 53 and 57)

Divider R916, R915 and R913 provide step attenuation of the input signal (÷1, ÷2 and ÷5). DMOS FETs Q922, Q920, Q911 and Q910, which are used as switches, control the transmission of the signal through the attenuator (see Table 2-5). Quad operational amplifier U910 (used as a comparator) controls the FETs, using data that the MPU supplies through step attenuator control lines LZ1 through LZ4. Table 2-5 shows the signal attenuation obtained from the various states of these lines.

Q921 blocks any blow-by that might occur through Q922 and Q920 in the ÷2 and ÷5 attenuator modes, when they are turned off.

5 VERTICAL PREAMP AND CONTROL

The Vertical Preamplifier and Control circuitry is located on the Preamp board, A4. It contains the vertical preamplifier circuits for channels 1 and 2, the attenuator and preamplifier control circuits, and the preamplifier analog bus multiplexer.

VERTICAL PREAMPLIFIERS (Self Tests 52, 55, 56, 59 and 60)

Since the preamplifier circuits for Channels 1 and 2 are almost identical, only Channel 1 is discussed. The preamplifier consists of input amplifier U710 and differential amplifier Q610 through Q613.

Monolithic preamplifier U710 contains a high-frequency, differential amplifier. The input signal from the attenuator circuit (SAT1) is applied to pin 14. Dual emitter input transistors in U710 allow two different frequency and gain compensation networks to be used: one for signals obtained at 5 mV/division vertical sensitivity (pins 1 and 16) and one for signals obtained at ≥10 mV/division (pins 2 and 15).

Transistor Q300 is a current source for U710. Q800 and Q801 switch the current to one compensation network or the other, depending on the state of the GC1 line: a low on GC1 selects the 5 mV/division network; a high selects the ≥10 mV/division network.

The 5 mV Gain adjustment R820 and 5 mV Offset adjustment R801 allow the 5 mV/division gain network to track the ≥10 mV/division network. Ch 1 Position Offset adjustment R720 and Ch 1 Gain Adjustment R344 (located in the output amplifier; Diagram 6) provide overall dc offset and gain adjustment for the preamp. Ch 1 Position Gain adjustment R821 controls the range of the front panel CH 1 POSITION control. R810 and C813 provide high frequency compensation adjustment for the ≥10 mV/division network.

The differential output signal at pins 8 and 9 of U710 is applied to differential shunt-feedback amplifiers Q610 and Q611, and Q612 and Q613. Feedback through R603 and R622 produces a virtual ground at the bases of Q611 and Q613, so that very little signal voltage appears at the input. R710 and C710 allow for adjustment of high frequency compensation. Diodes CR610 and CR611 protect Q610 and Q612 from damage if J1 or J2 is accidentally grounded. The resulting differential output signal is equal to approximately 25 mV for each vertical division of the display on a 7000-Series mainframe crt screen. The signal is applied to coaxial connectors J1 and J2, with output impedances of 50 Ω provided by R611

TABLE 2-5
Step Attenuator Control

LZ1	LZ2	LZ3	LZ4	Attenuation	FETs On	FETs Off
L	L	X	X	÷1	Q920, Q922	Q910, Q911, Q921
X	X	L	L	÷1	Q950, Q951	Q940, Q941, Q952
H	L	X	X	÷2	Q911, Q921	Q910, Q920, Q922
X	X	H	L	÷2	Q941, Q952	Q940, Q950, Q951
L	H	X	X	÷5	Q910, Q921	Q911, Q920, Q922
X	X	L	H	÷5	Q940, Q952	Q941, Q950, Q951

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and R612, and to Q500 and Q510 for further amplification.

Transistors Q500 and Q510 produce a single-ended trigger signal, which is applied to the trigger circuit via J5. R518 adjusts the offset of the trigger output stage, which produces a trigger signal with a sensitivity of approximately 25 mV/division. Q400 and Q410 current-amplify the differential trigger signal, which is then applied to the 7000-series mainframe interface through P810 pins A13 and B13.

ATTENUATOR AND PREAMPLIFIER CONTROL

Shift register U1230 and U300 receive attenuator and preamplifier control data from the serial data bus (SD1) at P810 pin 5B. These shift registers then distribute this control data to the attenuator and preamplifier circuits.

Clock signal $\overline{SCK1}$ and strobe signal SDS are applied to U1230 and U300 through P810 pins 4B and 3B, respectively. $\overline{SCK1}$ clocks the serial data through U1230 and U300. SDS latches the data to the outputs of the shift register at the end of 16 clock cycles.

$\overline{ICS}$ (pin 11 of U1230) activates a test signal, which is applied to the preamplifier circuits through Q1230 in the signal input and decade attenuator circuits (see Diagram 4). LZ1 through LZ4 control the step attenuator circuits (see Diagram 4). GC1 and GC2 select the gain networks for U710 and U740, respectively (see discussion of preamplifier circuits).

FC1 and FC2 force the channel 1 preamplifier and channel 2 preamplifier, respectively, to operate in the calibrated mode, regardless of the settings of the front panel VARIABLE VOLTS/DIV controls, R100 and R130.

When FC1 is low, the voltage on the wiper of R100 is transmitted through analog switch U340C to pin 12 of U710 via R722, which in turn controls the gain of U710. (When the CH 1 VARIABLE control is in its CAL position, 5 V is applied to pin 5 of U340C.) When FC1 is high, U340C disconnects the CH 1 VARIABLE control from the circuit and forces +5 V (calibrated level) on pin 4 of U340C.

The voltage level on pin 12 of U710 controls a current steering circuit inside the amplifier. This circuit determines the gain and polarity of the output signal (see Fig. 2-6). In the case of Channel 1, only a positive voltage is applied to pin 12. The CH 1 VARIABLE control thus decreases the gain of the amplifier from its calibrated gain to approximately 0.4 of its calibrated gain; the channel 1 preamplifier output signal polarity can only be non-inverting.

Analog switch U340A performs the same function for the CH 2 VARIABLE control as U340C does for Channel 1. In this case, however, analog switch U340D and operational amplifier U331 provide a voltage inversion for

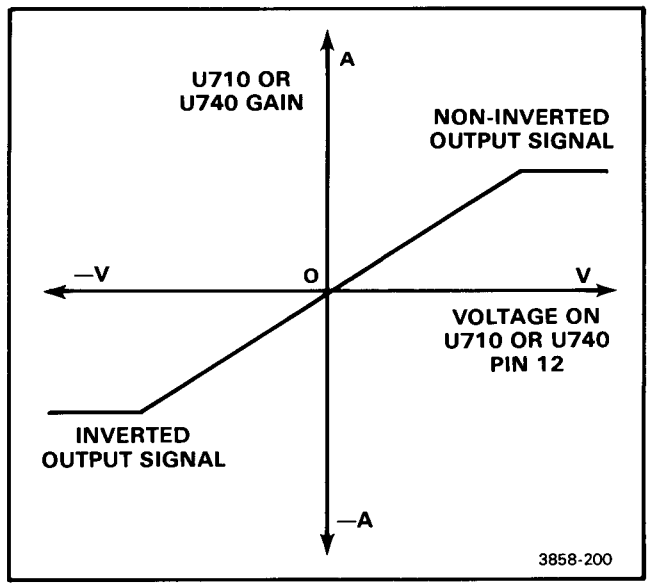

Figure 2-6. Effect of VOLTS/DIV VARIABLE control on preamplifier circuit gain.

inverted signal operation. The INV line selects inverted operation for the Channel 2 preamplifier circuit. When INV is low, the calibrated level is transmitted through pin 12 of U340D to pin 3 of U331. U331 in this case operates in voltage follower mode; the positive calibration level is thus applied through R753 to pin 12 of U740, creating a non-inverted output signal. When the front panel CH 2 INV pushbutton is engaged, the INV line is pulled high. Pin 3 of U331 is then grounded through R335, causing U331 to operate as an inverting amplifier with a gain of 1. The resulting negative voltage on pin 12 of U740 thus produces an inverted output signal.

PREAMPLIFIER ANALOG BUS MULTIPLEXER

The preamplifier analog bus multiplexer circuit multiplexes seven signals onto the two analog buses (ABUS1 and ABUS2). Control lines A, B and INH from U1230 control multiplexer U230. Table 2-6 shows the signals transmitted to the analog buses for the various states of the A, B and INH lines. (Note that a high on the INH line disables both the X and the Y outputs of U230.)

Operational amplifiers U330A, U330B, U231A and U231B, and analog switch U350B and U350C combine to produce an analog signal that contains probe coding information and indicates whether the vertical gain VARIABLE control is in its calibrated (CAL) or uncalibrated position.

The Channel 1 variable gain voltage level at pin 4 of U340C drives the output of U330A to either 0 V (calibrated mode) or +5 V (uncalibrated mode). In the calibrated mode, the probe coding resistance is connected through the PC1 line and analog switch

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TABLE 2-6
Preamplifier Analog Bus Multiplexer U230 Control

B	A	INH	ABUS1	ABUS2
L	L	L	Ch 1 Probe Coding/Gain CAL-Uncal	Ch 2 Probe Coding/Gain CAL-Uncal
L	H	L	Ch 1 Trigger	Ch 2 Trigger
H	L	L	Vertical Display Signal	Open
H	H	L	Ch 1 Position	Ch 2 Position
X	X	H	No Signal	No Signal

U350B to resistor R243. U231A thus operates in a voltage follower mode, producing a positive voltage level at pin 12 of U230. The probe coding resistance factor determines the voltage level of the output and thus indicates the attenuation of the probe.

In the uncalibrated mode, U350B switches the pin 3 input to U231A to ground through R243, converting U231A into an inverting amplifier with unity gain. The probe coding resistance factor then produces a negative voltage level at pin 12 of U230, indicating not only the attenuation of the probe, but also that the Channel 1 preamplifier is operating in its uncalibrated mode.

U330B, U350C and U231B perform the same function for the Channel 2 calibration indication signal and the probe coding resistance factor transmitted through PC2.

The CH 1 and CH 2 front-panel POSITION control levels (or levels produced in self tests or program modes) are applied to P830 pins 12 and 2 and connected to U230 pins 11 and 4, respectively, via damping resistors R232 and R140.

VERTICAL DISPLAY SIGNAL AMPLIFIER (Self Test 37)

The Vertical Signal (the vertical component of the display readout information) is applied to the Preamp board at P830 pin 1. U240A and U240B convert this signal into a push-pull signal. R230 and R240 provide a 50 Ω output impedance. The differential signal is applied to the 7000-series main interface via pins A11 and B11. In addition, the - signal is applied to U230 for selection via ABUS1 during self test.

CCD DRIVERS

The Charge Coupled Device (CCD) Driver Circuitry is located on the CCD board, A5. It contains the preamplifier output amplifier circuits, the CCD circuits and the CCD control circuit. See the introduction to this section for a discussion of CCD theory.

PREAMP OUTPUT AMPLIFIER (Self Test 61)

The preamp output amplifier circuits amplify the output of the preamplifier, shift the signal levels and match the preamplifier output impedance with that of the CCDs. Since Channels 1 and 2 are identical, only Channel 1 is discussed.

The Channel 1 preamp output amplifier circuit is a differential amplifier with a current gain stage (Q230 and Q250), plus two voltage shift stages, Q340-Q341, and Q440-Q441. Q330 and Q350 form an error correction circuit that compensates for gain changes in the amplifier due to compression and signal induced thermal distortion.

Q350 amplifies and inverts a portion of the (+) half of the differential signal, and adds it to the (-) half of the signal at the summing node at the emitter of Q441. As the (+) signal increases in amplitude, more error correction signal is added to the (-) signal, creating a near linear gain for the (-) half of the amplifier. Q330 performs the same function for the (+) side of the amplifier.

Operational amplifier U280A maintains a constant average output voltage of approximately 3 V at the collectors of Q440 and Q441. A divider composed of R374, R431 and R450 senses the average output voltage and connects it to the + input of U280A. The output of U280A (pin 1) is connected to the base of Q240 through R254, allowing the feedback through R254 to change the collector current until the proper output voltage is attained. Ch 1 Gain adjustment R344 allows the gain of the amplifier to be matched to the CCD voltage gain.

CCD CLOCK

The CCD Clock circuit provides three clock signals for each CCD channel: the input sampling clock, the transport clock and the output sampling clock. The phase and in some cases the width of these pulses change with changes in the time base mode. In the roll, real-time digitizing (RD) and equivalent time digitizing (ETD) time base modes, the clock pulses applied to each CCD channel are coincident. In the extended real-time digitizing (ERD) mode, the clock pulses applied to channel B are shifted one-half clock cycle with respect to the clock signals applied to channel A. These two phases of

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the clock signals support the alternate clocking of the two channels of the CCD that is required in the ERD mode.

Also, in the two fast-in, slow-out modes (ERD and ETD), the width of the transport clock changes between the fast-in and slow-out phases.

The phase clock (PCKE and $\overline{\text{PCKE}}$), ERD and fast-in (FI) signals provide the basic timing and control for the CCD clock signals. Line receivers U871B and U871C, and quad-OR gate U870, decode the PCKE, PCKE and ERD signals into two CCD clock signals at pins 2 and 15 of U870 (see Fig. 2-7).

Gates U870C and U870D control the output signal at pin 15. Line driver U871A holds the output of U870C high all the time. The $\overline{\text{PCKE}}$ signal is thus transmitted through line driver U871B and gate U870D with no change in phase or polarity, regardless of the state of the ERD line.

Gates U870A and U870B control the output signal at pin 2. The ERD line sets the levels on the pin 3 and pin 7 inputs to these gates. When the ERD line is low, pin 7 is held low and pin 3 is held high. The output of U870A is thus held high, and the $\overline{\text{PCKE}}$ signal is transmitted through U870B to the pin 2 output. The outputs at pins 2 and 15 of U870 in the non-ERD modes are thus coincident.

When the ERD line is high, pin 7 is held high and pin 3 is held low. The output of U870B is thus held high and the PCKE signal is transmitted through U870A to the pin 2 output. The outputs at pins 2 and 15 in the ERD mode, are thus shifted one-half clock cycle with respect to one another.

Input Sampling Clock

The signal at pin 15 of U870 is applied to line driver U770A and ECL to TTL converter U651D. The signal at the non-inverting output of U770A is transmitted through U750A to pin 6 of U651B (see Fig. 2-8). The inverted signal at pin 3 of U770A is transmitted through the delaying network made up of R871, L861, C861, L851 and C851. The input signals to OR gate U750A are delayed with respect to each other and produce complimentary outputs at pins 2 and 3. The resulting signal at pin 5 of U651B is thus a 6 ns wide, positive-going pulse, the width of which is set by the delaying network. U650B inverts the signal, and clock driver Q551 and Q553 inverts it again and amplifies it to a peak to peak amplitude of 12 V to produce the input sampling clock.

Gates U750B and U650A, and their accompanying converters, delay network and line driver perform an identical operation to create an input sampling pulse from the pin 2 output of U870. In the ERD mode, however, the input sampling signal at the collectors of Q550 and Q552 is shifted one-half clock cycle with respect to the signal at the collectors of Q551 and Q553.

Transport and Output Sampling Clocks

ECL to TTL converter U651D inverts the pin 15 output of U870 and applies the resulting positive-going pulse to gates U671A and U671B (see Fig. 2-9). U960C inverts the FI signal and applies it to U671B; U960D inverts and delays the U960C output and applies it to U671A. (The delay does not affect the genertion of the transport and output sampling clocks, since the FI signal is essentially a dc level that is shifted between high and low to switch the time base from the fast-in to the slow-out phase (see the discussion of the time base circuitry in this chapter for a detailed description of the fast-in and slow-out phases of the ERD and ETD time base modes).

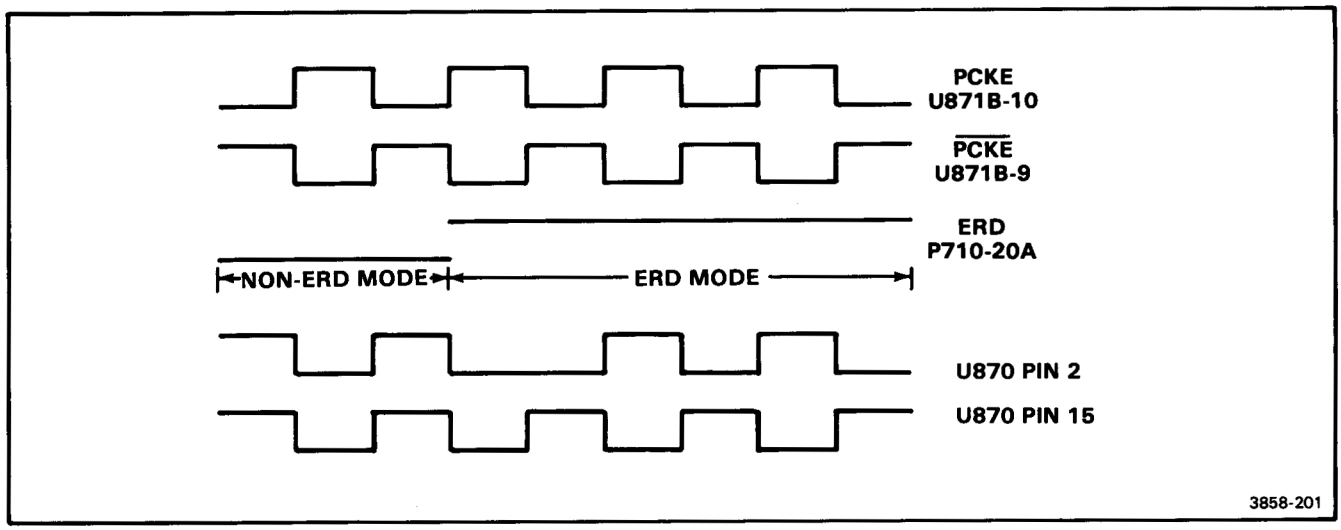

Figure 2-7. Generation of non-ERD and ERD CCD modes.

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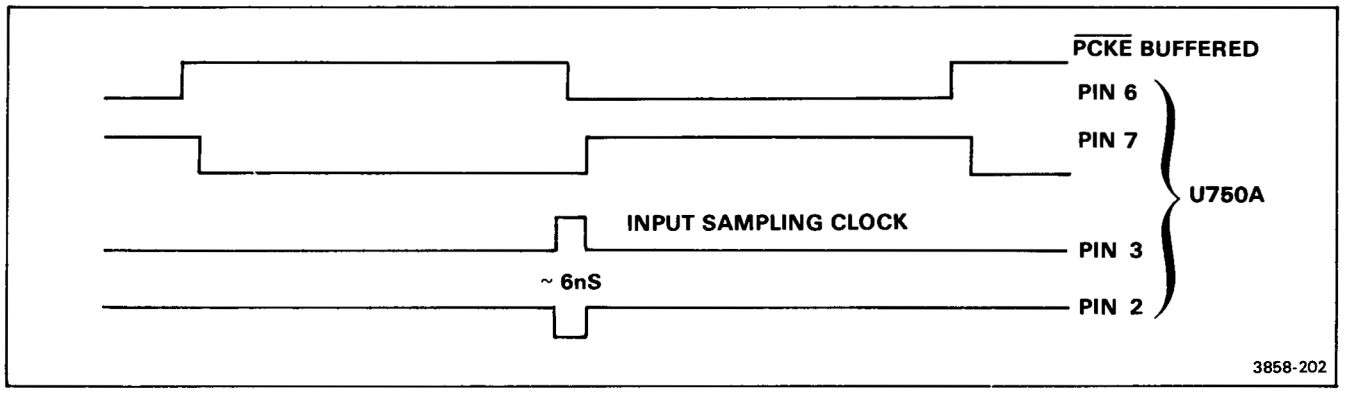

Figure 2-8. Generation of input sampling clock.

Gates U671A, U671B, U670C, U670A and U670B use these signals to create the transport clock and the output sampling clock. These clock signals are slightly different, depending on whether the Time Base is in a fast-in or a slow-out phase.

In the fast-in phase (FI high), the low at pin 4 of U671B holds the output of U671B high, which causes pin 2 of U670A and pin 10 of U670C to be held high (see Fig. 2-9). The high from U960D at its pin 2 input enables U671A. The positive-going pulse applied to pin 1 is thus transmitted through U671A and U670C and delayed approximately 10 ns by delaying network R684 and C684. The resulting signal is transmitted through inverter U670B and clock driver Q561 and Q560, to create the transport clock, a positive-going pulse with a peak-to-peak amplitude of approximately 12 V.

U670A combines the positive-going input at pin 13 with the delayed, negative-going pulse at pin 1, creating a negative-going output pulse at pin 12 with a width of approximately 10 ns. Q570 and Q571 amplify and invert the pin 12 output of U670A, creating a positive-going output sampling pulse with a peak-to-peak amplitude of approximately 12 V.

In this fast-in phase, the input sampling and output sampling pulses are thus raised on the leading edge of the PCKE pulse. The transport clock is then raised 10 ns later on the falling edge of the output sampling pulse.

In the slow-out phase (FI low), U671A is disabled and U671B is enabled. Pin 11 of U670C and pin 1 of U670A are thus held high.U671B and the delaying network R683 and C683 invert and delay the positive-going signal at pin 5 of U671B. U670A then combines the positive-going pulse at pin 13 with the delayed, negative going pulse at pin 2, to create a negative-going pulse at the pin 12 output. R683 and C683 set the width of the pulse at approximately 35 ns.

U670C inverts the delayed, negative-going pulse at pin 10 to create the transport clock. The negative-going, 35 ns pulse at pin 12 of U670A becomes the output sampling pulse.

In the slow-out phase, the input sampling and output sampling clocks are thus raised on the leading edge of the PCKE pulse, and the transport clock is raised 35 ns later on the falling edge of the output sampling pulse.

Gates U671C, U671D, U630A, U630C, U630B and their accompanying clock driver stages perform identical operations to create transport and output sampling clocks from the pin 2 output of U870. In the ERD mode, however, these clock signals are shifted one-half clock cycle with respect to the clock signals described above.

The two channels of each CCD can then be made to acquire samples simultaneously or on alternate half PCKE cycles, depending on the state of the ERD line.

CHARGE COUPLED DEVICES (CCD)

Each of the two CCDs, U440 and U460, has two channels. Channel A samples the (-) side of its associated preamplifier output signal and channel B samples the (+) side of the signal. The CCD clock signals from Q530, Q531, Q540, Q541, Q550 and Q552 are applied to channel A; the CCD clock signals from Q551, Q553, Q560, Q561, Q570 and Q571 are applied to channel B. The two sides of each preamplifier signal are applied to the inputs to the charge injection ports of the CCDs, pins 3 and 13.

When the input sampling clock pulse to channel A of U440 goes high, the (-) side of the Channel 1 preamplifier output signal is sampled. The charge injection port converts the sampled voltage into a charge. On the next transport clock (either 10 ns or 35 ns later, depending on the mode of operation) the transport clock shifts this charge into channel A's first analog shift register cell. On subsequent clock cycles, the transport clock shifts the charge from cell to cell until it reaches the 455th cell. At the beginning of the next cycle, the

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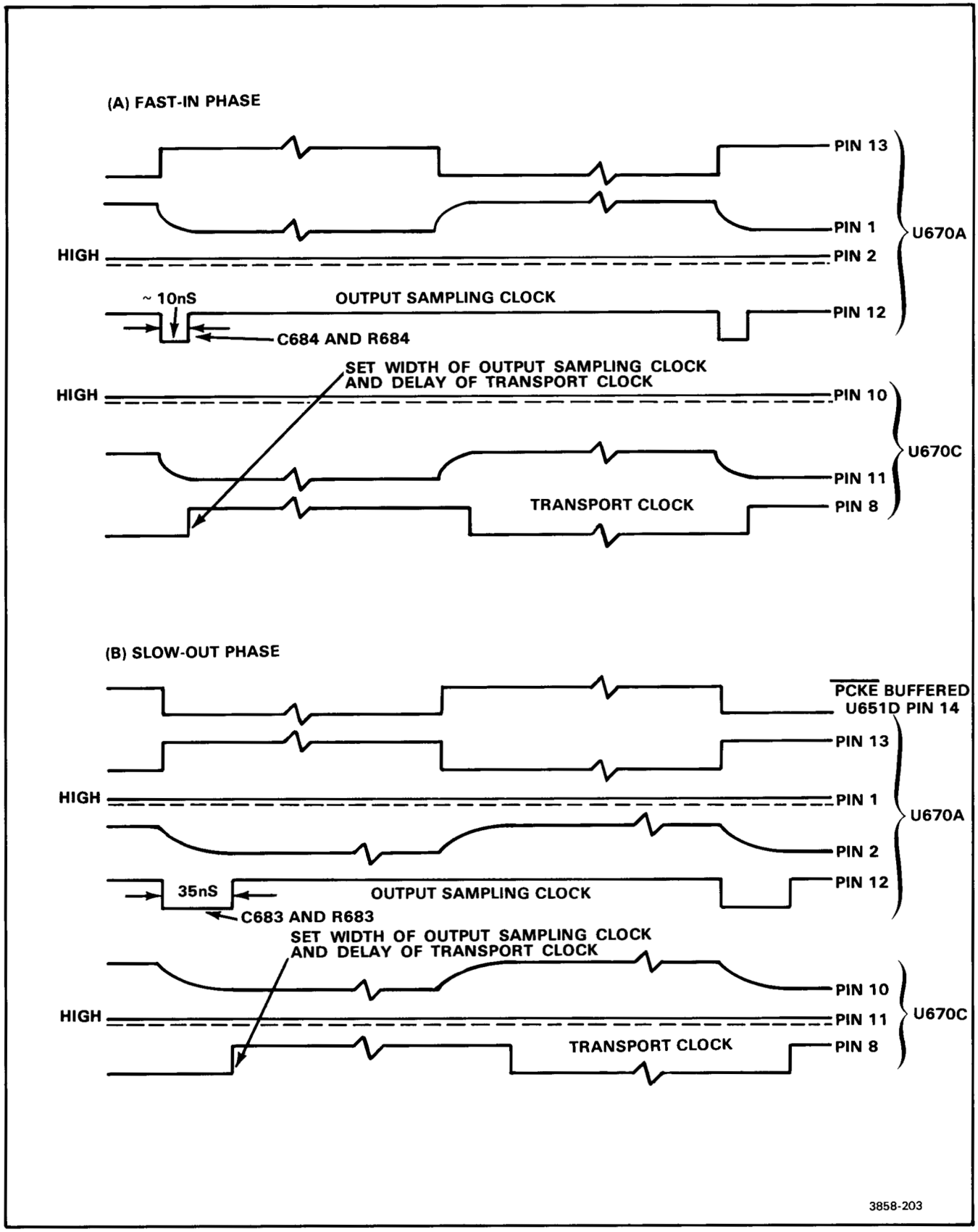

Figure 2-9. Generation of Output Sampling Clock and Transport Clock: (A) Fast-In Phase; (B) Slow-Out Phase.

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output sampling clock shifts the charge on the 455th cell into the channel A output amplifier, which converts it back into a voltage and applies it to output pin 1.

In the ERD mode, the differential samples produced at the CCD output are from two different sample clock edges, i.e., there is a half-clock cycle difference between the time channel A samples the (-) side of the preamplifier output signal and when channel B samples the (+) side. Each digitized sample thus represents the average signal level between the two clock events. This averaging has a negligible effect on the signal except in the case of a very fast transition. In the case of a fast pulse edge, for example, a single dot is generally displayed half way between the two levels, indicating the average of the two levels.

REF1 + adjustment R311 and REF1 - adjustment R310 set the reference voltage levels for the two channels of U440. ERD adjustment R210D provides correction for a baseline shift in reference levels that occurs in the ERD mode. ETD adjustment R210C provides baseline correction in the ETD mode. REF2 + adjustment R111, REF2 - adjustment R110, R210A and R210B provide the same function for U460.

7 CCD OUTPUT

The CCD output circuitry is located on the CCD board, A5. It includes two CCD output amplifiers, analog to digital converter, and a CCD test signal multiplexer.

CCD AMPLIFIERS AND MULTIPLEXER (Self Test 62)

The differential outputs of the two CCDs are applied to two identical differential amplifiers. The Channel 1 CCD output is applied to emitter followers Q430 and Q331, which buffer the signal. CENTERING adjustment R410 balances the input bias on the amplifier, allowing the baseline to be centered on the crt screen. Potentiometer R411, the 1BAL adjustment, allows the gain of the two CCD channels to be matched.

Transistors Q611 and Q610 form a differential amplifier. Operational amplifiers U730A and U730B are part of a gain control bridge that controls the bias on FETs Q710A and Q710B. Q710B in turn acts as a variable resistor, allowing the gain of the amplifier to be varied according to the level of the CH 1 GAIN line.

The front panel CH 1 AQR GAIN adjustment (R202—see diagram 2) adjusts the current conducted by the CH 1 GAIN line and thus controls the current that R1081 conducts. This same current is conducted by R730 and R733. Operational amplifier U730B forces the voltage across R731 to match that across R730 and R733. Operational amplifier U730A senses the common mode voltage at the emitters of Q610 and Q611, and forces the junction of R730 and R733 to this same potential. The voltage across Q710A is thus centered about the same common mode voltage as Q710B. Varying the voltage at the gates of Q710A and Q710B thus causes identical changes in the drain-source resistance of the two FETs. When the current through the CH 1 AQR GAIN line is changed, U730B changes the gate voltage of Q710A and Q710B in order to balance the bridge, which in turn changes the drain-source resistance of Q710B and changes the gain of differential amplifier Q610 and Q611.

Operational amplifier U850A senses the voltage at the junction of R615 and R612, and forces the collector voltage of Q611 and Q610 to be 3 V less than the sensed voltage; Q511 is a current source for the amplifier. Operation amplifier U420A controls the VBE on Q511 and Q510 to maintain a constant current source for both CCD amplifiers.

Q811, Q813, Q821 and Q823 are switching transistors, which pass either channel 1 or channel 2 differential amplifier output current to a current mirror (Q814, Q815, Q824A and Q824B), which develops the voltage signal to drive A-to-D converter U930. Steering transistors Q831 and Q833 control the switching transistors. When either the ADD or the CH 1/$\overline{\text{CH 2}}$ line is high, Q831 is turned off and Q833 is turned on, which in turn causes Q811 and Q823 to conduct. Q823 thus provides a signal path to U930 for the Channel 1 CCD output signal.

The Channel 2 CCD output amplifier operates identically to the Channel 1 amplifier. In this case, a low on the CH 1/$\overline{\text{CH 2}}$ line turns Q832 on and causes the Channel 2 CCD output signal to be applied to U930.

ANALOG-TO-DIGITAL CONVERTER (Self Test 63)

A-to-D converter U930 is a successive approximation A-to-D converter. It converts the analog samples from the CCD output amplifier into 8-bit digital values. Q951 and Q950 provide a 20-MHz clock signal to clock the DAC. Nine clock pulses are required for each A-to-D conversion cycle. A HIGH on the start conversion (SC) line initiates an A-to-D conversion cycle.

CCD TEST SIGNAL MULTIPLEXER

Multiplexer U1050 multiplexes the CM1 (pin 11), CM2 (pin 15) and CCD output signal (pin 2) into the analog buses, ABUS1 and ABUS2. The $\overline{\text{ABCCDE}}$ line enables U1050. The ADD line selects which outputs are applied to the analog buses (see Table 2-7).

TABLE 2-7
CCD Test Signal Multiplexing

	Multiplexer Output	
ADD Line	ABUS1	ABUS2
Low	CCD Signal	CM2
High	No Output	CM1

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DISPLAY

The Display circuitry is located on the Display Board (A6). It is divided into two sections: digital and analog. The digital control section controls the display mode: Y vs. time, X-Y, readout and cursor. The analog section converts the digital display information into an analog signal, which is amplified and applied to the mainframe.

DETAILED BLOCK DIAGRAM DESCRIPTION

The Display circuitry is divided into two parts: digital and analog. The digital part handles the setup of the display modes, control the display cycle, blanking, and the reading of digital data from the WFM. The analog part performs the digital-to-analog conversion and produces analog signals compatible with the mainframe vertical and horizontal display amplifiers.

The mode control data latches (see Fig. 2-10) receive setup data from the microprocessor through the microprocessor data bus (D0-D7), then distribute this data to the display circuits and to other related circuitry in the 7D20.

The display clock receives timing information from the Time Base, which is used to synchronize the Display circuitry with the Memory READ X and READ Y time slots. The display clock also produces a horizontal sweep rate clock, which is used to digitally generate a horizontal ramp. Note that since the input signal to the 7D20 has been digitized, the horizontal sweep rate in the Y vs. time display mode does not need to be referenced to the TIME/DIV setting. The clock multiplexer, which selects the horizontal ramp rate, uses the MAGCK signal from the Time Base in the horizontal magnification mode to create the horizontal ramp.

The display length counter counts the horizontal sweep rate clock and produces a digital horizontal ramp—a series of digital numbers that increase from 0 to 1024 (or 820 in the ERD time base mode).

The display control logic decodes the outputs of the display length counter to begin and end the display cycle. It also controls the $\overline{\text{DISPINTR}}$ line, which indicates to the microprocessor that a display cycle has been completed.

The X temporary latch and Y latch receive X and Y data from the WFM via the latched waveform data bus (LWD0-LWD7). The Y data is then applied to the vertical DAC and the blanking logic. The X data is applied to the X data multiplexer/latch.

The X data multiplexer/latch selects either X data from the WFM, or digital ramp data from the display length counter and applies the data to the horizontal DAC.

The blanking logic controls the AUX Z AXIS line, which controls the blanking of the electron beam of the crt. It provides automatic blanking of the beam at the end of each display cycle. It also provides blanking between data points displayed as dots and between selected portions of the display in the readout mode.

The Display circuitry generates two types of waveform displays: dot or vector. In the dot mode, the crt beam is blanked between the waveform data points. The waveform display thus consists of a series of individual dots. In the vector mode, the beam is slewed between data points to create a more continuous waveform display. The cursor and readout are only displayed in the dot mode.

The horizontal digital-to-analog converter (DAC) converts the X-axis data from the X data multiplexer/latch into an analog voltage signal. Front-panel horizontal gain and position controls allow the amplitude and positioning of the waveform display to be adjusted horizontally to match the mainframe horizontal display amplifier. In the Y vs. time mode, the horizontal signal is a ramp; in the X-Y, readout and cursor modes, the horizontal signal is a waveform, the shape of which depends on the X-axis data received from the WFM.

The vertical DAC converts the Y-axis data into an analog voltage signal. Front-panel vertical gain and position controls allow the vertical DAC to be matched to the gain and position of the mainframe vertical display amplifier. In addition, the vertical DAC circuitry vertically offsets and expands or compresses the signal.

The vector filter allows the vertical and horizontal signals to be transmitted through a filter that slows the transition between data points. The blanking is off during this time.

The output amplifier buffers the vertical and horizontal display signals and provides impedance matching with the inputs to the mainframe vertical and horizontal amplifiers.

The display analog bus multiplexer picks off the vertical and horizontal signals at various stages in their development for use in self test. The microprocessor selects which signal is applied to the analog bus.

TYPICAL DISPLAY CYCLE

A display cycle begins with the latching of display setup data from the microprocessor into the mode control data latches (U600, U1300 and U1305). At the same time, the microprocessor also sets up the display address generator (DAG) on the Memory board. With the Display and Memory circuitry set up for a display cycle, the microprocessor then pulses $\overline{\text{START DISPLAY CYCLE}}$ low through decoder U1400, which sets the Q output of U500A high to initiate the display of a waveform. On the next clock edge from U400B, the $\overline{\text{DISPINTR}}$ line is set high, the display length counter is reset to 0, and the $\overline{\text{AUXBLANK}}$ line is set high to unblank the crt beam.

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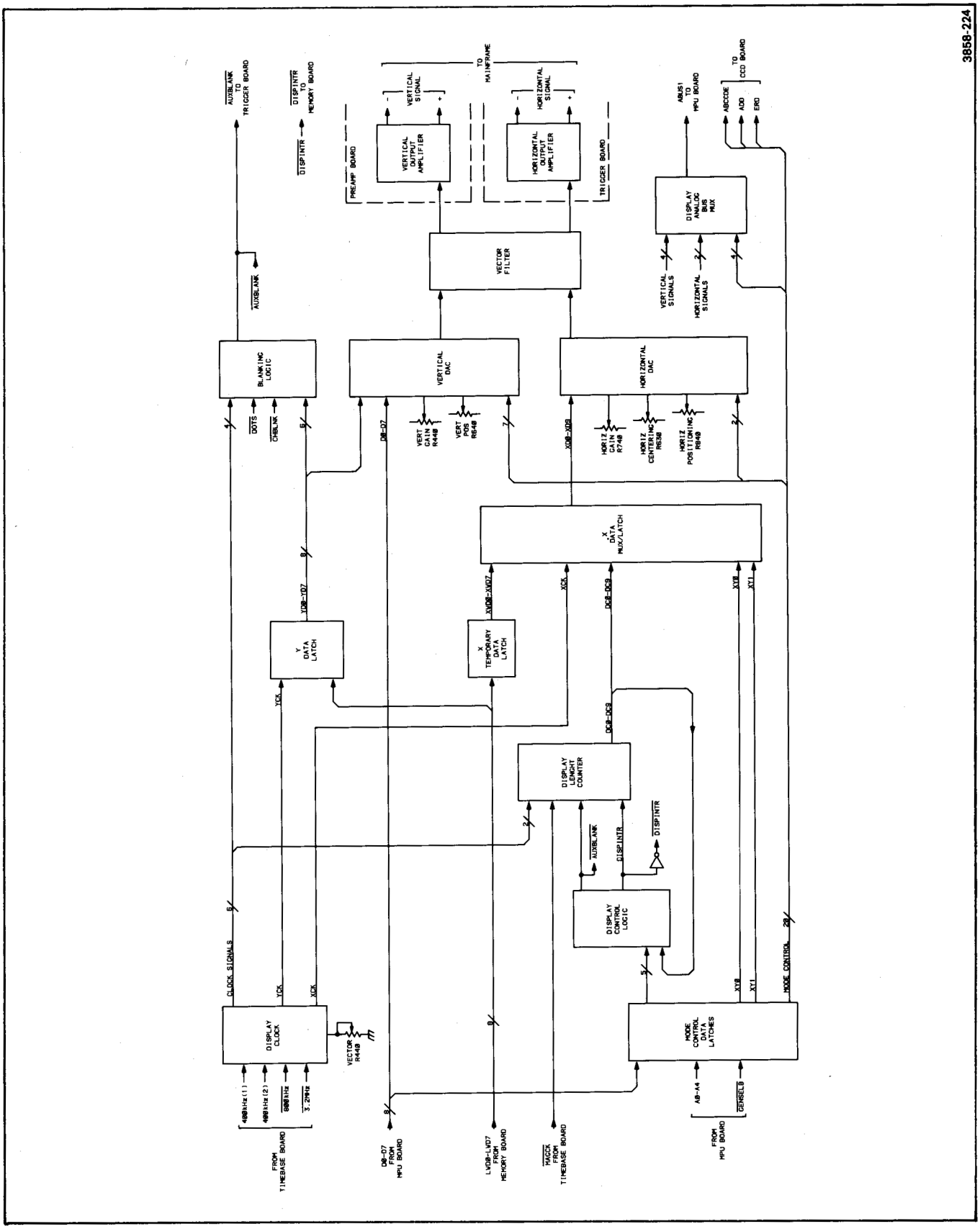

Figure 2-10. Detailed block diagram of display circuitry.

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DISPLAY CLOCK (Self Test 29)

The 400kHz(1), 400kHz(2), 800kHz, 3.2MHz and MAGCK signals from the Time Base board provide the basic timing information for the Display circuitry (see Fig. 2-11). In addition, U200A creates the 400kHz(4) and 400kHz(4) timing signals. Display clock multiplexer U310 selects one of four timing signals to drive the display length counter: MAGCK (X10 CLOCK), 800kHz (X2 CLOCK), 400kHz(4) (X1 CLOCK) and DISPLAY LENGTH COUNTER SINGLE STEP.

The 400kHz(2) signal provides the basic timing to latch the X-axis and Y-axis data to the DAC inputs. Transistor Q300 and single-shots U400A and U400B create an adjustable delay between the clock signal to pin 11 of U410 and the signal at pins 11 of U320, U520 and U620 to compensate for the delay line in the mainframe vertical amplifier. U400A produces a fixed delay of approximately 50 ns between the receipt of a low on the 400kHz(2) line and the output of a falling edge on the YCK line. U400B produces a rising edge on the XCK line. Q300 and the front-panel VECTOR adjustment (R640) allow the XCK edge to be delayed by between −25 ns and 200 ns with respect to the YCK edge. This adjustable delay compensates for the different delay line lengths of various mainframes. About 60 ns of delay occurs in the 7D20 vertical circuitry with respect to the horizontal circuitry. The adjustment is required to ensure straight vectors between data points.

DISPLAY CONTROL LOGIC (Self Test 28)

Gates U210 and U100C and flip-flops U500A and U500B control the starting and stopping of a display cycle. Prior to the beginning of a display cycle, END DISPLAY CYCLE and START DISPLAY CYCLE are both high. The resulting high on pin 8 of U500B holds the DISPINTR line low, which inhibits the display address generator (DAG) on the Memory board; the low on pin 9 of U500B holds AUXBLANK low, which blanks the crt beam.

When the microprocessor pulses START DISPLAY CYCLE low to begin the display cycle, DISPINTR and AUXBLANK are pulled high, which enables the DAG and unblanks the crt beam. The high on pin 9 and the low on the pin 8 outputs of U500B also enables the display length counter to begin counting from 0 (see the following discussion of the display length counter).

During display setup, the microprocessor sets the 820/1024 line for the number of data points to be displayed horizontally: 820 for the ERD time base mode;

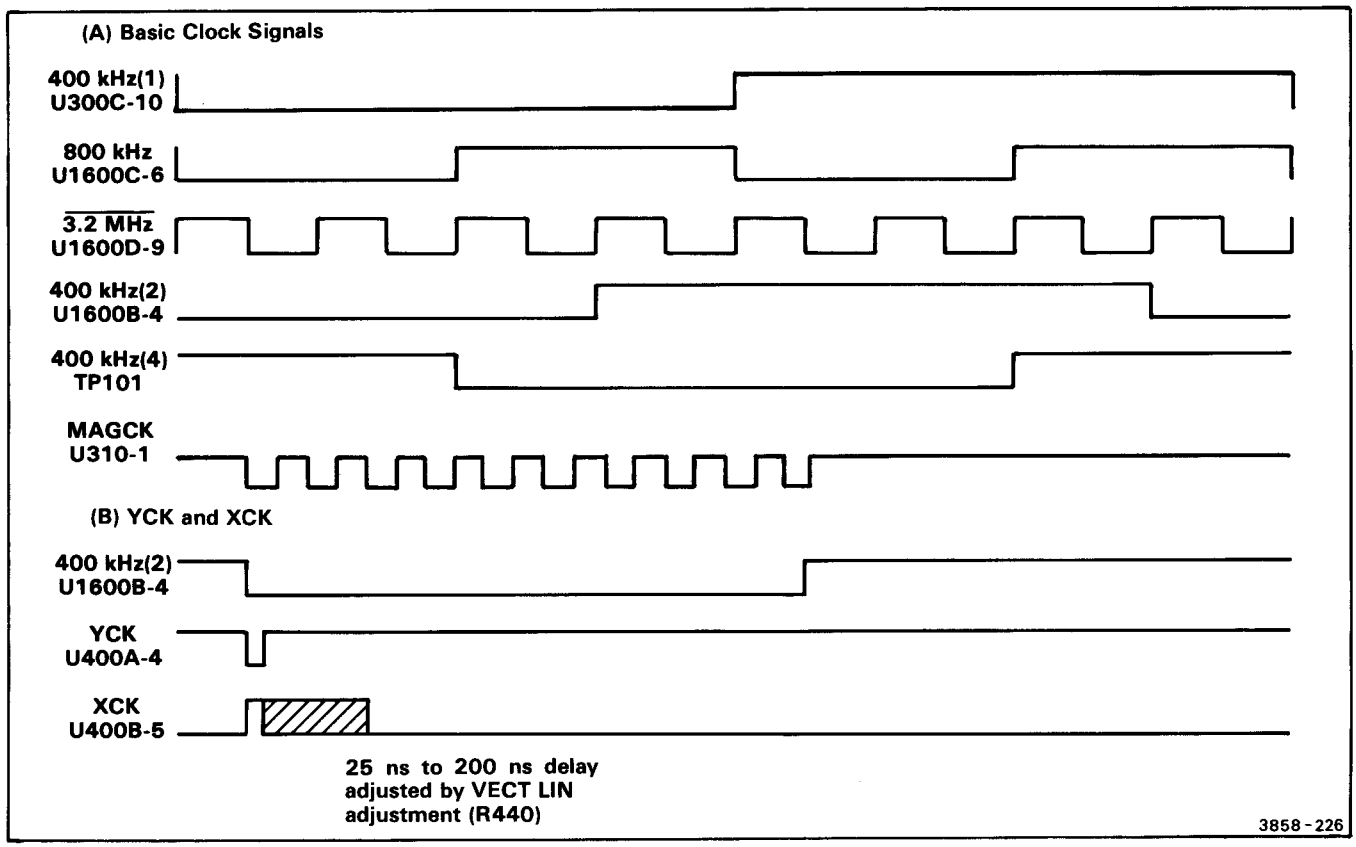

Figure 2-11. Display timing: (A) Basic Clock Signals; (B) YCK and XCK Signals.

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When DISPINTR is set high, the Memory circuitry begins transmitting waveform data from the WFM to the Display board via the latched waveform data lines (LWD0-LWD7). The Display circuitry transmits the Y-axis waveform data through latches U410 to the vertical DAC. It transmits either the X-axis data from the WFM or the horizontal ramp data from the display length counter through latches U320, U520 and U620 to the horizontal DAC.

The resulting vertical and horizontal analog signals are then transmitted to the mainframe vertical and horizontal display amplifiers for display on the mainframe crt.

When the display length counter reaches its maximum display length or when the microprocessor sets END DISPLAY CYCLE low through U1400, the DISPINTR line is set low, which halts the DAG on the Memory board and signals the microprocessor that the display cycle has ended. The low on the Q output of U500B at the end of the display cycle sets AUXBLANK low, which blanks the crt beam until the beginning of the next display cycle.

DISPLAY MODES

The same Display circuitry is used with slight modifications in setup data to create the four display modes: Y vs. time, X-Y, readout and cursor. In the Y vs. time mode, Y-axis waveform data from the WFM is transmitted through Y latch U410 to the vertical DAC. The display length counter then generates the X-axis data, which in this case is used to create the horizontal ramp signal. The X-axis data is transmitted through the X data multiplexer/latches (U320, U520 and U620) to the horizontal DAC. The display length counter and the X-data multiplexer/latch are clocked at the same rate as the DAG on the Memory board so that each increment of the X-axis ramp corresponds with a new Y-axis waveform point on the crt display.

The X-Y mode is similar to the Y vs. time mode, except that X-axis waveform data from the WFM is substituted for the X-axis ramp data. X-axis data is read from the WFM during a READ X time slot and stored temporarily in the X temporary latch (U420). Y-axis waveform data read during the READ Y time slot and the temporarily stored X-axis data are then latched simultaneously through Y latch U410 and X data multiplexer/latch U320, U520 and U620 to their respective DACs. The display cycle continues until the display length counter has reached its maximum (1024 or 820 counts). The resulting display is a plot of one waveform against another.

The readout mode is a variation of the X-Y mode. Readout data (characters and numbers) are stored in the WFM as a series of X-Y coordinates (matrix points). The character data is then read into the Display circuitry, latched and converted to analog data points during one display cycle, as in the X-Y mode.

The main difference between the readout mode and the X-Y mode is in the creation of eight blanking fields, each one data point wide, that extend horizontally across the crt screen. These blanking fields are spaced 64 vertical data points apart. When the Y-axis data for a waveform point falls in one of these fields, the crt beam is blanked for one dot time.

These blanking fields perform two functions. First, for readout displays that do not require 1024 data points, these blanking fields provide places to put data points so that they will not be displayed. A second function of these blanking fields is to ensure clear readout displays when moving the crt beam from the top of the crt screen to the bottom and vice versa. When moving the beam a large distance between data points, the beam is allowed to rest in a blanking field, near the next dot location to be written, for one dot time to allow the vertical amplifier to settle.

The cursor mode is again a variation of the X-Y mode. Once the microprocessor has determined the horizontal location of the cursor on the display, it writes a waveform in the WFM (the X-axis in one block of the WFM and the Y-axis in another block) composed only of the data points located at the cursor position. It then reads the coordinates for this cursor waveform continuously. Approximately 50 μs after the start of the cursor display cycle, the microprocessor sets the END DISPLAY CYCLE low through U1400 to end the display cycle early. A dot is thus repeatedly refreshed on the crt screen to create the intensified cursor on the waveform display. In the delta-time mode where two cursors are displayed, a display cycle is repeated for each cursor point.

DISPLAY-DIGITAL

MODE CONTROL DATA LATCHES

The mode control data latches (U600, U1300 and U1305) receives display setup data from the microprocessor via data lines D0-D7. A low on GENSELB and a high on A4 enable address decoder U1400 to decode address lines A0, A1 and A2. The decoded data then causes pins 14, 12 or 11 to be set low, latching data into U600, U1300 or U1305, respectively.

Address decoder U1400 also controls the START DISPLAY CYCLE, END DISPLAY CYCLE and DISPLAY LENGTH COUNTER SINGLE STEP lines. START DISPLAY CYCLE initiates the reading of waveform data from the WFM. END DISPLAY CYCLE allows the microprocessor to end a display cycle before the display length counter has reached its maximum count. DISPLAY LENGTH COUNTER SINGLE STEP is used to single step the display counter during self test.

The functions of the other display mode control lines are described as part of the description of the circuits in which they are used.

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and 1024 for the roll, RD, Readout and ETD modes. The 820/1024 line at pin 1 of U210 determines whether the display length counter is allowed to count to 820 or to 1024 before the display cycle is ended. When the display length counter reaches the selected maximum count, U210 and U100C clock U500A, which sets the D input of U500B low. On the next display clock at pin 11 of U500B, $\overline{\text{DISPINTR}}$ and $\overline{\text{AUXBLANK}}$ are pulled low and the display cycle is ended.

In the cursor mode, the microprocessor pulls $\overline{\text{END DISPLAY CYCLE}}$ low to end the display cycle. The low on $\overline{\text{END DISPLAY CYCLE}}$, also pulls $\overline{\text{DISPINTR}}$ and $\overline{\text{AUXBLANK}}$ low.

DISPLAY LENGTH COUNTER (Self Test 29)

Counters U120A, U120B, U220A and U220B count display clock cycles and apply the count to the display count lines (DC0-DC9). This count is then applied to the horizontal (X-axis) DAC to produce the horizontal ramp.

At the end of the display cycle, the display logic sets the $\overline{\text{Q}}$ and Q outputs of U500B to low and high, respectively. The resulting low on pin 15 of U220A and pin 14 of U220B, and the high on pin 2 of U120A and pin 12 of U120B, resets the counter to 0 and inhibits it from counting. When the display cycle is initiated ($\overline{\text{START DISPLAY CYCLE}}$ is set low), Q and $\overline{\text{Q}}$ of U500B are set high and low, respectively, which enables the counters to begin counting XCK pulses. It continues to count until it reaches its selected maximum count, or until the $\overline{\text{END DISPLAY CYCLE}}$ line is pulled low. The display logic then the resets the counter to 0 and holds off counting until the beginning of the next display cycle.

X TEMPORARY LATCH AND Y LATCH (Self Test 33)

Latches U420 and U410 latch data from the WFM via the latched data lines (LWD0-LWD7). U420 latches X-axis data read during a READ X Memory time slot; U410 latches Y-axis data read during a READ Y time slot. U420 thus provides temporary storage of X-axis data so that the Y-axis and X-axis data can be applied to the vertical and horizontal DACs at approximately the same time (see Fig. 2-12). YCK latches the Y-axis data onto the Y-data bus (YD0-YD7). A short time later (the delay being determined by the front-panel VECTOR adjustment) XCK latches the X-axis data from U420 through the X data multiplexer/latch (U320, U520 and U620) onto the X-data bus (XD0-XD7).

X DATA MULTIPLEXER/LATCH

Latches U320, U520 and U620 latch either X-axis data from U420 or display length count data from the display

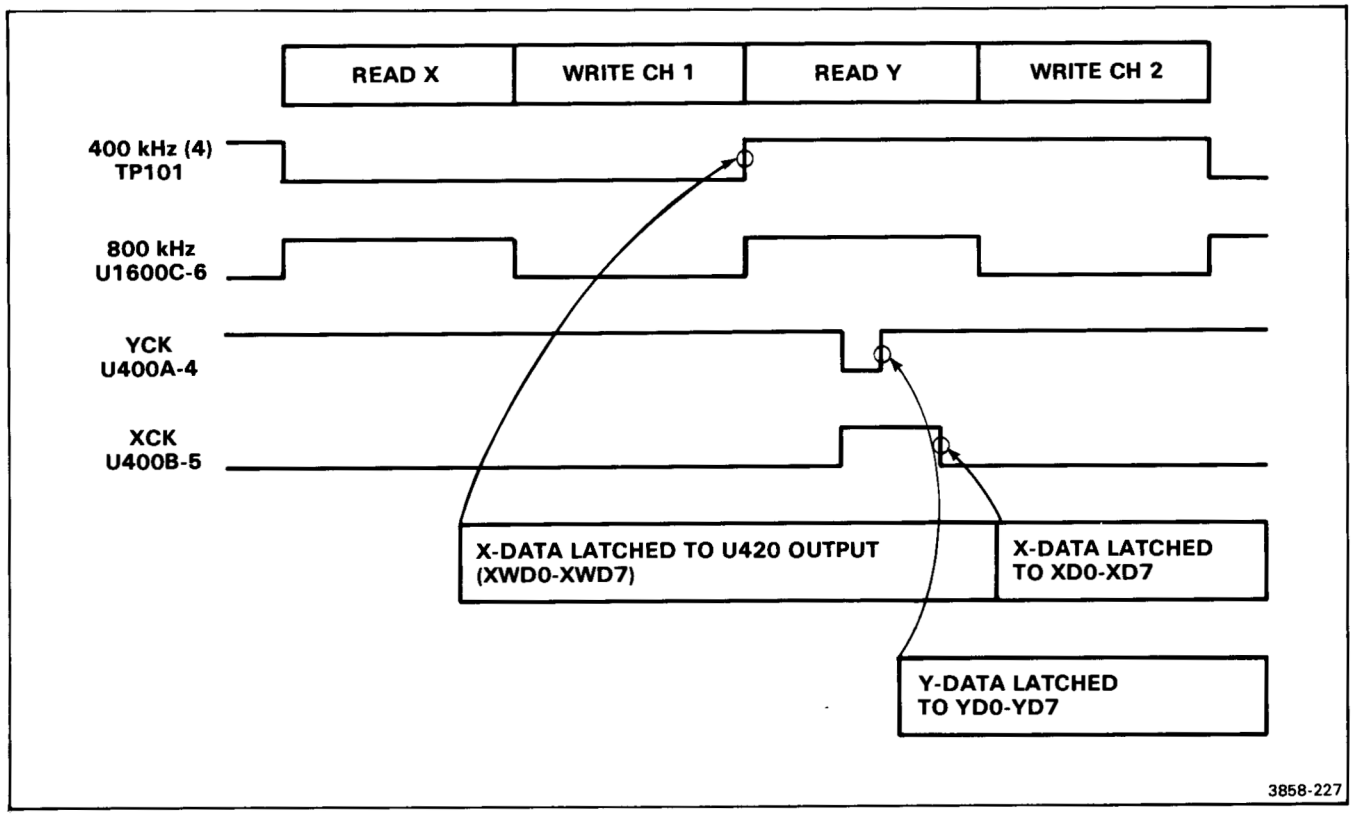

Figure 2-12. X-Data and Y-Data latch timing.

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length counter onto the X-data bus (XD0-XD9), depending on the display mode. In the Y vs. time mode, the display length count is latched onto the X-data bus; in the X-Y, readout and cursor modes, X-axis waveform data from the WFM is latched onto the X-data bus.

The X-axis data from the WFM is only 8-bits. In the cursor mode, these bits contain the eight most significant bits of the cursor X-axis location; the microprocessor provides the two least significant bits (XY0 and XY1).

BLANKING LOGIC (Self Test 38)

The blanking logic circuit has a number of modes of operation. U500B controls the $\overline{\text{AUXBLANK}}$ line at the start and end of each display cycle as described in the discussion of the display control logic.

During a display cycle, flip-flops U200B and U1500A control the blanking of the display. When the $\overline{\text{DOTS}}$ line is low (dots mode), the high at pin 12 of U1600F holds the $\overline{\text{Q}}$ output of U200B high. U1500A then controls the blanking of the crt beam (see Fig. 2-13). The output of U1500A at pin 6 is essentially the 400kHz(2) signal, inverted. The beam is thus blanking prior to the switching from one data point to the next and unblanked when the vertical and horizontal amplifiers have settled.

When the $\overline{\text{DOTS}}$ line is high (vector mode), the $\overline{\text{Q}}$ output of U1500A is held high and U200B controls the blanking of the crt beam. In this case, the beam is unblanked prior to the switching from one data point to the next and blanked again just prior to the display of the next data point. The unblanking of the beam during the transition from one dot and the next combined with the delay introduced by the vector filter (see the discussion of the vector filter circuit) causes a vector to be drawn on the crt screen between the two data points.

Gates U510 and U300B create the blanking fields during a readout display cycle. When the display is set up for a readout cycle, the character blanking ($\overline{\text{CHBLNK}}$) line is set low. A low at the output of U510 then causes $\overline{\text{AUXBLANK}}$ to be pulled low, blanking the crt beam. The six least significant Y-data bus bits control U510. When they are all high, pin 8 of U510 is pulled low, which occurs on every 64th Y-axis point.

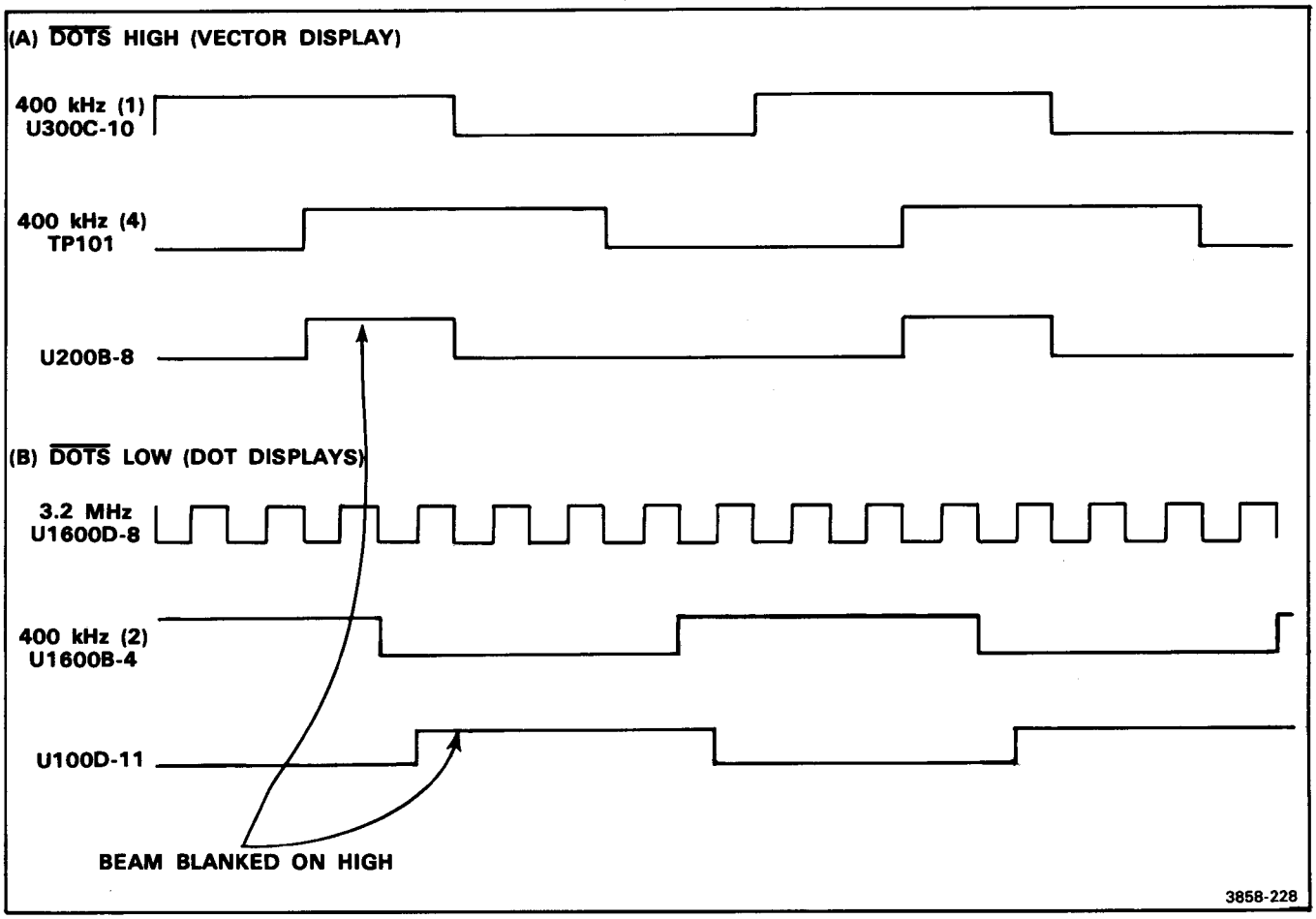

Figure 2-13. Crt Beam Blanking Timing: (A) Vector Mode; (B) Dots Mode.

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DISPLAY-ANALOG

HORIZONTAL D-TO-A CONVERTER (Self Test 30)

The horizontal DAC (U720) converts the data from the X-data bus (XD0-XD9) to an analog current at its pin 3 output that is proportional to its digital input. The Vref- and Vref+ inputs to the DAC (pins 16 and 15, respectively) establish the current gain of the DAC. The front-panel HORIZ GAIN adjustment (R740) allows the DAC current gain to be adjusted to the gain of the mainframe horizontal display amplifier.

The current input to Vref+ sets the overall reference current (or over all gain) of the DAC. R820 sets this reference current in the roll, RD and ETD time base modes, in which 1024 data points are displayed horizontally. In the ERD mode, in which 820 data points are displayed horizontally, the gain of the DAC is increased to provide a full screen display. When the microprocessor sets the 820 GAIN COMP line high, analog switch U1020 applies the BY input to its channel B output. The additional reference current that R916 conducts is thus applied to the Vref+ input to U720 to increase its current gain. When the 820 GAIN COMP line is low, CR916 conducts, clamping U1020 pin 1 to 1 V.

The DAC output current is applied to current-to-voltage converter U820. R822 sets the current-to-voltage conversion ratio. R821 introduces an offset current at the pin 2 input to U820 such that when the DAC output current is at midrange, the horizontal display signal is centered horizontally on the crt screen. The front-panel HORIZ CTR adjustment (R840) allows this offset current to be adjusted to align the display horizontally with the graticule lines during adjustment.

The front-panel HORIZ POSITION control (R630) provides horizontal positioning current to the null point of U820 through channel A of U1020. This control can be disabled under either of two conditions. When the microprocessor sets the HORIZ POS line low, CR1119 is turned on, which pulls the AY/X input to U1020 (pin 11) low and inhibits the horizontal position current from being conducted through U1020 to the null point of U820. Comparator U1325B performs a similar function. When the HORIZ POSITION control is turned fully clockwise to its detent position, the level at pin 5 of U1325B causes the anode of CR1322 to be pulled low, which sets pin 11 of U1020 low and inhibits the horizontal positioning current. CR920 prevents the analog switch from latching up when the AY input is not selected. The 0.5 V/division output signal from U820 is applied to the vector filter circuit.

VERTICAL D-TO-A CONVERTER (Self Tests 34 and 35)

The vertical display circuitry consists of a number of devices that not only convert the data from the Y-data bus (YD0-YD7) into an analog signal, but also allow the signal to be expanded or compressed, and offset. DAC U610 converts the Y-axis data into an analog current that is proportional to the digital input, in a manner similar to that described for the horizontal DAC circuit. This current is applied to current-to-voltage converter U800. R802 sets the current-to-voltage conversion ratio.

The front-panel VERT GAIN adjustment (R440) adjusts the Vref+ level, and allows the vertical DAC gain to be adjusted to that of the mainframe vertical display amplifier. The reference voltage for the Vref- input is applied to U610 through a divider (R711, and R911 through R915). Multiplexer U810 allows the reference voltage to be divided down in order to provide programmable attenuation of the full scale output current of U610, and thus provide programmable compression of the vertical display signal. The microprocessor controls the compression control lines (CA, CB and CC) to U810, which select the compression factor.

Offset DAC U700 converts digital offset data from the microprocessor data line (D0-D7) into an analog offset current. This current is also applied to current-to-voltage converter U800. DAC Gain Bal adjustment R900 adjusts the gain of U700 to match the gain of U610.

The front-panel VERT GAIN adjustment (R440) adjusts the Vref+ level to U610, the Vref- level to U700 and the reference voltage to the compression divider (R711 and R911 through R915). R440 thus adjusts the overall current gain of the vertical DAC, allowing it to be matched to that of the mainframe vertical amplifier.

Operational amplifier U905 introduces an offset current at pin 2 of U800, such that when the vertical signal DAC and the vertical offset DAC currents are at midrange, the vertical display signal is vertically centered on the crt screen. DAC Offset adjustment R1000 allows any current offset to be nulled out, preventing undesired display shift when expansion is used.

The output voltage of U800 is applied to a divider (R906, and R1200 through R1207). Expansion multiplexer U1100 selects taps on this divider. The unexpanded signal at pin 5 of U1100 has been attenuated by a factor of 5. By reducing the attenuation of the input signal, the output signal at pin 3 of U1100 is thus in effect expanded. In addition, the gain produced at pin 13 of the multiplexer is unique for use in displaying readout characters. The microprocessor controls the expansion control lines (EA, EB and EC), which select the expansion factor. Note that the expansion divider affects the vertical offset level as well as the vertical signal amplitude.

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The output of the expansion multiplexer at pin 3 of U1100 is applied to buffer amplifier U1010. Q1001 and Q1015 provide overvoltage protection for the amplifier by clipping the signal if it reaches an amplitude of greater than ±0.8 V peak-to-peak.

The vertical positioning current, which the front-panel VERT CTR adjustment (R540) controls, is also applied to buffer U1010 to compensate for the vertical offset of the mainframe vertical amplifier.

VECTOR FILTER (Self Tests 31 and 36)

The vector filter slows the changing of the analog vertical signal from one data point level to the next data point level, which causes the dots to appear to be connected.

There are two identical vector filters, one for the vertical signal (R1210, C1211, C1210 and L1210) and one for the horizontal signal (R1220, C1221, C1220 and L1220). Multiplexer U1215 selects either filtered (vector mode) or un-filtered (dots mode) operation. When the microprocessor sets the $\overline{\text{DOTS}}$ line high, the Y inputs to channels A and B of U1215 are selected, which allows the filtered signals to be applied to the output pins; when $\overline{\text{DOTS}}$ is low, the unfiltered signals, which are conducted through R1222 and R1120, are applied to the outputs.

Buffer amplifier U1315 and U1325A transmit the horizontal and vertical signals, respectively, to the display output amplifiers. There is a unity gain between the input to the vector filter and the output of each signal.

DISPLAY OUTPUT AMPLIFIERS (Self Tests 32 and 37)

The vertical and horizontal display signals from U1315 and U1325A, respectively, are applied to display output amplifiers on the Preamp Board (A4) and the Trigger Board (A10). Attenuators at the inputs to these amplifiers reduce the signal levels to approximately the levels that the respective mainframe display amplifiers require. They also provide noise filtering. The pair of operational amplifiers in each circuit (U230B and U230A, and U240A and U240B) convert the single-ended signals to differential signals for application to the mainframe. The (-) side of each signal is picked off through R255 and R220, respectively, for application to an analog multiplexer on the Preamp and Trigger board. These signals are then transmitted to the MPU board for use in self test.

DISPLAY ANALOG BUS MULTIPLEXER

Multiplexer U1510 picks off the vertical and horizontal signals at various stages of their development and transmits them to the MPU board via an analog bus (ABUS1) for use in self test. A low on the analog bus display enable ($\overline{\text{ABDISPE}}$) line enables U1510 to transmit the selected signal to ABUS1. The microprocessor controls the analog bus display select lines (ABDISPA, ABDISPB and ABDISPC), which select which display signal is transmitted to the MPU board.

10 POWER SUPPLY

The Power Supply circuitry is located on the Power Supply Board (A7). In addition, the Power Supply board (A7) houses drivers for the relays on the Ch 1 and Ch 2 Attenuator boards (A12 and A13).

POWER CONVERTER (Self Test 13)

The +5-VL and -5-V power converter is a fly-back circuit. Energy is stored in fly-back transformer T340 while fly-back transistor Q330 is on. When Q330 is turned off, the energy stored in the transformer is transferred to the secondaries, where it is filtered and regulated to create the +5-VL and -5-V supplies. The +5 V sense line is used to control the conduction time of Q330 and thus regulate the overall output voltage of the power converter.

Half-wave rectifier CR350 and its associated filter rectify and filter the +5 V secondary output to produce the +5 VL logic power supply.

Operational amplifier U310A forms a self-oscillating comparator circuit that drives the base of Q330 through Q220 and Q230. U310A senses the level of the +5 V supply through divider R412 and R411. It uses this voltage to set the duty cycle of the oscillator made up of R416 and C416, and the inverting side of U310A. When the power supply load is increased, Q330 is held on longer to supply additional current to the supply.

Comparator U310B monitors the current that Q330 conducts. When an overcurrent condition is encountered, it shuts the U310A oscillator down, holding Q330 off.

Snubber network R231, C231, CR230, C230 and VR230 ensure that the breakdown voltage of Q330 is not exceeded under overload or fault conditions.

The series pass regulator made up of U660A, U660B, Q660 and Q650 provide a precision -5 V supply for use with analog circuitry in the plug-in. The -5 V supply is referenced to the -15 V supply via divider R762 and R763. U660A then increases or decreases the drive to Q650 as required to maintain the -5 V output voltage. Comparator U660B senses the current that the -5 V supply conducts, and turns off Q650 when the current reaches the overcurrent limit.

SELECT LOGIC

The microprocessor supplies select data for the power supply monitor self test multiplexer and the attenuator

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relay drivers. Address decoder U840 decodes address line A5 to determine which of two latches (U710 and U711) is to receive the select data. A low level on the general select B line and the A4 line enable U840 to decode A5. A low on output Y2 of U840 causes the data on data bus lines D0-D4 to be latched into U710; a low on Y3 latches data into U711.

POWER SUPPLY MONITOR

A group of dividers (R611 through R618, and R620 through R623) pickoff a fraction of each power supply voltage level for application to multiplexer U610. The multiplexer transmits the selected level from a divider to the microprocessor via analog bus 1 (ABUS1) for use in self test. The microprocessor sets the select inputs to U610 (pins 9, 10 and 11) via U710 to select specific power supply levels. A low on pin 6 of U610 enables the selected input level to be transmitted to ABUS1.

ATTENUATOR RELAY DRIVERS

Buffer amplifier U741 and U640 drive relays on the Ch 1 and Ch 2 Attenuator boards (A12 and A13). The 16 relays are configured into a matrix that enables them to be selected with eight relay control lines (see Fig. 2-5 and Table 2-4). The microprocessor selects which relay lines are activated through select data applied to U741 and U640 from latch U711, and decoders U740A and U740B. Each gate in the buffer amplifier is connected both to a select line and to Q641. Q641 activates a temporary enable line.

The attenuator relays are permanent magnet latching relays, which require an enable pulse of only a short duration to cause them to switch. C811 and R724 determine the duration of this enable pulse.

11 MEMORY

The waveform memory (WFM) and memory control circuitry is located on the Memory board (A8). This circuitry controls the storing of waveforms and readout data in the waveform memory (WFM). It also controls the reading of these data from the WFM for display on a 7000-series mainframe crt and for processor control.

DETAILED BLOCK DIAGRAM DESCRIPTION

The waveform memory consists of 16 1K-byte (1024 bytes) blocks of dynamic RAM (see memory map in Fig. 2-14). Data to be written into the WFM comes either from the data bus (D0-D7) or the CCD analog-to-digital converter (AD0-AD7). The data multiplexer selects which data source is transmitted to the WFM. The selected data are then applied to the memory data bus and transmitted to the WFM and to the memory data self test latch.

The WFM can be addressed from one of three sources: address bus, acquire address generator (AAG) and display address generator (DAG). The microprocessor controls the 14 bit address bus (A0-A13). The AAG generates sequential addresses, which are used to direct the WFM where to store the waveform data that the CCD acquires. The DAG also generates sequential addresses, which are used to read waveform data from the WFM for display on the mainframe crt. Both of these address generators have a microprocessor programmable starting address.

The address multiplexer converts the addresses from the 14-bit addresses bus into the 7-bit row and column addresses that are required to access specific memory cells in the WFM. The display/acquire address multiplexer selects either the display addresses or acquire addresses. It combines these addresses with additional address information from the block register to create 7-bit row and column addresses. The 4-bit block address from the block register selects which 1K block of the 16K WRS the AAG or DAG is to access. These row and column addresses are transmitted both to the WFM and to the memory address self test latches.

Data read from the WFM are applied both to the display data latch and the WFM data latch. The data from the display data latch are transmitted to the Display circuitry for display on the crt. The data from the WFM data latch are output onto the microprocessor data bus (D0-D7).

In addition the memory write data and memory address self test latches allow the microprocessor to monitor the activity in the Memory circuitry.

The memory timing and synchronization, and the memory control circuits convert clock signals and control inputs from the time base and microprocessor circuitry into timing, synchronization and enable lines to control the sequencing of the Memory circuitry.

MEMORY READ/WRITE TIMING

The WFM completes one read/write cycle every 2.5 μs for a rate of 400 kHz. Each read/write cycle is divided into four time slots (see Fig. 2-15): READ X, WRITE CH 1, READ Y and WRITE CH 2. During the READ X time slot, a byte of data is read from the WFM to be displayed on the X-axis of the mainframe crt; during the READ Y time slot, a Y-axis data point is read. Note that although X-axis data are always read, it is used only when displaying waveforms in the X-Y mode.

Likewise, during the WRITE CH 1 time slot, a data point acquired from Channel 1 of the CCD circuitry is stored in the WFM, and during the WRITE CH 2 time slot a data point acquired from Channel 2 is stored

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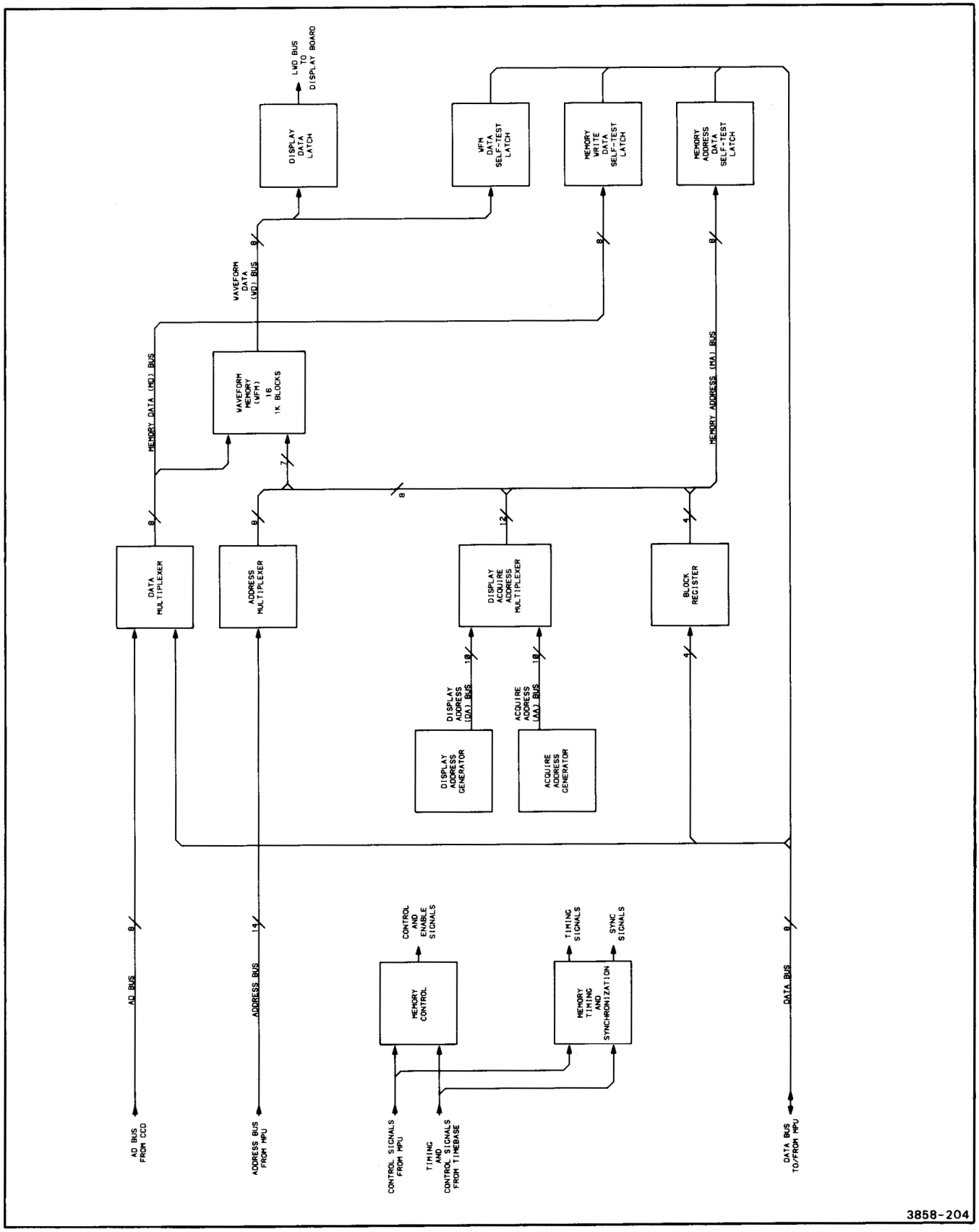

Figure 2-14. Detailed block diagram of Memory circuitry.

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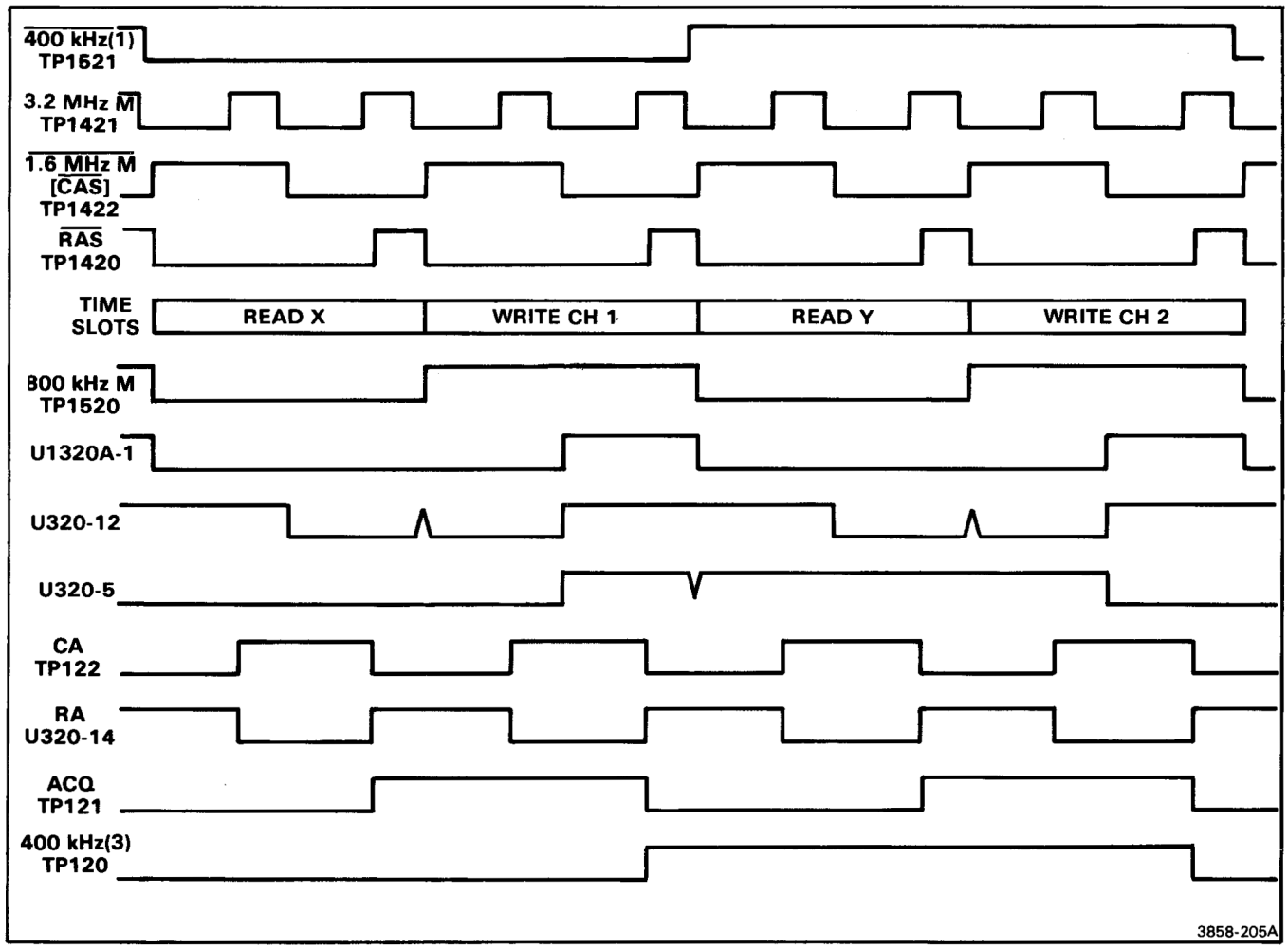

Figure 2-15. Memory timing signals.

During each of these time slots, a row and a column address is applied to the WFM's RAM devices, and data are then either read from or written into the selected cell. The Time Base circuitry generates the basic timing and synchronization signals that control this operation. The memory access cycle is tus synchronized with the CCD acquire cycle and the display cycle.

The microprocessor steals an occasional read or write time slot to gain access to the WFM. Firmware control of these accesses, however, ensures that they do not interfere with the writing of acquired data into the WFM or the reading of the waveform data for display.

DETAILED CIRCUIT DESCRIPTION

The detailed circuit description of the Memory circuitry is divided into four parts: waveform memory (WFM), memory timing, memory synchronization and memory control.

WAVEFORM MEMORY (WFM) (Self Tests 19 through 26)

The WFM is made up of eight 1 × 16K dynamic RAMs, which allow data to be read from or written into the WFM one byte at a time. Each device has a single data input port (pin 2) and a single data output port (pin 14). The 14-bit address required to address one byte of the WFM is divided into two 7-bit segments called a row address and a column address. These addresses are applied to the address lines (A0-A6) sequentially.

A falling edge on the row address strobe (RAS) input (pin 4) latches the row address on the address lines; a falling edge on the column address strobe ($\overline{1.6MHz}$) input (pin 15) latches the column address (on the same address lines) and the state of the read/write (R/$\overline{W}$) line. A high on the R/$\overline{W}$ line causes data to be read from the selected memory address; a low causes data to be written to the selected address.

During a read (or display) time slot, the acquire (ACQ) line is low and the R/$\overline{W}$ line is high (see Fig. 2-16). The next

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low on the $\overline{RAS}$ line latches the row address. The row address (RA) and column address (CA) lines then change state, switching the address multiplexer outputs from row to column addresses. A low on the $\overline{1.6MHzM}$ line then latches the column address. Then, 135 ns after the column address is latched, the data from the selected address are applied to the waveform data bus (WD0-WD7). The data remain on the bus until the $\overline{RAS}$ line again goes low. Prior to $\overline{RAS}$ going low, the $\overline{800kHz}$ line latches the data into display data latch U1510.

During a write (or acquire) time slot, the ACQ line is high and the R/$\overline{W}$ line is low. $\overline{RAS}$, RA, CA and $\overline{1.6MHz}$ timing is the same as for a read time slot. On the falling edge of the column address strobe ($\overline{1.6MHz}$), the data on the memory data bus is written into the waveform memory RAMs.

The microprocessor can access the WFM during either a display or an acquire time slot. The RAM access timing shown in Figure 2-16 is the same. The source of addresses and data, however, are changed. (See the description of waveform memory select under Memory Synchronization.)

Dynamic RAMs such as the 4116 RAMs used in the WFM require periodic access (termed refresh) to 128 sequential row addresses in order to retain the data stored in them. The reading of the WFM for display generally causes the memory devices to be refreshed automatically. If the microprocessor interrupts normal display cycles for a long period of time, however, it sets the REFRESH line (pin 9 of U1220) high to initiate the refresh mode. The high on REFRESH overrides the interrupt to the DAG, allowing it to run continuously (see the discussion of the display address generator).

The refresh line is set high at the end of each display cycle to ensure no data is lost if the μp is busy and exceeds the refresh interval before starting the next display. Some conbinations of display cycles do not guarantee refresh, which this refresh interval overcomes.

Refresh is set low before initializing the DAC for the next display cycles.

MEMORY TIMING

The $\overline{3.2MHz}$, $\overline{1.6MHz}$, $\overline{800kHz}$ and 400kHz(1) signals from the Time Base board supply the basic timing information for the Memory circuitry (see Fig. 2-15). The 3.2MHz and $\overline{1.6MHz}$ signals are applied to inverter U1520E, inverter U1420D and gate U1320D to create the 3.2MHzM, $\overline{1.6MHzM}$ and row address select ($\overline{RAS}$) signals.

The $\overline{800kHz}$ signal is used unbuffered to gate data from the display data latch (U1510) onto the latched waveform data bus (LWD0-LWD7). The use of the $\overline{800kHz}$ signal prevents a race condition from occurring when the low on the $\overline{1.6MHz}$ line causes the outputs of the waveform memory RAMs to be tri-stated.

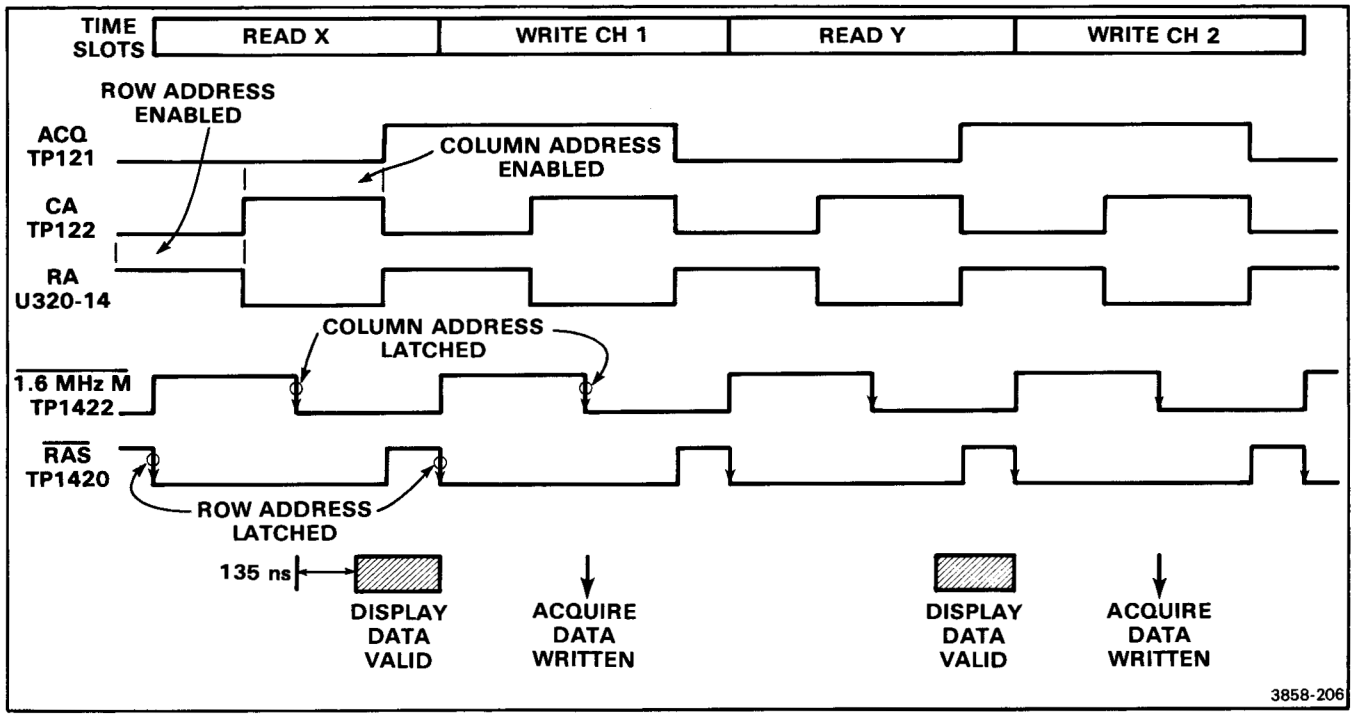

Figure 2-16. Waveform memory RAM access timing.

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For all other Memory board applications, inverters U1520A and U1520C, and gates U1320A and U1420C buffer the $\overline{800kHz}$ and 400kHz signals.

Quad D-Type flip-flop U320 gates these signals through flip-flop sections 2, 3 and 4 to create additional special purpose timing signals: CA, RA, ACQ and 400kHz(3). Figure 2-15 shows the input and output timing relationship of these signals.

MEMORY SYNCHRONIZATION

The general select A ($\overline{GENSELA}$) and waveform memory select ($\overline{WMEMSEL}$) lines from the microprocessor and the acquire waveform clock (AWCK) line from the Time Base are used to synchronize the Microprocessor and Time Base circuitry with the Memory circuitry.

The microprocessor runs asynchronous to the system (Time Base) clock for maximum speed of instruction execution. In order to access the WFM, the microprocessor read and write signals must be synchronized with the WFM time slots to avoid scrambled addresses and possible unwanted modification of WFM data.

$\overline{GENSELA}$ is a decoded range of the microprocessor memory map, which is used in combination with some of the lower address lines to select Memory functions. Flip-flop 1 of U320 and U620B synchronize $\overline{GENSELA}$ with the memory timing signals. When $\overline{GENSELA}$ goes low (see Fig. 2-17), the $\overline{GSA}$ line (pin 4 of U620B) is pulled low on the next positive- going transition of 3.2MHzM. ($\overline{GSA}$ is the synchronized version of $\overline{GENSELA}$.) When $\overline{GENSELA}$ goes high again, $\overline{GSA}$ follows one gate delay later. The positive-going edge of $\overline{GSA}$ is purposely not synchronized with the 3.2MHzM signal to ensure that unwanted control data is not written to the Memory control circuitry after the select has been removed, which might occur if the circuitry had to wait for the next 3.2MHzM transition before $\overline{GSA}$ was raised.

AWCK from the Time Base indicates to the Memory circuitry that a digitized sample is available to be written into the WFM. Flip-flop U820B synchronizes the AWCK signal with the Memory circuitry to produce the acquire waveform (AW) signal.

WAVEFORM MEMORY SELECT (Self Test 18)

$\overline{WMEMSEL}$ indicates to the Memory circuitry that the microprocessor awaits access to the WFM. Flip-flops U720A and U820A and associated gates synchronize $\overline{WMEMSEL}$ signal with the available WFM time slots to produce the waveform memory select (WMS) signal.

When the processor wishes access to the WFM, it pulls the $\overline{WMEMSEL}$ line low (see Fig. 2-18). The 800kHzM and PRWS lines then determine whether the processor will access the memory during a read or a write time slot. A high on the PRWS line selects the read time slot for processor access; a low selects the write time slot. When PRWS is low, the 800kHzM signal is transmitted through U1420B unchanged; when PRWS is high, the 800kHzM signal is complemented.

For example, when PRWS is low and $\overline{WMEMSEL}$ is high, pin 6 of U720A is low, pin 5 of U820A is high, and pin 6 of U820A is low. When the processor pulls $\overline{WMEMSEL}$ low, U820A latches the low on the D input on the next leading edge of RA. (Since the J input to U720A is low at this time, its pin 6 output is unaffected by RA.) The RA signal clocks U820A until a low on the D input causes its outputs to switch and activate the WMS and $\overline{WMS}$ lines. The phase of the 800kHzM line thus determines whether WMS and $\overline{WMS}$ are activated during a read time slot or a write time slot.

When the WMS line goes high, the J input to U720A is pulled high. On the next leading edge of RA, the D input to U820A is high as a result of pin 6 of U720A changing state. The WMS and $\overline{WMS}$ lines are then deactivated on the next RA leading edge. When the $\overline{WMEMSEL}$ line goes high, U720A is returned to its quiescent state and U820A remains in its last state.

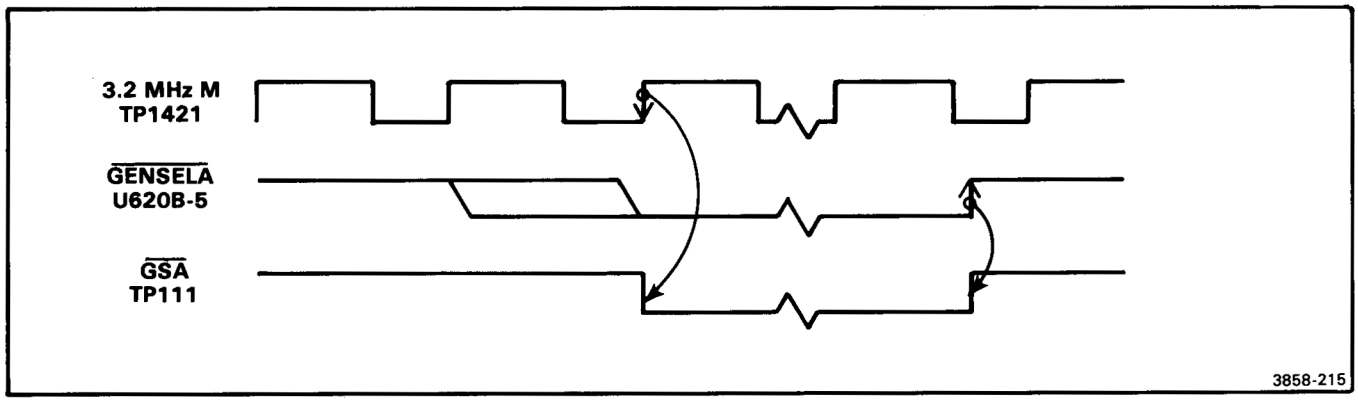

Figure 2-17. GENSELA and GSA signal synchronization.

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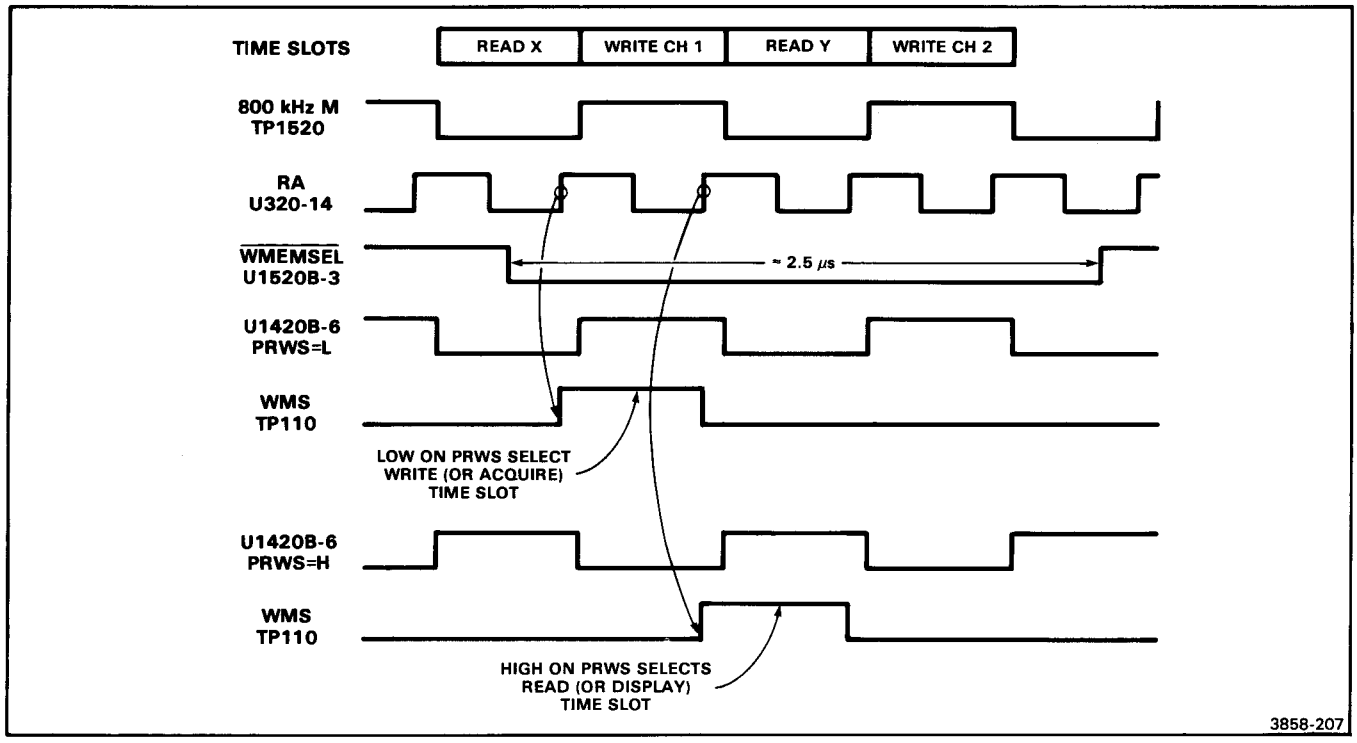

Figure 2-18. WMEMSEL timing and synchronization.

MEMORY CONTROL

GENSELA, write/read (W/R), display interrupt (DISPINTR) and various address lines from the microprocessor, and AWCK and end acquire (ENDACQ) from the Time Base circuitry provide control and setup information for the memory timing circuitry.

Four wide AND-OR gate U220 combines the 800 kHzM, AW, ENDACQ, W/R, CA and waveform memory select (WMS) signals to create the read/write (R/W) signal. The R/W signal determines whether data is read from the WFM or written into it. The gate at pins 11, 9 and 10 of U220 control R/W for memory access from the Time Base; the gate at pins 3, 4 and 5 control R/W for access from the microprocessor.

Assume that WMS is low, which is the case when the normal WFM read/write cycles are occurring without interruption from the microprocessor. If AW is high, indicating that acquired data from the CCD circuitry is to be written into the WFM, the 800kHzM line then toggles the R/W line: high during a read time slot and low during a write (or acquire) time slot. When AW is low (no acquire data present), the R/W line remains high (read). Note that a low on the ENDACQ line blocks the AW signal, inhibiting writes.

When the microprocessor wishes access to the WFM, the WMS line is pulled high (see discussion of memory synchronization), which enables the gate at pins 3, 4 and 5 of U220. The CA line then gates the W/R line through to the pin 6 output of U220. The microprocessor controls the W/R line; the WMS signal, however, synchronizes the W/R line with the WFM read and write time slots.

Decoder/Demultiplexer U420 and 8-bit addressable latch U1220 allow the microprocessor to activate special memory functions such as loading the DAG and AAG start addresses, single stepping the DAG and AAG, or initiating a refresh cycle. They also allow the microprocessor to cause selected data or addresses to be written to the self test latches, where it can then read the data or addresses without interrupting the normal WFM read/write cycle.

Decoder/Demultiplexer U420 decodes address line A5 and A6, and W/R to select the read memory address (RMA), read memory data (RMD), acquire address generator single step (AAGSS), display address generator single step (DAGSS), display start address (DSA), acquire start address (ASA), BLOCK and U1220 enable (pin 10) lines. (The application of these lines is discussed in the following description of the Memory circuits.)

Address line A4 and the GSA line control U420; a low on these two lines causes the output line that A5, A6 and W/R have selected to be pulled low. U420 does not latch the output; the selected line stays low only for the duration of the low at pin 4.

The outputs of U1220 are latched. When U420 pulls the pin 14 enable input to U1220 low, the bit that A0, A1 and

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A2 have selected is set to the logic state at D0. U1220 controls the display address generator single step enable ($\overline{\text{DAGSSE}}$), acquire address generator single step enable ($\overline{\text{AAGSSE}}$), processor read write select (PRWS) and REFRESH lines, and the four latch data lines, LA, LB, LC and LD. Data remains latched on these outputs until the processor modifies it.

Four-bit magnitude comparator U1120 compares the levels set on the latch data lines (LA, LB, LC and LD) with the states of 400 kHz (3), ACQ, RA and WMS. If all the respective A and B inputs are the same when the A=B input to U1120 at pin 3 is pulled high, the LATCK line (pin 6) is pulled high. U1120 is essentially a word recognizer. By setting the latch data lines for a specific combination, the processor can latch specific addresses or data into the self test latches, U200 and U300.

Table 2-8 shows the data latched into U200 and U300, depending on the state of LA, LB, LC, LD, and PRWS. (Not Clocked indicates that the data latched into U200 or U300 prior to LATCK going high is not changed.) Note that LC determines whether U200 latches row or column addresses and LD determines whether the microprocessor address or the AAG/DAG multiplexer addresses are latched. Both the MA and MD bus states are latched at the same time. The microprocessor asserts $\overline{\text{RMA}}$ or $\overline{\text{RMD}}$ to read U200 or U300, respectively. To prevent LATCK from being activated and changing the latched data while the microprocessor read is taking place, $\overline{\text{GENSELA}}$ is used to disable LATCK, via the A=B input, and U320 and U1320C. Flip-flop 1 of U320 synchronizes the $\overline{\text{GENSELA}}$ line to 3.2 MHz so that gate U1320C produces no glitches that could produce a LATCK pulse.

SELF TEST LATCHES (Self Test 14)

Memory address self-test latch U200 latches the memory address applied to the WFM address inputs. When the latch clock (LATCK) line goes high, the address on the memory address bus (MA0-MA7) is latched into U200. When the read memory address ($\overline{\text{RMA}}$) line is pulled low, the address is output onto the data bus (D0-D7).

(Self Test 17)

Memory write data self-test latch U300 operates in the same manner as U200. When LATCK goes high, the memory write data lines (MD0-MD7) are latched into U300. When the read memory data ($\overline{\text{RMD}}$) line is pulled low, the data is output onto the data bus.

DISPLAY ADDRESS GENERATOR (Self Tests 15 and 16)

The Display Address Generator (DAG) consists of three synchronous up/down counters, U500, U600 and U700.

TABLE 2-8
LATCK Timing

LD U1120-1	LC U1120-14	LB U1120-11	LA U1120-9	PRWS U1420B-5	Data Latched During Selected Time Interval	
					U200	U300
0	0	0	0	X	Not Clocked	Not Clocked
0	0	0	1	1	MPU COL	MPU Written Data
0	0	1	0	X	Not Clocked	Not Clocked
0	0	1	1	0	MPU COL	MPU Written Data
0	1	0	0	X	Not Clocked	Not Clocked
0	1	0	1	1	MPU ROW	Not Defined
0	1	1	0	X	Not Clocked	Not Clocked
0	1	1	1	0	MPU ROW	Not Defined
1	0	0	0	X	X COL	CH 2 Data
1	0	0	1	X	Y COL	CH 1 Data
1	0	1	0	X	CH 1 COL	CH 1 Data
1	0	1	1	X	CH 2 COL	CH 2 Data
1	1	0	0	X	X ROW	CH 2 Data
1	1	0	1	X	Y ROW	CH 1 Data
1	1	1	0	X	CH 1 ROW	CH 2 Data
1	1	1	1	X	CH 2 ROW	CH 1 Data

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The up/down mode control (pin 5) on each device is wired to ground, so the DAG always operates in the count-up mode. The data inputs at pins 15, 1, 10 and 9 of each counter are used to load a starting address in the device. The data outputs at pins 3, 2, 6 and 7 of each counter apply the address bits to the display/acquire multiplexers.

When the display interrupt (DISPINTR) line is pulled low, the counter enable input (pin 4 of U700) is pulled high (except when REFRESH is high), disabling the counters. The counters may then be loaded with a new starting address. The display starting address (DSA) line and address bit A0 control the loading of a starting address. This address loading operation is carried out in two steps. On the first step, the microprocessor causes both DSA and A0 to be pulled low, which activates the pin 11 LOAD inputs on all three address counters. The two most significant bits of the starting address are then read into the DA and DB inputs of U500 from the data bus (D0 and D1). (Data is also read into U600 and U700 during this step, but this data is written over on the next load step.) At the end of the microprocessor cycle, DSA is pulled high, disabling the load function.

A number of CPU cycles later, the DSA line is pulled low, but A0 remains high. Thus on this second load step, only U600 and U700 are enabled for an address load. The lower eight bits of the starting address are then loaded into U600 and U700, completing the load of the starting address.

When the microprocessor has completed loading a starting address in the DAG, it signals the Display circuitry, which in turn raises the display interrupt (DISPINTR) line and allows the counters to begin counting.

The three counters are connected as a ripple counter, with the carry bit at pin 13 enabling the next counter in series for one count. The three counters create a 10 bit address that allows addressing of 1024 sequential locations in the WFM.

A positive-going edge on the pin 14 clock input to each counter device clocks the device one count. Two clock modes are provided: continuous and single step. In the continuous mode, the 400kHz(3) clock signal clocks the counters once every 2.5 μs, just before the beginning of the READ X time slot (see Fig. 2-15). In the single step mode, the display address generator singlestep enable (DAGSSE) line is pulled low, which blocks the 400kHz(3) clock from being applied to the counter devices. The display address generator single step (DAGSS) line then controls the clock inputs to the counter devices, allowing the microprocessor to single-step the counters.

ACQUIRE ADDRESS GENERATOR (Self Test 40)

The Acquire Address Generator (AAG), U900, U1000 and U1100, operates almost identically to the Display Address Generator. The pin 4 enable input to U900 is wired to ground, causing the circuit to be permanently enabled. The state of the pin 14 clock inputs to the counter devices thus determines when the counter is incremented. The acquire address generator single step enable (AAGSSE), acquire address generator single step (AAGSS), 400kHz(3), and AWCK lines control these clock inputs.

The AAG also has two operating modes: continuous and single step. In the continuous mode, AAGSSE and AAGSS are both high. AWCK and 400kHz(3) then control the clocking of the counter devices. The Time Base circuitry creates the AWCK signal (see diagram 14). AWCK is coincident with the 400kHz(2) signal, but is enabled only when data is to be read from the CCD. It is also synchronized with the phase clock signals, which provide the timing information for the CCD circuitry. A high on both AWCK and 400kHz(3), which occurs on the rising edge of 400kHz(3), causes a positive edge to be applied to the clock inputs to U900, U1100 and U1000, clocking the counter one count.

When the counter reaches 1024, the memory end acquire (MEA) line is raised. MEA is applied to the Time Base circuitry through P410 pin 30A for use in the ERD and ETD time base modes. When MEA goes high, it causes the end acquire (ENDACQ) line to go low, which in turn disables the AWCK signal. The ENDACQ signal is also transmitted back to the memory board through P410 pin 30B. It is transmitted through multiplexer U1110 and applied to memory address self-test latch U200. The microprocessor monitors U200 to find out when the waveform acquisition cycle has been completed.

Data inputs to U900, U1000 and U1100 allow the microprocessor to set the starting address at which acquired data is to be stored. When the acquire starting address (ASA) line is low, the data on the data bus (D0-D7) is applied to the counters. Only the seven most significant bits of the starting address can be set. The three least significant bits are automatically set high.

In the single step mode, AAGSSE is low, which disables U1020B. The microprocessor then controls the clocking of the AAG through the AAGSS line.

DISPLAY/ACQUIRE ADDRESS MULTIPLEXER

The display/acquire address multiplexer, U1210, U1110 and U1010, multiplexes the display addresses from the DAG and the acquire addresses from the AAG onto the

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memory address bus (MA0-MA6). The display address bus (DA0-DA9) is applied to channel A of the multiplexers and the acquire address bus (AA0-AA9) is applied to channel B. The acquire (ACQ) line determines which channel of the multiplexer is enabled. When ACQ is high, acquire addresses are output to the memory address bus; when ACQ is low, display addresses are output.

U1210 and U1110 multiplex the row address (the seven least significant bits of either the display address bus or the acquire address bus). U1010 multiplexes the three least significant bits of the column address; the processor supplies the four most significant bits through the block register, U800.

The $\overline{\text{WMS}}$, RA and CA lines determine which of the multiplexers are enabled through gates U920D and U920A. When $\overline{\text{WMS}}$ is low, none of the multiplexer devices are enabled. Memory address in this case come from U1410 and U1310. When $\overline{\text{WMS}}$ is high, the RA and CA line select which addresses are applied to the memory address bus. A high on RA enables the U1210 and U1110 outputs; a high on CA enables the U1010 outputs and the block register (U800). Since RA and CA are complementary, the row and column addresses are always output onto the memory address bus sequentially.

Section four of U1110 multiplexes the $\overline{\text{DISPINTR}}$ and $\overline{\text{ENDACQ}}$ lines onto the memory address bus; section four of U1010 multiplexes the AW and MEA lines. These lines do not go to the RAM; instead, the microprocessor monitors them through memory address self-test latch U200.

BLOCK REGISTER (Self Test 27)

The block register, U800, supplies the four most significant bits of the column address, which in turn selects which of the 1K sections of WFM is read from or written to. U800 is a 4 × 4 register file. It is organized into 4-bit words. Separate address and enable lines are used to access the register for a read (pins 4, 5 and 11) or for a write (pins 13, 14 and 12).

The $\overline{\text{BLOCK}}$ line enables U800 to write address data from data bus lines (D0-D3). When $\overline{\text{BLOCK}}$ is low, A0 and A1 select into which register the address data is written.

The $\overline{\text{WMS}}$ and CA lines enable U800 to output address data to the memory data bus (MA3-MA6). When both $\overline{\text{WMS}}$ and CA are high, the read mode of U800 is selected. The 400kHz(3) and ACQ lines then select which register is read. Each register is assigned a specific time slot (see Table 2-9). Then 400kHz(3) and ACQ select these registers in the sequence that the WFM is read from and written to: READ X, WRITE CH 1, READ Y and WRITE CH 2 (see Fig. 2-15).

TABLE 2-9
Block Register Address Assignments

A0 400kHz(3) U800-5	A1 ACQ U800-4	Memory Read/ Write Frame
0	0	READ Y
0	1	WRITE CH 1
1	0	READ X
1	1	WRITE CH 2

DISPLAY OUTPUT LATCH (Self Test 33)

Display output latch U1510 transmits data from the WFM to the display board for display on the mainframe crt. The pin 1 enable of U1510 is tied to ground. Each time the $\overline{\text{800kHz}}$ line goes high, the data on the waveform data bus (WD0-WD7) is clocked to the output lines (LWD0-LWD7) and applied to J410 pins 26A-29A and pins 26B-29B.

WAVEFORM DATA LATCH

When the waveform memory select ($\overline{\text{WMS}}$) line goes high, the data on the waveform data bus is latched into U400. If the microprocessor has accessed the WFM for a read, $\overline{\text{WMEMSEL}}$ and W/$\overline{\text{R}}$ enable the outputs of U400, causing the latched data to be output onto the microprocessor data bus (D0-D7). The microprocessor then reads the data just before $\overline{\text{WMEMSEL}}$ goes high.

MICROPROCESSOR ADDRESS MULTIPLEXER (Self Test 14)

The microprocessor address multiplexer, U1410 and U1310, converts the 14-bit addresses from the address bus (A0-A13) into 7-bit row addresses and 7-bit column addresses. U1410 and U1310 are 4-bit multiplexers. Each multiplexer section has two input channels (A and B) and one output channel (Y). The channel select input at pin 1 selects which of the input channels is fed through to the output: low selects channel A; high selects channel B.

When the waveform memory select ($\overline{\text{WMS}}$) line is low, indicating that the microprocessor wishes to read from or write to the WFM, the pin 15 output enable input is activated, enabling the selected input channel to be fed through to the output. At the same time, WMS disables the display/acquire multiplexer via gates U920A and U920B.

The row address consists of the seven least significant bits (A0-A6) of the address; the column address is the seven most significant bits (A7-A13). The row addresses are thus applied to the A channels of the multiplexer devices and the column addresses are applied to the B channels. The CA line controls the channel select input:

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when CA is low, the row address is applied to the memory address bus (MA0-MA7); and when CA is high, the column address is applied to the bus. The CA transitions precede the $\overline{RAS}$ and $\overline{CAS}$ transitions, respectively, by approximately 125 ns, to ensure that the addresses are present when the read row address or read column address is initiated.

The read/write (R/$\overline{W}$) line is multiplexed through section 4 of U1310 to the MA7 line. The processor then monitors the activity of R/$\overline{W}$ through memory address self-test latch U200.

DATA MULTIPLEXER (Self Test 17)

The data multiplexer, U1600 and U1700, multiplexes the microprocessor data bus (D0-D7) and the CCD A-to-D converter output (AD0-AD7) onto the memory data bus (MD0-MD7). U1600 and U1700 operate almost identically to the microprocessor address multiplexer, U1410 and U1310. In this case, AD0-AD7 are applied to channel A and D0-D7 are applied to channel B. The $\overline{WMS}$ line determines which input channel is applied to the output Since the pin 15 enable input is wired to ground, one channel is always being fed to the WFM.

12 MPU CONTROL

The Microprocessor circuitry is located on the MPU board (A9). It consists of a microprocessor, a number of memory devices, hardware ports, A-to-D and D-to-A converters and diagnostics circuitry.

MICROPROCESSOR

The microprocessor (U910) has an 8-bit data bus (D0-D7) and a 16-bit address bus (A0-A15), and can address up to 64K bytes of memory space. Crystal Y825 clocks U910 at 6.25 MHz. Internally, the microprocessor divides this clock by 4 to create a 1.5625 MHz machine cycle rate.

The R/$\overline{W}$ output (pin 32) determines whether the microprocessor reads or writes data. The Q and E outputs (pins 35 and 34) control the sequencing of the addresses and data on the address and data buses (see Fig. 2-19).

The microprocessor has three interrupt inputs, the priority of which is shown in Table 2-10.

TABLE 2-10
U910 Interrupt Priority

Priority	Interrupt Inputs	Function
1	NMI	Power down interrupt
2	FIRQ	Display interrupt
3	IRQ	GPIB request interrupt

The non-maskable interrupt (NMI) is used to interrupt the microprocessor for a power down. When the power to the plug-in is switched off, the Power Supply sets the power down ($\overline{PWRDN}$) line low. (See the description of the EAROM circuit for further explanation of the use of this interrupt.)

The fast-interrupt request (FIRQ) input is used to indicate to the microprocessor that a display cycle has been completed. A low on the display interrupt ($\overline{DISPINTR}$) line from the Display board activates this interrupt.

The interrupt request (IRQ) input is used to indicate to the microprocessor that the GPIB interface device (U720 on the LED Board) is requesting service. A low on the $\overline{GPIBINT}$ line activates this interrupt.

The microprocessor RESET input is used only on power up. Capacitor C924 holds the RESET input low for approximately one second during power on to reset the microprocessor. It also holds the clear (CLR) line low for this time period.

The DMA/BREQ and HALT inputs to U910 are not used.

The memory ready (MRDY) input is used to stretch the E signal's active time, which in turn extends the microprocessor's write and data access time. This feature is used when the microprocessor is accessing hardware ports and the waveform memory (WFM) on the Memory board. (See the description of the memory ready logic for further discussion of the use of this input.)

MEMORY READY LOGIC

Gates U810C, U815B, U815A and U815C, and single-shots U825B and U825A control the MRDY input to the microprocessor (see Fig. 2-20). They also produce a number of enable and select signals, which are used to enable the hardware ports and communicate with the Memory board.

When the microprocessor requires access to the WFM, it sets the memory waveform memory (MWFM) line high. The high on MWFM at pin 9 of U810C sets the waveform memory select ($\overline{WMEMSEL}$) line low. This line is applied to the Memory board, where it indicates to the memory that the microprocessor requires access to the WFM for a read or a write. The low on the $\overline{WMEMSEL}$ line is transmitted through U815B. The resulting high on pin 6 of U815B triggers U825B, which in turn sets the MRDY input to U910 low for approximately 3 μs. The data on the microprocessor thus remains valid for this time, giving the Memory board time to fit the requested access into one of its four read and write time slots. At the end of this hold-off time, the MRDY line goes high. The microprocessor then completes its current machine cycle and continues with the next.

A high on pin 6 of U815B also sets the latch enable (LATEN) line high, which latches the address on the address bus into U915 and U925 (see the description of the address latches for further explanation of the function of LATEN.)

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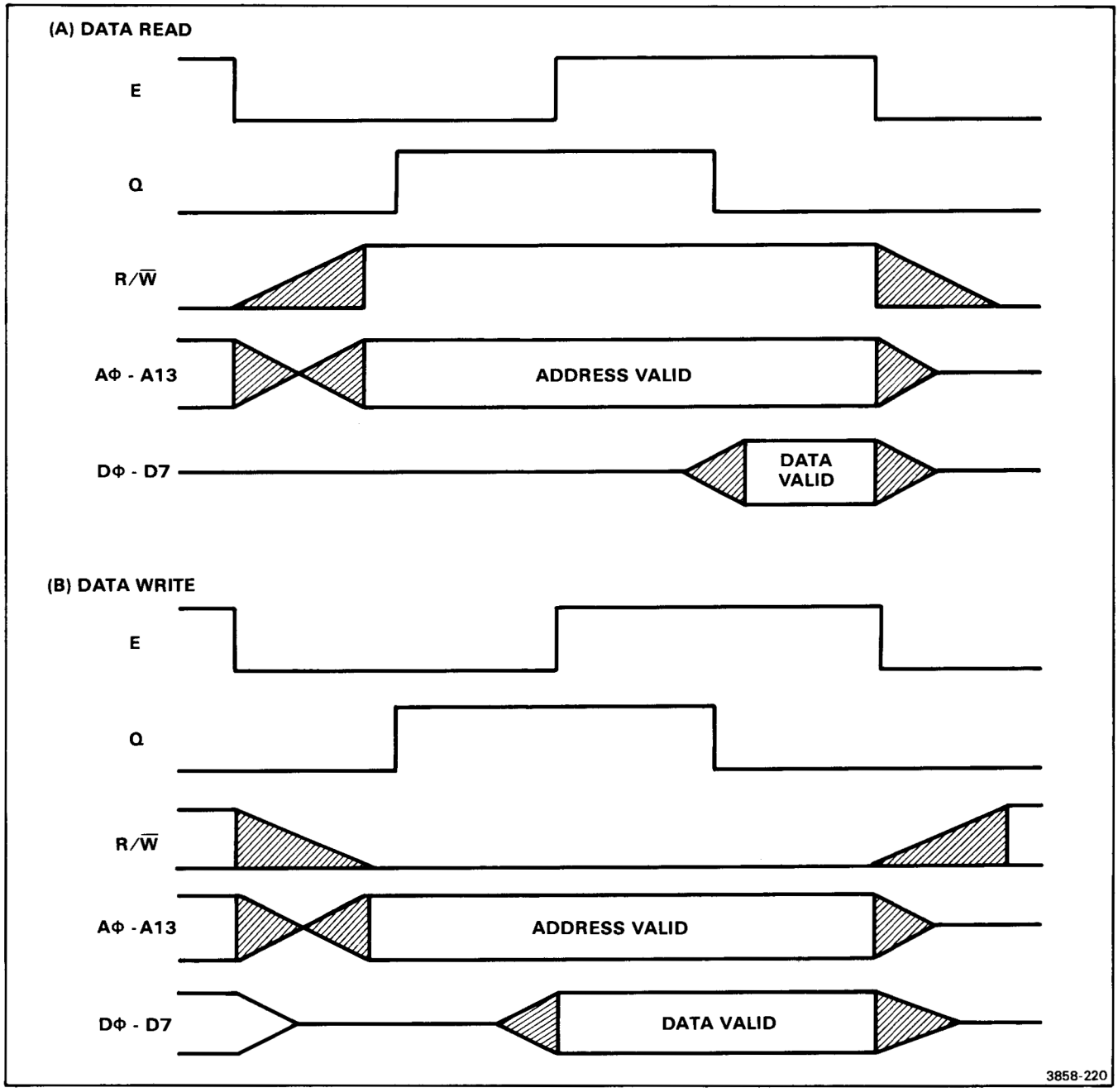

Figure 2-19. Microprocessor (U910) read/write timing.

A low on $\overline{\text{RECALL}}$ also initiates the MRDY hold off, when transferring data from the EAROM (U100) ROM to the on-chip RAM during power on. (See the discussion of the EAROM for an explanation of the function of $\overline{\text{RECALL}}$.

A low on INEX initiates microprocessor hold off when writing to or reading from the MPU board hardware ports. INEX, W/$\overline{\text{R}}$ and E also control the generation of the SELEN signal. (See the discussion of the MPU board hardware ports for an explanation of the function of INEX and for a description of the operation of U825A, U815A and U815C.)

DATA BUS BUFFER

Buffer U1000 buffers the data bus when the microprocessor is transceiving data to and from circuits off the MPU board. The W/$\overline{\text{R}}$ line selects which direction data is transmitted through the buffer. The MWFM, INEX and A10 lines enable the buffer. The buffer is thus enabled either when the microprocessor requires access to the WFM (MWFM high) or when the microprocessor is providing setup information to the Display, Power Supply

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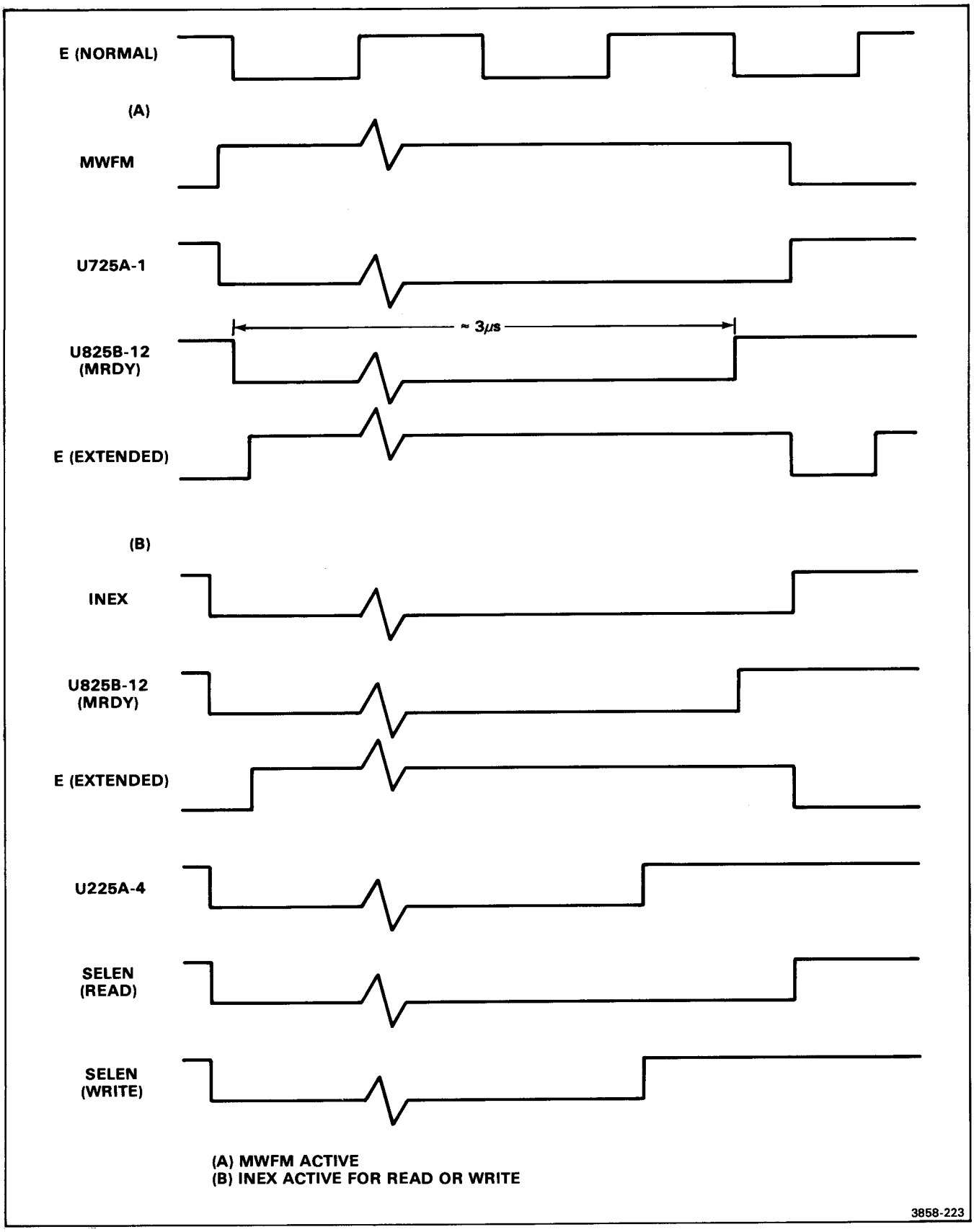

Figure 2-20. Timing of microprocessor memory read logic: (A) MWFM active; (B) INEX active for a read.

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or Memory boards, or the front panel (INEX and A10 high). A low on pin 10 of U725C also sets the EXTEN line low (see the following description of the address latch for an explanation of the function of EXTEN).

ADDRESS LATCHES

Latches U915 and U925 latch the addresses on the address bus (A0-A13) when the microprocessor is communicating with circuits off the MPU board. These latches are required in order to keep the address data valid long enough for the off-board circuits to respond. A low-to-high transition on the LATEN line latches the contents of the address bus into U915 and U925. A low on the U210 pin 9 then outputs the address onto the off-board address bus.

MEMORY AND HARDWARE PORT ADDRESSING

The microprocessor addresses 64K bytes of memory space. This address space (see the memory map in Fig. 2-21) is used to address memory devices (ROM and RAM), hardware ports and the WFM on the Memory board.

Gates U810B, U810D and U725A modify the R/$\overline{W}$, Q and E signals from the microprocessor for use in controlling the memory addressing logic (see Fig. 2-22). U810B inverts the R/$\overline{W}$ line to create the W/$\overline{R}$ line. Both the microprocessor and Memory circuitry use this signal.

Gate U725A combines the Q and E signals, creating a low at the pin 1 output whenever the address from the microprocessor is valid. U810D combines the W/$\overline{R}$ and Q signals to create the write enable input for the static RAMS (U800 and U900) and the EAROM (U100). (See the description of the static RAM circuit for further information on the use of this line.)

Decoders U710, U715 and U610 decode the address lines to select memory locations or hardware ports. U710 selects 8K pages of memory. The Y0 and Y1 outputs select the two pages of waveform memory. U810A creates the MWFM line, which is active when either of the two 8K sections of WFM are selected. The Y4 through Y7 outputs select the four monitor EPROMs (U400, U300, U200 and U500). The Y3 output selects EPROMS U600 and U700.

Decoder U715 selects the memory and hardware ports within the 8K page from 4000H to 5FFFH (the page selected by the Y2 output of U710). The Y2 and Y3 outputs of U715 select static RAMs U900 and U800. the Y0 output controls the CC line, which selects the EAROM (U100). The Y1 output controls the internal-external (INEX) line, which selects hardware port address decoder U610.

Decoder U610 decodes the 2K of addresses assigned to the memory mapped hardware ports (see the description of the MPU hardware ports for further information on the function of U610).

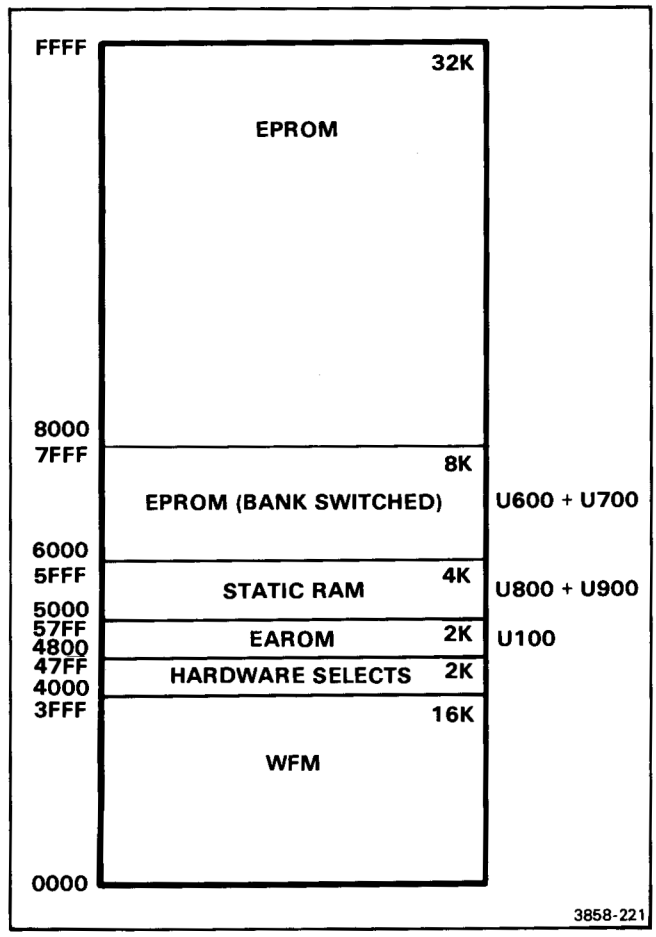

Figure 2-21. MPU board memory map.

MPU BOARD MEMORY (Self Tests 1 through 9)

Monitor ROM

The 7D20 monitor firmware is located in four 8K-byte EPROMs (U400, U300, U200 and U500). U710 provides a separate enable line for each device.

Static RAM

U800 and U900 provide general, temporary data storage space. A low on the W/$\overline{R}$ line enables the memory for a read; a low at the write enable (WE) input (pin 21) enables the memory for a write. The output of U810D pin 11 holds the WE input low until the falling edge of the Q signal to ensure that the memory has time to read the data presented to it.

EPROM

U600 and U700 contain GPIB interface and diagnostics firmware. Each of these devices contain 8K bytes of memory locations, however, they are both addressed from a single 8K page of the memory map. The ENQ input to each device accomodates bank switching to allow both devices to be addressed from the same

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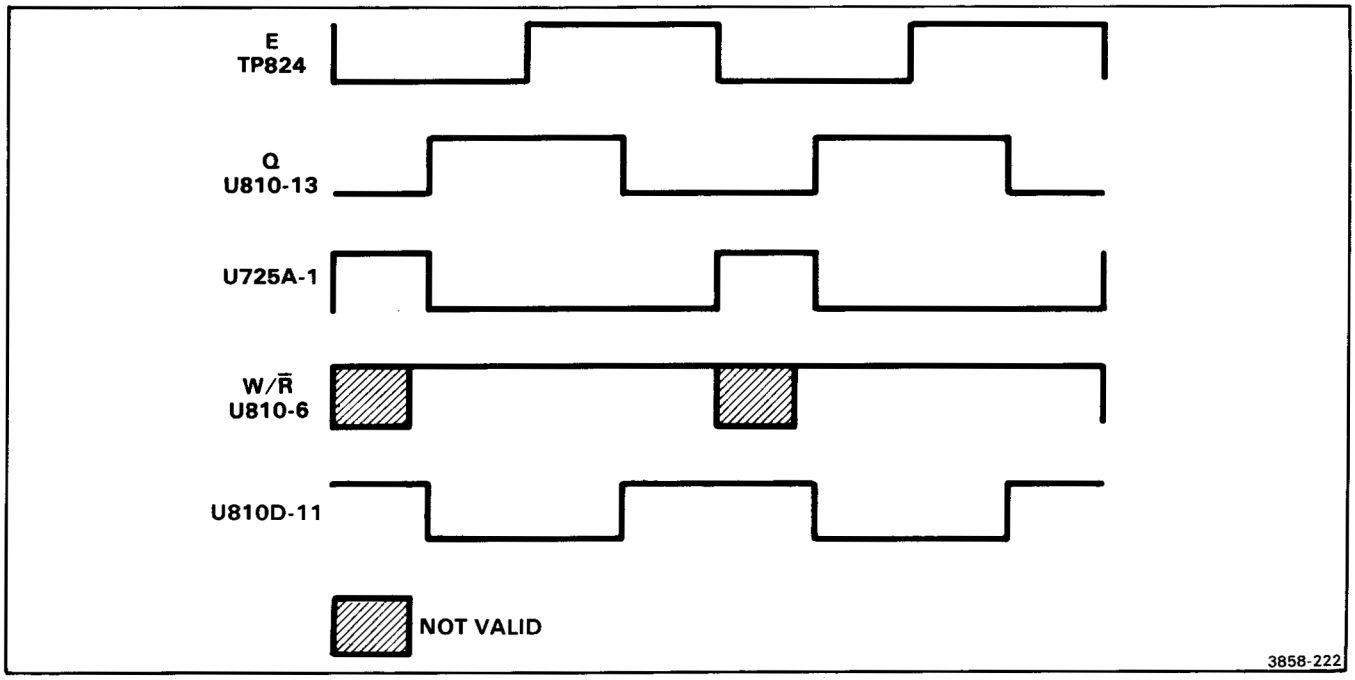

Figure 2-22. Microprocessor memory space select timing.

address space. R-S flip-flop U720A and U720B select which of the two devices is to be accessed from decoded data obtained from U610. When addressing U600 and U700, U720A and U720B are set during one machine cycle; the selected device is then addressed on the next machine cycle.

EAROM

Electrically Alterable ROM (EAROM) U100 contains 1K of volatile RAM and 1K of electrically alterable ROM. During normal operation, the microprocessor stores front-panel settings and parameters such as time/division, volts/division, trigger mode, etc. in the RAM section of U100. When the plug-in is powered down, this data is moved to the ROM section of the device. When the plug-in is powered back up, the data is then transferred back from the ROM section to the RAM section. In this manner, the front-panel settings at the time of power off are retained and the plug-in is automatically reset to these values when power is next applied.

EAROM U100 is a 1-bit wide by 1024 bits, with separate data in and data out ports. A low on the chip select ($\overline{CS}$) line selects the device for a read or a write. A low on the $\overline{RECALL}$ line moves the data from the ROM to the RAM. A low on the $\overline{STORE}$ line moves data from the RAM to the ROM.

Gates U110A through U110D and inverters U120A through U120F control the $\overline{RECALL}$, CS and $\overline{STORE}$ lines. When power is applied to the plug-in, POWERON (pin 11 of U210) is latched high as part of the microprocessor initialization procedure. The high on POWERON sets pin 10 of U110C high. On the next machine cycle, the CC line (pin 15 of U715) is set low, which pulls pin 3 of U110A high, activating both the $\overline{CS}$ and $\overline{RECALL}$ lines.

The low on $\overline{RECALL}$ also sets pin 3 of U815B low (Memory Ready Logic), which fires single-shot U825B and activates the MRDY input to U910. The microprocessor is thus held off for approximately three microseconds to allow additional time to complete the data transfer from U100's ROM to RAM. (See the description of the memory ready logic for more information on the operation of the MRDY line.)

During normal operation of the microprocessor circuitry (POWERON and SNOR low) a low on the CC line sets $\overline{CS}$ low for reads and writes to U100's RAM.

When power to the plug-in is shut down, the $\overline{PWRDN}$ line is pulled low, activating the NMI interrupt (pin 2 of U910). The SNOR line (pin 12 of U210) is then latched high. The resulting high on the anode of CR118 sets the $\overline{CS}$ line low. The high on SNOR also sets pin 13 of U110D high. At the same time, the charge on C215 holds pin 12 of U110D high, so the $\overline{STORE}$ line is set low. When the microprocessor shuts down, CR118 is reverse biased. The charges on C211 and C215, however, hold $\overline{CS}$ and $\overline{STORE}$ low to allow U100 to complete the data transfer from RAM to ROM.

MPU BOARD HARDWARE PORTS

The MPU board contains a number of hardware ports, which are used to control on-board circuits and to

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communicate with off-board circuits. U610 and the address lines select these devices and control the operation of the on-board circuits. INEX, SELEN and A10 enable U610.

When U715 (Memory and Hardware Port Addressing) sets INEX low to select the hardware ports, pin 6 of U815B is set high. Single-shot U825B then extends the current microprocessor cycle for approximately 3 microseconds to allow enough time for the data to be read from or written to the hardware ports. (See the description of the memory ready logic for an explanation of the use of the MRDY input to U910.)

The high at pin 6 of U815B also sets pin 11 of U815C high. The select enable line (SELEN) is then set according to the state of W/$\overline{R}$ and E (see Fig. 2-20). If the microprocessor is reading a hardware port, W/$\overline{R}$ is set low, which sets pin 10 of U815C low. SELEN remains low for the duration of the E signal. Since the high on MRDY extends the active time of E, SELEN is in effect active for the duration of U825B's single-shot interval.

If the microprocessor is writing to a hardware port, W/$\overline{R}$ is set high. Single-shot U825A thus controls SELEN. U825A has a single-shot interval of approximately 2.4 μs. When INEX is set low, SELEN is thus pulled low for approximately 2.4 μs.

Data Latches

Addressable latches U210 and U315 latch the hardware selects, enable lines and data applied to off-board circuits. The Y7 output of U610 selects U210 and Y6 selects U315. Address lines A1, A2 and A3 select to which output the input data are sent. The D1 line supplies data to U210; D2 supplies data to U315.

The Q0, Q1 and Q2 outputs of U210 control analog switch U220. Q3 and Q4 control channels A, B and C of analog switch U125. Q5 controls the FREERUN line, which is connected to the Trigger board. Q6 and Q7 control the POWERON and SNOR lines, respectively. (See the previous description of the EAROM circuit for an explanation of the functions of POWERON and SNOR.)

The Q0, Q1, Q2 and Q3 outputs of U315 provide the two least significant bits of the 10-bit words applied to position DACs U320 and U420. Q4 and Q5 control the serial data in (SDI) and serial data strobe (SDS) lines, which provide setup data to the Time Base, Trigger and Preamp Boards. (Note that D2 is the source of the SDI data.) Q6 is a START/STOP test point. Q7 initiates an A-to-D conversion by U525.

Shift Registers

Shift registers U310 and U410 provide the eight most significant bits of the 10-bits words that are applied to the position DACs. The Y4 and Y5 outputs of U610 clock these shift registers. The D3 line supplies data to U310 and D4 supplies data to U410.

System Clock and Off-Board Select Decoder

Address decoder U1010 activates the three system clock lines ($\overline{SCK1}$, $\overline{SCK2}$ and $\overline{SCK3}$), the GPIB select line ($\overline{GPIBSEL}$), and the front-panel select line ($\overline{FPSEL}$) and the two general select lines ($\overline{GENSELA}$ and $\overline{GENSELB}$). When INEX and SELEN are set low, U1010 decodes address lines A8, A9 and A10 to pull one of the outputs low. The microprocessor uses these lines to clock data to off-board circuits, select inputs to the microprocessor, and initiate off-board operations. The unused output is selected when writing or reading on the MPU Board.

POSITION CONTROL (Self Tests 11 and 12)

The MPU board has two DACs (U320 and U420) and a multiplexer (U125) that provide programmable vertical positioning voltage to the Preamp board. U320 and U420 convert vertical positioning data from the microprocessor to an analog current that is proportional to the digital input. U320 receives its 10-bit digital data from U310 and U315; U420 receives its digital information from U410 and U315.

The current outputs of the DACs are applied to current-to-voltage converters U325B and U325A. R322 and R523 set the current-to-voltage conversion ratio for each DAC. The position voltage is transmitted through U125 to the CH 1 POS and CH 2 POS lines. Position control voltages from the front-panel POSITION controls (CH 1 POS FP and CH 2 POS FP) are also applied through U125 to the CH 1 POS and CH 2 POS lines. The CH 1 POS and CH 2 POS lines are applied to the Preamp board. Either the front-panel POSITION controls or the programmable position voltages from the position DACs thus control the vertical positioning of the trace on the crt screen.

The microprocessor, through Q3 of U210, selects the source of the positioning voltage: Y inputs to channels A and C for front-panel control; X inputs for microprocessor control. The Q4 output of U210 selects one or the other microprocessor-controlled position voltages for output to analog switch U220.

SELF TEST AND ANALOG DATA PROCESSING (Self Test 10)

Analog switch U220 and A-to-D converter U525 convert self test, probe coding, trigger level and position voltage into digital values, which the microprocessor uses to analyze the operation of the various circuits in the plug-in unit.

The Q0, Q1 and Q2 outputs of U210 (MPU Hardware Ports selection) select one of the eight analog inputs to U220 for transmission to the pin 3 output. The following signals can be selected: ABUS1, ABUS2, +2.5V REF, ground reference, CH 1 POS FP, CH 2 POS FP, TRIG LEVEL and the Ch 1 or Ch 2 position DAC output from pin 15 of U125. The ABUS1 and ABUS2 lines transmit either

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self-test signals or probe coding information. Analog switches on the various boards in the plug-in select the signals applied to ABUS1 and ABUS2.

The output of U220 is applied to U525. A high on the INIT input to U525 initiates an A-to-D conversion of the input level. The 10-bit digital output of U525 is applied to the microprocessor through data bus multiplexer U515 and U510. A high on the BUSY output of U525 indicates to the microprocessor that an A-to-D conversion is in process.

On power on, the microprocessor selects the +2.5V REF and ground reference levels for A-to-D conversion by U525. These levels are then used to calculate a calibration factor for U525 to read the offset and gain errors.

Data Bus Multiplexer

U510 and U515 are two-channel, four-bit multiplexers with tri-state outputs. The A0 line selects either channel A or channel B for output onto the data bus. The Y3 output of U610 enables the outputs of U510 and U515. The data bus multiplexer transmits the output of A-to-D converter U525 to the microprocessor. Note that since U525 has a 10-bit output, two machine cycles are required to transmit the data to the 8-bit data bus. U515 also transmits the U525 BUSY line to the microprocessor. U510 transmits the SSRST signal from the Trigger board and the TRIG'D and serial data out (SDO) lines from the Time Base and Trigger Boards to the microprocessor. The SDO line transmits Time Base self test data and the fast ramp count to the microprocessor. Connectors J510 and J410 are used in troubleshooting the MPU board and for manufacturing testing.

TRIGGER

The Trigger circuitry is located on the Trigger Board (A10). This circuitry produces the trigger gate signals (TGE and $\overline{\text{TGE}}$), to which the Time Base circuitry references acquired data. The Trigger Board also contains the horizontal display signal output amplifier, a blanking signal buffer amplifier and the sweep gate and holdoff circuit.

DETAILED BLOCK DIAGRAM DESCRIPTION

The microprocessor reads the settings of the front-panel TRIGGERING pushbuttons and controls (or externally programmed triggering data) and converts it into corresponding Trigger circuitry setup data. It supplies this setup data to three serial data latches on the Trigger board (A10) through the serial data (SDI) line (see Fig. 2-23). This setup information selects the trigger mode, source, coupling, trigger level and analog bus output.

The trigger level circuit converts the digital trigger level data from the microprocessor to an analog trigger level. The voltage level on the PEAK-TO-PEAK line sets the trigger level range and thus the range of the front-panel TRIGGERING LEVEL control.

The external trigger circuit adjusts the amplitude and dc level of the external trigger signal to match the input requirements of the trigger generator circuit.

The coupling and source logic select the trigger source and coupling according to setup data received from the microprocessor.

The trigger generator produces the trigger gate signals (TGE and $\overline{\text{TGE}}$). The microprocessor establishes the trigger level and slope through the serial data latches. The trigger generator then monitors the selected trigger source and produces a trigger gate when the trigger signal reaches the trigger level on the selected trigger signal slope.

The peak-to-peak detector measures the peak-to-peak amplitude of the trigger signal. It then applies a voltage to the trigger level circuit that is proportional to the magnitude of this peak-to-peak amplitude.

The sweep gate circuit converts the display interrupt ($\overline{\text{DISPINTR}}$) signal into the SWEEP GATE and HOLDOFF signals to control the mainframe display.

The single-sweep circuit allows the trigger circuit single-sweep (HOLD NEXT) mode to be reset externally.

TRIGGERING MODES

The front-panel TRIGGERING pushbuttons select the triggering mode, trigger signal coupling, trigger source and trigger slope. The microprocessor then supplies corresponding setup information to the Trigger circuitry. In addition, the microprocessor converts the analog voltage from the front-panel TRIGGERING LEVEL control into a digital value, which is supplied to the Trigger circuitry to establish the trigger level.

Four triggering modes are allowed: normal, auto, peak-to-peak and hold next. In the normal triggering mode, the Trigger circuitry is first set for the desired trigger source, coupling and trigger level. The trigger generator is then reset (enabled). When the trigger signal reaches the trigger level, the trigger gate is activated and remains active until the end of the acquire cycle. Following the output of a trigger gate, the trigger generator remains latched until it is again reset.

The auto mode is similar to the normal mode. The trigger generator is setup and enabled as in the normal mode.

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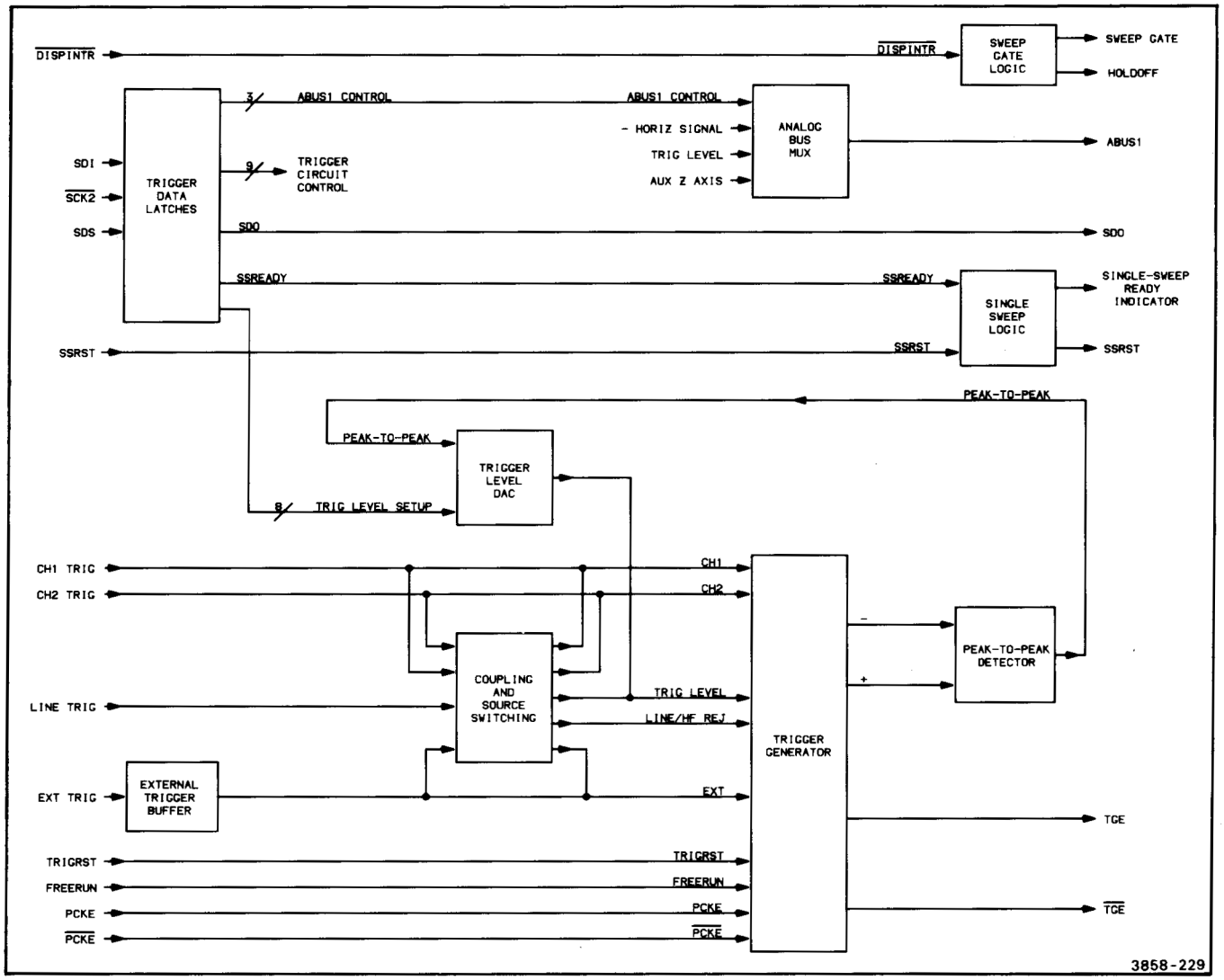

Figure 2-23. Block diagram of trigger circuitry.

When the trigger generator is enabled, however, the microprocessor begins counting. If an appropriate trigger event is not received within 33 ms (3.3 ms in the equivalent time digitizing—ETD—time base mode) of the enabling of the trigger generator, a trigger gate is generated automatically.

The peak-to-peak mode is a variation of the auto mode. In this mode, the peak-to-peak amplitude of the trigger signal is measured. The magnitude of this measurement is then used to set the range of the trigger level DAC (and thus the range of the front-panel TRIGGERING LEVEL control). Reducing the trigger level window of the DAC to the peak-to-peak amplitude of the trigger signal, simplifies triggering adjustments. The trigger generator then generates valid triggers from a wide variety of input signal amplitudes with less need to readjust the TRIGGER LEVEL control (see Fig. 2-24).

The hold next mode is used to acquire a single waveform record. The trigger generator is set as usual for triggering. In all time base modes except the ETD mode, one trigger gate is then generated and the reset of the trigger generator is held off, inhibiting any further acquisition cycles. In the ETD mode, gates are generated until the waveform record is complete.

The trigger is selected from one of five sources: Ch 1, Ch 2, line, external and fast ramp test. When Ch 1 or Ch 2 is selected as a trigger source, a portion of the input signal is picked off and supplied to the trigger generator. When the line source is selected, the 60 Hz (or 50 Hz) line voltage from the mainframe is attenuated and applied to the trigger generator. The external source can be any signal applied to the EXT TRIG connector that is within the range of the external trigger circuit. When the MODE pushbutton is pressed, the microprocessor automatically

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selects either Ch 1 or Ch 2 as the trigger source depending on the AQR MODE that has been selected. For the CH 1, BOTH or ADD modes, the Ch 1 trigger is selected. For the CH 2 mode, the Ch 2 trigger is selected.

The trigger signal can be coupled to the trigger generator in five ways: dc, ac, ac low frequency reject, ac high frequency reject and dc high frequency reject. When dc coupling is selected, the trigger signal is applied directly to the trigger generator circuit, allowing triggering on the full frequency range of the 7D20. Ac coupling allows triggering on only ac signals above approximately 30 Hz. Low frequency reject coupling attenuates the low frequency component of the trigger signal. High frequency reject coupling attenuates the high frequency component of the trigger signal. The high and low frequency filters both have -3 dB attenuation at approximately 40 kHz.

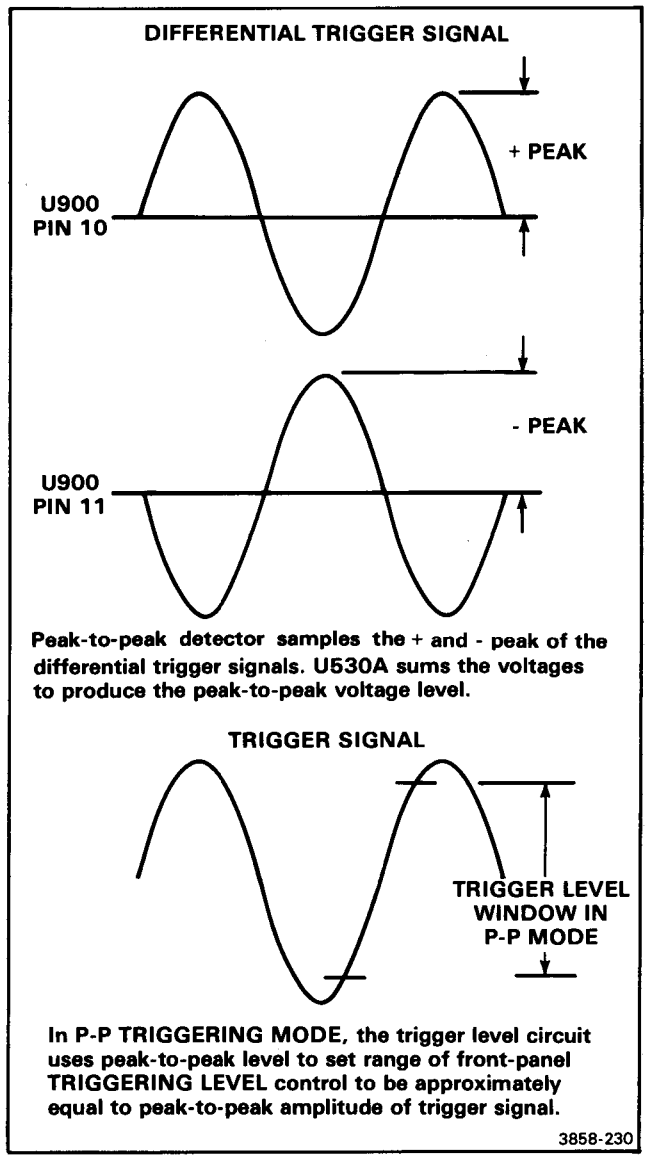

Figure 2-24. Peak-to-peak detector in p-p triggering mode.

DETAILED CIRCUIT DESCRIPTION

TRIGGER DATA LATCHES

Serial data latches U210, U201 and U200 are connected in series, the overflow data from one shift register being applied to the data input of the next. They receive Trigger circuitry setup data from the microprocessor through the serial data in (SDI) line. Pin 15 of each device is wired to +5 V, which permanently enables the data outputs. Data are shifted one place in each latch device with each rising edge of the serial data clock 2 ($\overline{SCK2}$) signal. A positive-going pulse on the serial data strobe (SDS) line latches the setup data to the outputs of the three latches

Gate U101D inverts the $\overline{SCK2}$ signal so that it can be used to clock the serial data out (SDO) information through gate U101B. Data on the SDO line are supplied to the MPU board.

TRIGGER GENERATOR (Self Tests 47 and 50)

The trigger generator circuit is composed of trigger generator U900 and its associated filter and biasing network. As shown in Figure 2-25, U900 uses a split path amplifier circuit. One side of the amplifier is configured to accept only high frequency signals and the other side is configured to accept only low frequency signals. The input signal (Vin) is applied directly to the high frequency input of U900 through a capacior. An inverting operational amplifier with unity gain drives the low frequency input. The trigger level is also applied through the operational amplifier to the low frequency input. The trigger level sets the threshold level of the amplifier. When the trigger generator is enabled, the trigger gate signals (GATE and $\overline{GATE}$) are activated whenever the input signal becomes greater then this threshold level (+ slope triggering) or less than the level (- slope triggering).

The RESET, -SLOPE SELECT and HYST inputs control the enabling of the trigger generator and the selection of trigger slope and hysteresis. When the Time Base circuitry begins an acquisition cycle, it sets the trigger reset (TRIGRST) line low. Upon receipt of this reset pulse at pin 17, U900 begins monitoring the trigger signal. When the signal reaches a selected enabling level, U900 enables itself (see Fig. 2-25). The enabling level is either slightly below (+ slope triggering) or slightly above (- slope triggering) the trigger level. Once enabled, U900 continues to monitor the trigger signal, activating the trigger gate when the trigger threshold is crossed. U900 then remains in a latched state until it is again reset.

The -SLOPE SELECT input (pin 8) determines which slope of the trigger signal that U900 activates on. If pin 8 is set low, U900 sets the enabling level below the trigger level. U900 can thus produce a trigger gate only on the positive-going slope of the trigger signal. If pin 8 is set high, U900 sets the enabling level above the trigger level,

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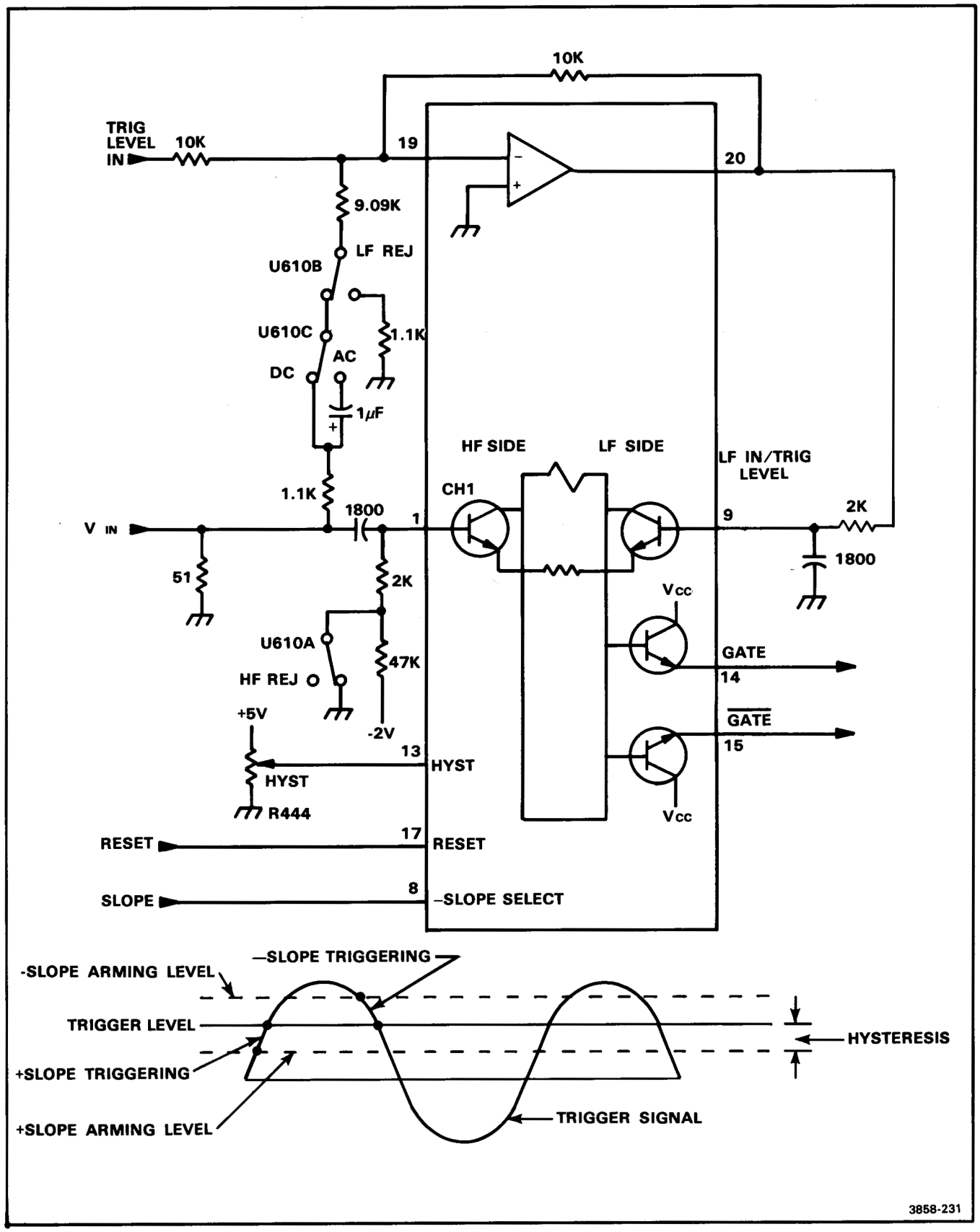

Figure 2-25. Simplified schematic of trigger generation U900.

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allowing trigger gates to be produced only on the negative-going slope of the trigger signal.

The HYST input (pin 13) controls the voltage difference (hysteresis) between the enabling level and the trigger level. The HYST adjustment (R444) sets the voltage level at pin 13 and in turn sets the hysteresis. SLOPE adjustment R440 controls the balance between the triggering level in + slope and - slope operation.

The FREERUN input to U900 causes a trigger gate to be generated automatically. The microprocessor controls this line, pulling it high at the end of the auto triggering waiting time interval in the Auto mode. The trigger reset signal (TRIGRST) can terminate the gate signals (GATE and $\overline{\text{GATE}}$), even if FREERUN is asserted (high).

Differential amplifier Q1011 and Q1010 amplifies and invert the GATE and $\overline{\text{GATE}}$ pulses to produce the trigger gate pulses (TGE and $\overline{\text{TGE}}$).

For the fast ramp self test (FRT high), the phase clock signals (PCKE and $\overline{\text{PCKE}}$) from the time base provide a trigger source through Q1020, Q1022 and Q800.

TRIGGER LEVEL (Self Test 46)

The trigger level circuit consists of a digital-to-analog converter (DAC) (U310) and an inverting operational amplifier (U530D). U310 converts the digital trigger level data from serial data latch U310 into an analog current that is proportional to the digital input. Most of the output current of U210 flows through R311. U530D amplifies the resulting voltage across R311. The output voltage at pin 14 of U530D determines the trigger threshold level of trigger generator U900.

The voltage level on the PEAK-TO-PEAK line, which is applied to the VREF- input to U310 (pin 15), determines the overall current output range of U310. Since the output current of U310 is proportional to the setting of the front-panel TRIGGERING LEVEL control, the voltage level on the PEAK-TO-PEAK line also determines the range of the TRIGGERING LEVEL control.

In all triggering modes except P-P, divider R330 and R331 (near the peak-to-peak detector circuit) set the range of U310 for approximately 0 to 1 mA. In the peak-to-peak triggering mode, the level on the PEAK-TO-PEAK line is proportional to the magnitude of the peak-to-peak amplitude of the trigger signal. The front-panel TRIGGERING LEVEL control is thus desensitized to the peak-to-peak window of the trigger signal (see Fig. 2-24).

The manual trigger level (Man Trig Level) adjustment (R402) allows the trigger level to be set manually during manufacturing testing.

The voltage from the + side of the peak-to-peak detector (Pin 15 of U430B) is applied to amplifier U530D through the + PEAK line and input resistor R532. This voltage shifts the baseline level of the trigger level circuit output at pin 14 of U530D in proportion to the + peak magnitude. This operation readjusts the trigger level when the dc level of the trigger signal is changed. Centering (Cent) adjustment R543 allows system offsets to be nulled out when the TRIGGERING LEVEL control is at midrange.

Operational amplifier U530D has a gain of approximately 0.13. Analog switch U430A switches the P-P Range adjustment (R541) into the operational amplifier circuit in the P-P mode to allow the operational amplifier to be set for higher gain, which is required for proper level range in this mode.

EXTERNAL TRIGGER

The external trigger circuit attenuates the external trigger signal and converts the high impedance external trigger input into a low impedance output.

A frequency compensated divider network (C1043, R1042 and R1043; R942, C942 and R941; R843 and C940; and R940) provide approximately ÷5.7 (EXT ÷1 mode) and ÷57 (EXT ÷10 mode) attenuation of the signal applied to the EXT TRIG input connector. C1041 couples the ac component of the external trigger signal to the impedance converter in the ÷1 mode; C941 couples the ac component of the external trigger signal in the ÷10 mode.

Transistors Q1040, Q1030, Q940 and Q931, and operational amplifiers U940 and U830A form a split path impedance converter amplifier. Q1040 and Q1030 amplify the ac component of the external trigger in the ÷1 mode; Q940 and Q931 amplify the ac component of the external trigger in the ÷10 mode; and U940 and U830A amplify the dc component of the external trigger. Figure 2-26 shows a simplified schematic for the EXT ÷1 path and the dc path of this circuit. Q1040 and Q1030 convert the signal from high impedance to low impedance. Transistors Q630 and Q631 select which of the impedance paths are activated. For example, when the ÷1 line is high (EXT ÷1 mode), Q631 is turned off and Q630 is turned on. The gate of Q940 is thus pulled to approximately −10 V, which turns it off. The gate of Q1040 is raised to approximately +2 V, which turns it on. When Q1040 is turned on, CR831 is also forward biased, allowing voltage from the dc path to be applied to the gate of U1040. The ÷10 path is activated in a similar manner when the ÷1 line is low.

Operational amplifier U940 amplifies only the dc component of the external trigger signal. With an input resistance of approximately 1 MΩ (R1042 + R942 + R940), U940 provides an attenuation of the signal of approximately −6.2. When ac coupling is selected, the dc input to Q640 is pulled low. Q640 and Q930 are thus turned on, which shorts the input of U940 to its output, reducing its gain to 0. This disabling of U940, plus the switching of the output of analog

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switch U740B to ground, disables the dc path of the external trigger circuit. Analog switch U740A causes the dc signal to be applied to divider R743 and R744 in the ÷ 10 mode.

The external input signal and the external impedance converter output signal are input to operational amplifier U830A. These signals, which appear at R740 and R931 respectively, are summed at the virtual ground input at pin 2 of U830A. The error-correcting signal developed at pin 1 of U830A is used in a feedback loop to improve the accuracy of the external impedance buffer.

In the AC coupled mode, Q830 (operating as a switch) is turned on, reducing the feedback impedance of U830A. No signal is present across R740, since it is grounded via analog switch U740B pin 2. The output signal at the emitters of Q1030 and Q931 is supplied to U830A through input resistor R931. The feedback loop completed by the coupling of U830A's output (pin 1) to ipedance converting amplifiers Q1040 and Q1030 (or Q940 and Q931 in the EXT ÷10 mode) provides low-frequency stability for the circuit.

Diodes CR1040 and CR935 protect the inputs to Q1040 and Q940. CR933 and CR1030 keep the bases of Q931 and Q1030 from being pulled excessively negative when Q940 and Q1040 are turned off.

COUPLING AND SOURCE LOGIC

Multiplexer U710 selects the trigger signal that is applied to the trigger generator, using setup information from the microprocessor. U610A, 610B and U610C couple the selected signal to U900. The transistor shown as the high frequency input to U900 in Figure 2-25, is actually five transistors with emitters and collectors in parallel. The inputs to these transistors at pins 1, 3, 5, 7 and 4 provide inputs to the high frequency path for the five allowable trigger sources: CH 1, CH 2, LINE, EXT TRIG, and PCKE and $\overline{\text{PCKE}}$, respectively. PCKE and $\overline{\text{PCKE}}$ are used as a trigger source during the fast ramp self test (FRT high).

Multiplexer U710 selects one of the four front-panel selected trigger sources through the Y output and through analog switch U610C and U610B to the low frequency side of the trigger generator amplifier. (The low frequency path goes through the operational amplifier in U900 and into the LF IN/TRIG LEVEL input at pin 9 of U900.)

The X half of U710 in turn enables the selected trigger source to be applied to the high frequency path. Dividers R802 and R703, R810 and R710, R711, and R811, R812 and R712, normally connect the bases of the high frequency signal input transistors to −2 V, which holds the input transistors off. U710 raises the base of the input transistor that corresponds to the selected trigger signal to ground through analog switch U610A, which enables the selected trigger signal to be applied to the high frequency side of the trigger generator amplifier.

For example, if CH 1 is selected as the trigger source, U710 enables the pin 1 input to U900 and couples the CH 1 signal through R700 to pin Y (U710), and then through U610B, U610C and R904 to pin 19 of U900.

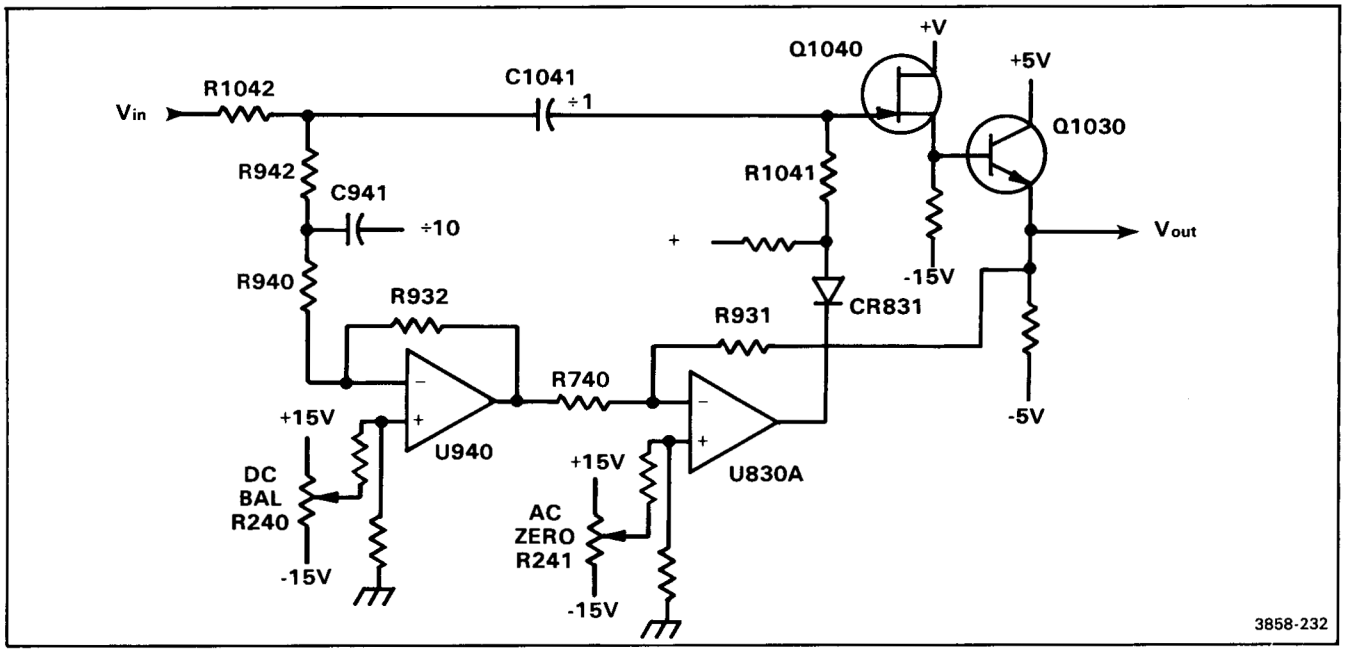

Figure 2-26. Simplified schematic of external trigger circuit.

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Analog switch U610C selects either dc or ac coupling. In the dc coupled mode, the input signal is coupled directly through U610C, to the low frequency path. In the ac coupled mode, the input signal is coupled through capacator C600, which blocks the dc component of the trigger signal. When low frequency reject coupling is selected, analog switch U610B disconnects the low frequency path from the input signal.

When high frequency reject coupling is selected, U610A opens the X input to U710. The CH 1, CH 2 and EXT inputs to the high frequency path are thus disabled. The transistor at pin 5 of U900 is enabled through U610A pins 13 and 14, however, to provide the proper biasing for the amplifier, even though a signal is not applied to the high frequency path. Note also that when the LINE trigger source is selected, the line signal is only applied to the low frequency path, but pin 5 of U900 is enabled, again for proper biasing of the amplifier.

PEAK-TO-PEAK DETECTOR

Trigger generator U900 also has an amplifier that presents a signal proportional to the trigger signal at output pins 10 and 11. Operational amplifier U530C and U530B peak-detect these signals. For example, the base-emitter junction of the transistor that drives pin 11 of U900 and capacitor C921 rectify the (–) signal at pin 11. Voltage peaks are retained for only a short period due to a short time constant. Non-inverting amplifier U530C and its associated components retain peak voltages on capacitor C630 for longer periods of time. Only positive peak voltages appear on C630 due to rectification by CR531. CR530 and CR532 provide an alternate feedback path for U530C for negative-going signals. C630 is thus charged to the positive peak of the (–) signal. In the peak-to-peak mode, this voltage level is applied through analog switch U430C to summing operational amplifier U530A.

Likewise, U530B, CR431 and C546 peak detect the (+)signal and apply the resulting voltage level through U430B to U530A. U530A sums the two peak levels. Since the input signals to this circuit are differential, the sum of the positive peaks are proportional to the magnitude of the peak-to-peak amplitude of the trigger signal (see Fig. 2-24). The output of U530A is applied to the PEAK-TO-PEAK line, which is applied to the trigger level circuit.

In the Normal, and Auto triggering modes, divider R330 and R331 sets the peak levels applied to U530A, and thus determines the voltage level on the PEAK-TO-PEAK line. (See the description of the trigger level circuit for an explaination of the function of the PEAK-TO-PEAK line.)

Operational amplifier U830B and diode CR730 provide temperature compensation for this circuit. The -Peak Offset and +Peak Offset adjustments (R645 and R546) adjust the dc level of the outputs of their respective operational amplifiers, and thus allow the peak detectors to be balanced.

ANALOG BUS MULTIPLEXER

Analog switch U300 selects one of three signals (–horizontal display output, auxiliary Z axis or trigger level) to be transmitted to the microprocessor via analog bus 1 (ABUS1). The inputs to pins 11 and 10 of U300 select the input signal; a low on pin 6 enables the signal to be applied to ABUS1.

SWEEP GATE

Transistors Q240, Q140 and Q141, and dual nand gate U140 produce the SWEEP GATE and HOLDOFF signals, which are supplied to the 7000-series mainframe interface. Common base amplifier Q240 transmits the display interrupt ($\overline{\text{DISPINTR}}$) signal to pin 6 of U140. When $\overline{\text{DISPINTR}}$ is low, the HOLDOFF line is set high and the SWEEP GATE line is set low; when $\overline{\text{DISPINTR}}$ goes high, the HOLDOFF and SWEEP GATE outputs are switched. R146 and C240 cause the SWEEP GATE transistions to be slightly delayed from the HOLDOFF transitions.

SINGLE SWEEP

The single sweep circuit (U101C, U100A and Q120) allows the trigger circuit to be reset externally when in the single-sweep (HOLD NEXT) mode. When the single sweep reset (SSRST) line from the mainframe is pulled low, the Q output of U100A is reset high. The SSRST line to the MPU board (pin 27A of P210) is then set high. In response to this high on SSRST, the microprocessor sets up the trigger circuit, then initiates an acquisition cycle, which removes the reset to the trigger circuit (low on the TRIGRST line P210-11B).

In setting up the trigger circuit, the microprocessor also sets pin 10 of U101C high through the serial data bus, which in turn activates the SINGLE-SWEEP READY INDICATOR line and clocks the SSRST line low.

HORIZONTAL DISPLAY OUTPUT AMPLIFIER

See the description of the Display circuitry for a discussion of the horizontal display output amplifier (U230B and U230A).

BLANKING OUTPUT AMPLIFIER

See the description of the Display circuitry for a discussion of the blanking output amplifier circuit (Q110).

TIMEBASE BOARD

The Time Base circuitry is located on the Time Base board (A11). It provides basic timing information for the CCD, Memory and Display circuitry as well as the Time Base circuitry itself. It also controls the Time Base modes.

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Because of the complexity of this circuitry, the circuit description has been divided into three sections: detailed block diagram description, detailed circuit description, and description of the operation of the Time Base circuitry for each Time Base mode. It will be helpful before reading this section to review the description of the Time Base and the Time Base Modes given in the Overall Block Diagram Description at the beginning of this section.

DETAILED BLOCK DIAGRAM DESCRIPTION

The serial data latches (see Fig. 2-27) accept Time Base setup information from the microprocessor on the serial data bus. This information is then used to set up the sample counter, the post-trigger counter, phase clock generator and the time base mode according to the time/division setting. The serial data latches also latch time base control data and the fast ramp count, and transmit the data back to the microprocessor on the serial data bus.

The clock generator circuit provides the basic timing for the Time Base circuitry. The twelve different clock signals that the clock generator produces are used within the Time Base circuitry; selected clock signals are also distributed to the Memory and Display circuitry.

The phase clock generator produces the phase clock signals (PCK and $\overline{\text{PCK}}$), which control the sample rate of the CCDs. The phase clock signals are also used within the Time Base circuitry.

The sample counter determines which of the samples from the CCDs are actually stored in the WFM. In the roll and real-time digitizing (RD) modes, it counts down the 400 kHz signal and produces a sample clock pulse at selected intervals (every 100th phase clock pulse, every 1000th, etc.) depending on the time/division setting (see Table 2-11). In the extended real-time digitizing (ERD) and equivalent time digitizing (ETD) modes, it uses the 800 kHz signal as the sample clock.

The acquire waveform clock (AWCK) generator divides the sample clock by 2 and synchronizes it with the

TABLE 2-11
Timing of Time Base Modes

Mode	TIME/DIV	Sample Clock U800-5)	AWCK	PCK (U1220-5)		PCK/ AWCK	VSCK AWCK
EXT	ET CK	EXT RATE	EXT RATE	Fast-In NA	Slow-Out 400kHz		
Roll	20 s	5 Hz	5 Hz	Not	400 kHz	80 k/1	AWCK
	10 s	10 Hz	10 Hz	Applicable	400 kHz	40 k/1	AWCK
	5 s	20 Hz	20 Hz	"	400 kHz	20 k/1	AWCK
	2 s	50 Hz	50 Hz	"	400 kHz	8 k/1	AWCK
	1 s	100 Hz	100 Hz	"	400 kHz	4 k/1	AWCK
	500 ms	200 Hz	200 Hz	"	400 kHz	2 k/1	AWCK
	200 ms	500 kHz	500 Hz	"	400 kHz	800/1	AWCK
	100 ms	1 kHz	1 kHz	"	400 kHz	400/1	AWCK
RD	50 ms	2 kHz	2 kHz	"	400 kHz	200/1	AWCK
	20 ms	5 kHz	5 kHz	"	400 kHz	80/1	AWCK
	10 ms	10 kHz	10 kHz	"	400 kHz	40/1	AWCK
	5 ms	20 kHz	20 kHz	"	400 kHz	20/1	AWCK
	2 ms	50 kHz	50 kHz	"	400 kHz	8/1	AWCK
	1 ms	100 kHz	100 kHz	"	400 kHz	4/1	AWCK
	500 μs	200 kHz	200 kHz	"	400 kHz	2/1	AWCK
ERD	200 μs	400 kHz	400 kHz	200 kHz	200 kHz	1/2	PCK
	100 μs	400 kHz	400 kHz	400 kHz	200 kHz	1/2	PCK
	50 μs	400 kHz	400 kHz	800 kHz	200 kHz	1/2	PCK
	20 μs	400 kHz	400 kHz	2 MHz	200 kHz	1/2	PCK
	10 μs	400 kHz	400 kHz	4 MHz	200 kHz	1/2	PCK
	5 μs	400 kHz	400 kHz	8 MHz	200 kHz	1/2	PCK
	2 μs	400 kHz	400 kHz	20 MHz	200 kHz	1/2	PCK
ETD	1 μs	400 kHz	400 kHz	20 MHz	400 kHz	1/1	PCK
	500 ns	400 kHz	400 kHz	20 MHz	400 kHz	1/1	PCK
	200 ns	400 kHz	400 kHz	20 MHz	400 kHz	1/1	PCK
	100 ns	400 kHz	400 kHz	20 MHz	400 kHz	1/1	PCK
	50 ns	400 kHz	400 kHz	20 MHz	400 kHz	1/1	PCK

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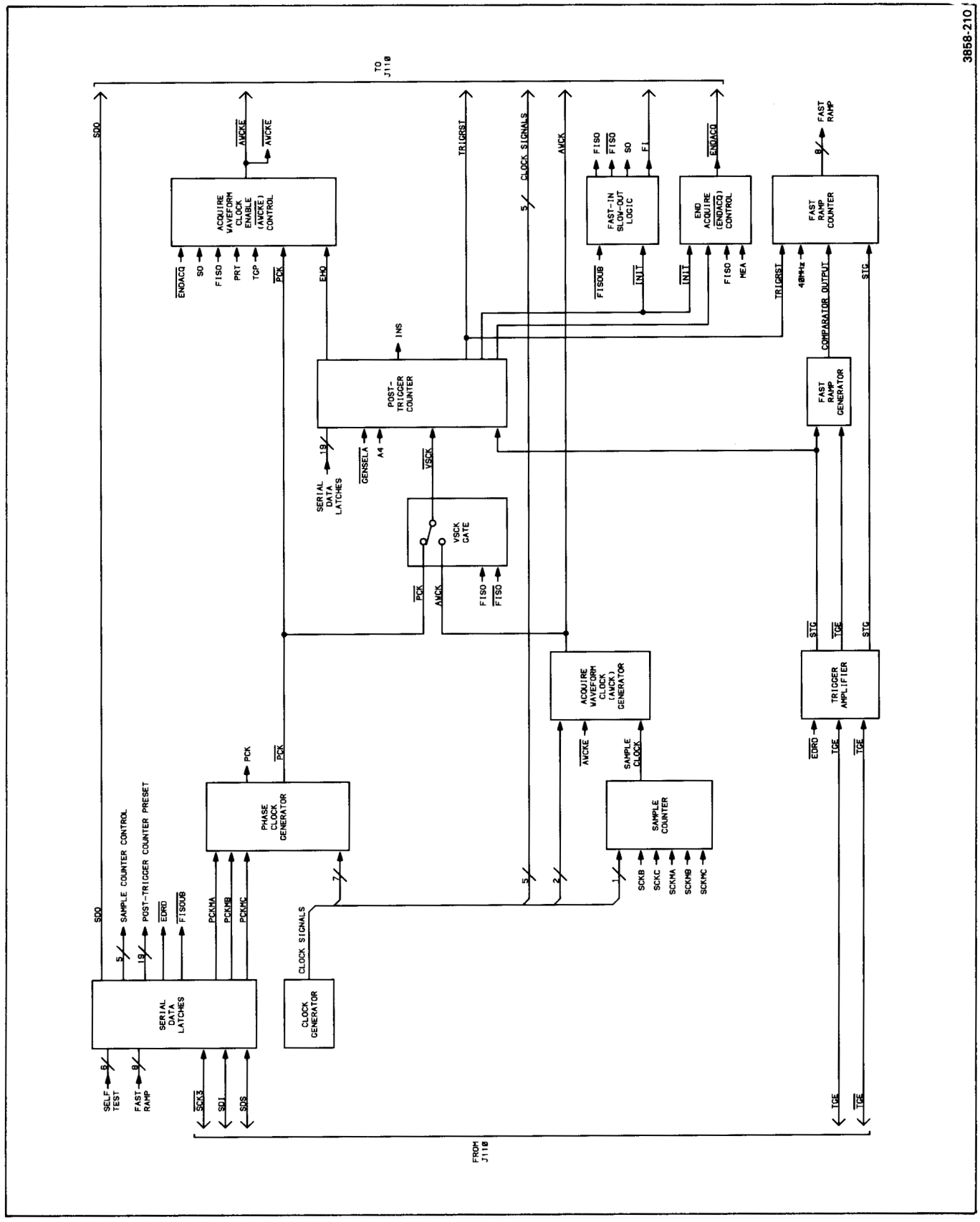

Figure 2-27. Detailed block diagram of time base circuitry.

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memory timing signals to produce the $\overline{\text{AWCK}}$ signal. $\overline{\text{AWCK}}$ indicates to the WFM that a valid sample is available to be written into the WFM.

The acquire waveform clock enable (AWCKE) circuit controls the $\overline{\text{AWCKE}}$ line, which in turn enables the acquire waveform clock generator circuit. In the roll and RD modes, $\overline{\text{AWCKE}}$ is activated for the entire waveform acquisition cycle; in the ERD and ETD modes, it is activated at the beginning of the slow-out phase.

The valid sample clock gate selects either the AWCK (roll and RD modes) or the $\overline{\text{PCK}}$ signal (ERD and ETD modes) to be the valid sample clock ($\overline{\text{VSCK}}$). This clock is used to increment the post-trigger counter. The switching from one source to another for the VSCK is done so that the post-trigger counter counts the samples to be written into the WFM.

The post-trigger counter controls the sequencing of the Time Base in the various time base modes. When a waveform acquistion cycle is initiated, the CCD begins sampling the input signal. The post trigger counter holds off the trigger signal until the data that was in the CCD when the sampling began (old data) has been cleared (clocked through the CCD). When the old data has been cleared, the post-trigger counter enables the trigger and times the post-trigger interval. At the end of the post-trigger interval, it either ends the acquire cycle (roll and RD modes) or activates AWCKE to begin the slow-out phase (ERD and ETD modes)

The end acquire circuit controls the $\overline{\text{ENDACQ}}$ line, which in turn disables the AWCK signal at the end of an acquisition cycle. In the roll and RD modes, the $\overline{\text{ENDACQ}}$ line is activated at the end of the post-trigger interval; in the ERD and ETD modes, $\overline{\text{ENDACQ}}$ is activated following the writing of the samples into the WFM during the slow-out phase.

The fast-in, slow-out (FISO) logic controls the fast-in (FI) and slow-out (SO) lines. These lines control the switching of the Time Base from the fast-in phase to the slow-out phase in the ERD and ETD modes.

The trigger gate input circuit conditions the trigger gates (TGE and $\overline{\text{TGE}}$) from the Trigger board, and produces the trigger gate pulse (TGP) and synchronized trigger gate ($\overline{\text{STG}}$) signals. The TGP signal is used in the ERD mode to synchronize the writing of the first waveform sample into the WFM with the output of that sample from the CCD. $\overline{\text{STG}}$ is used in all time base modes to initiate the loading of the post-trigger count into the post-trigger counter, following the receipt of a valid trigger, and to begin the post-trigger count. The trigger gate input circuit also starts and stops the fast ramp in the ETD mode.

The fast ramp generator generates a negative-going ramp that begins when the trigger gate is received and ends on the falling edge of the $\overline{\text{STG}}$ pulse. This ramp is used in the ETD mode to measure the time between the trigger event and the first sample taken after the trigger. The microprocessor then uses this data to position the samples in the waveform memory with respect to the trigger point to create the composite waveform.

The fast ramp counter measures the time interval of the fast ramp and produces a number proportional to the time between the trigger and the first sample taken. This number is then transmitted back to the microprocessor via the serial data latches.

DETAILED CIRCUIT DESCRIPTION

CLOCK GENERATOR

CLOCK GENERATOR (Self Test 44)

Crystal oscillators U1630 and U1730 provide the basic timing information for the clock generator circuitry. U1630 produces a 16 MHz clock, which decade counter U1520A divides down to 8 MHz and 3.2 MHz. The 8 MHz signal is applied to phase clock multiplexer U1530 and to decade counter U1520B, which divides it down to 4 MHz.

Quad D-Type flip-flop U510 divides the $\overline{\text{3.2 MHz}}$ signal to create clock signals of 1.6MHz, 800kHz and 400kHz (see Fig. 2-28). U510 operates as a state machine. For example, the 1.6MHz output at pin 3 is fed back to the pin 4 input of the flip-flop. On each leading edge of the 3.2MHz signal, the pin 2 output changes state. Note that two phases of the 400kHz clock signal are generated: $\overline{\text{400kHz(1)}}$ and $\overline{\text{400kHz(2)}}$.

These clock signals are used on the Time Base board. Certain of the clock signals are also transmitted to the Memory and Display boards through J110 pins 16A, 16B, 17A, 17B and 18B.

PHASE CLOCK GENERATOR (Self Test 44)

The phase clock generator creates the phase clock signals (PCK and $\overline{\text{PCK}}$), which control the sample rate of the CCD circuitry. Phase clock multiplexer U1530 selects the phase clock rate when SO is low, which occurs in the roll and RD modes, and in the fast-in phase of the ERD and ETD modes. The phase clock multiplexer select (PCKMA, PCKMB and PCKMC) lines select which clock signal is transmitted through U1530 to output pin 5. (The microprocessor controls the state of PCKMA, PCKMB and PCKMC.) In the slow-out phase of the ERD and ETD modes, SO is high, which disables U1530. The 800kHz signal, applied to pin 4 of U1420B, then determines the phase clock rate.

Gates U1100D, U1000B and U1420B control the operation of flip-flop U1220A and thus select the phase

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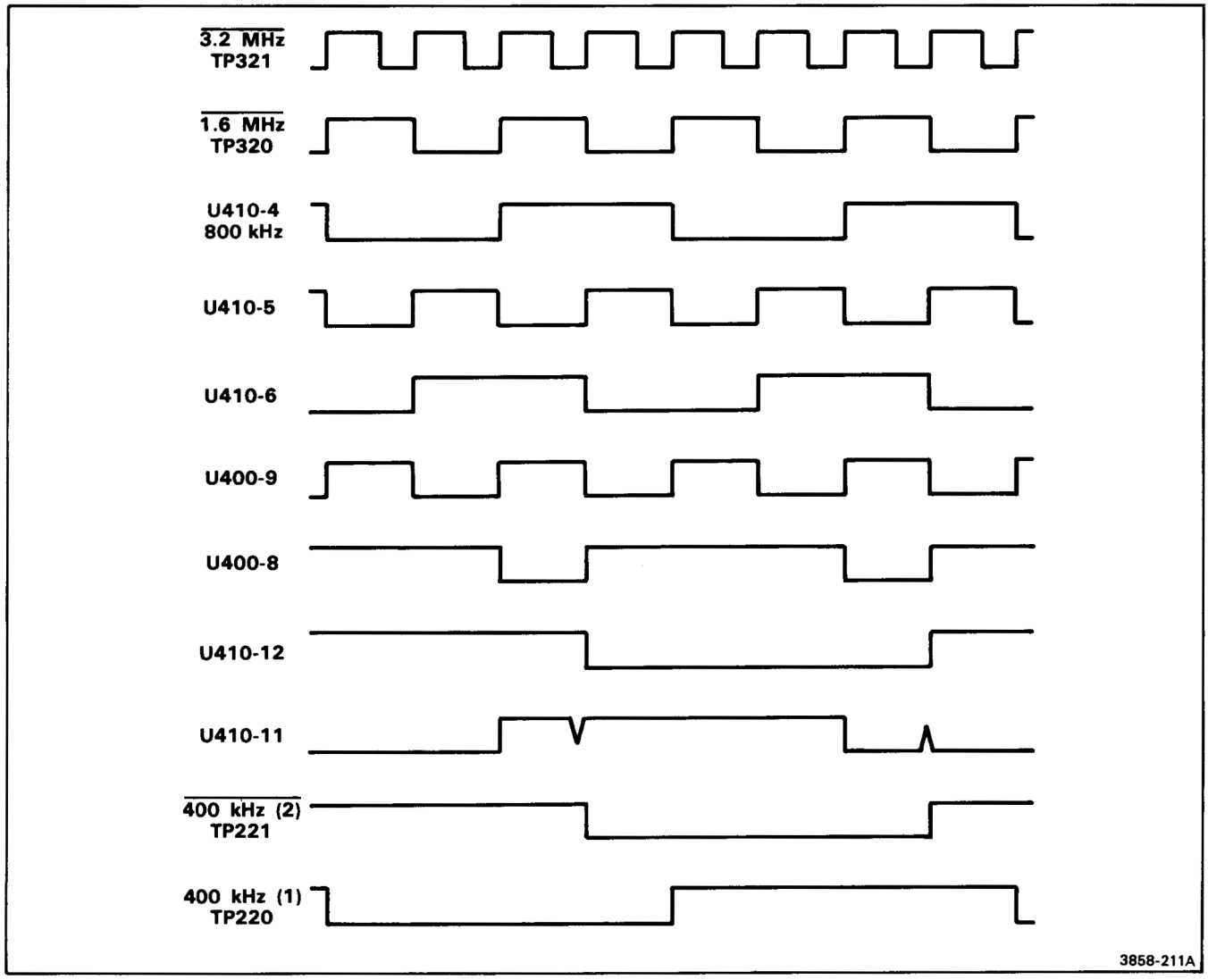

Figure 2-28. Clock generator output signals.

clock generator mode. When the SO and ERD lines are low, the J and K inputs of U1220A are held high. The clock input to U1220A thus toggles the output, causing U1220A to divide the input clock rate by 2 and produce symmetrical PCK and $\overline{\text{PCK}}$. The clock signal in this case comes from U1530. The input strobe (INS) line enables this clock signal to be transmitted through U1420B, when a waveform acquisition cycle is initiated. When SO is low, the PCK rate can then be from 200 kHz to 20 MHz.

There are two slow-out clock rates, which the ERD line controls. When ERD is high (ERD mode), the $\overline{\text{400kHz(2)}}$ signal toggles the J and K inputs to U1220A. The 800kHz clock signal from U1420B is thus divided by 4 to create a 200 kHz phase clock. Since in the ERD mode a sample is provided on each edge of the phase clock, the 200 kHz slow-out rate is required so that the data rate to the waveform memory 400 kHz. When the ERD line is low, the K input is held high and only the J input is toggled. The 800kHz clock signal is then divided by 2 to create a 400 kHz phase clock.

Differential amplifier Q100 and Q101 converts the complementary PCK and $\overline{\text{PCK}}$ signals to ECL logic levels, which which are then applied to the CCD Board and the Trigger Board.

SAMPLE COUNTER (AWCK Generator Self Test 42)

The sample counter circuit counts down the 400kHz(1) signal to create a number of sample clock signals, which are applied to multiplexer U800. These sample clock signals control the rate of the acquire waveform clock (AWCK). AWCK determines which samples from the CCD are written into the waveform memory (WFM).

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Counter U900 provides a ÷1, ÷2 and ÷5 count down of the 400kHz(1) signal depending on the state of the sample clock select lines (SCKB and SCKC). U500A, U500B, U600A and U600B perform a ÷10 and ÷100 function. Multiplexer U800 selects which of the sample clock signals are to be applied to the acquire waveform clock generator circuit, depending on the state of the sample clock multiplexer select lines (SCKMA, SCKMB and SCKMC). The microprocessor sets the SCKB, SCKC, SCKMA, SCKMB and SCKMC lines according to the TIME/DIV setting of the Time Base.

In the Roll and RD modes, U800 transmits one of the signals derived from counting down the 400kHz(1) signal to the acquire waveform clock generator. In the ERD and ERT modes, U800 transmits the 800kHz signal to the acquire waveform clock generator.

START CONVERSION, CH 1/$\overline{\text{CH 2}}$ AND MAGNIFIER CLOCK GENERATORS

Flip-flop U300A generates the 800-kHz start conversion clock (SC)—see Figure 2-29. The SC signal initiates the A to D conversion of the CCD samples (see the description of the CCD output circuitry).

The SC signal in turn clocks flip-flop U300B to create the CH 1/$\overline{\text{CH 2}}$ signal CH 1/$\overline{\text{CH 2}}$ selects which of the two CCD output amplifiers into the A-to-D converter U930 (see the description of the CCD output circuitry.)

Decade counter U810, flip-flop U210B and gate U400B create the magnifier clock (MAGCK). The MAGCK signal is a burst of 10 pulses that occurs following the leading edge of the display clock, which is coincident with the 400kHz(1) signal. Assume that the pin 15 carry output of U810 is low. When the 400kHz(1) signal goes high, the Q output of U210B is set high, enabling U400B. The 8MHz clock signal is then transmitted through U400B to create the MAGCK burst. At the same time, U810 counts the pulses in the burst. When 10 pulses have been counted, pin 15 of U800 is pulled high, toggling the Q210B output low and disabling U400B. When the front-panel HMAG pushbutton is pressed, the MAGCK signal increments the horizontal D-to-A converter in the Display circuitry, which creates the horizontal ramp. By incrementing the D-to-A converter ten times between displayed samples, the display is magnified horizontally by a factor of 10.

EXTERNAL CLOCK

Gates U400A and U410A feed the external clock signal from pin 35A of J110 to sample clock multiplexer U800. Exclusive-OR gate U410A adjusts the polarity of the external clock signal: a high on the EXT CK POLARITY line causes the external clock to be transmitted through U400A and U410A unchanged; a low causes the complement of the external clock signal to be generated.

ACQUIRE WAVEFORM CLOCK GENERATOR

Gates U710A and U710B, and flip-flops U610A and U610B generate the acquire waveform clock (AWCK). When the acquire waveform clock enable ($\overline{\text{AWCKE}}$) line is high, the pin 6 output of U610A is held low, which in turn holds the pin 9 output of U610B low. The circuit is thus disabled. When the $\overline{\text{AWCKE}}$ line is pulled low (see Fig. 2-30), the pin 6 output of U610A is raised on the next sample clock edge from U800. On the next rising edge of the $\overline{\text{400kHz(2)}}$ clock, AWCK is pulled high. AWCK remains high until both the 400kHz(2) and $\overline{\text{400kHz(1)}}$ signals go high and reset the U610B output low. When AWCK and $\overline{\text{400kHz(1)}}$ go high, U710A resets pin 6 of U610A low. U610A is then ready for the next sample clock from U800.

VALID SAMPLE CLOCK GATE

Gate U1420A selects the valid sample clock ($\overline{\text{VSCK}}$) rate. $\overline{\text{VSCK}}$ is either the $\overline{\text{PCK}}$ (ERD and ETD modes) or the AWCK (roll and RD modes), depending on the state of the fast-in, slow-out lines (FISO and $\overline{\text{FISO}}$). The $\overline{\text{VSCK}}$ signal is used to clock the post trigger counter (see following discussion of acquire control circuitry).

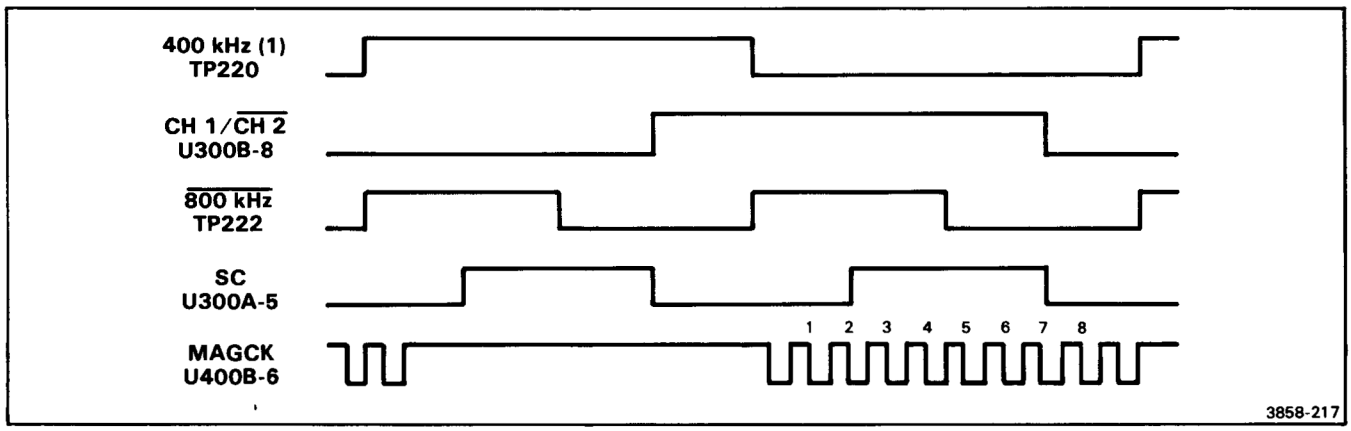

Figure 2-29. Start Conversion (SC), Ch 1/Ch 2 and Magnifier Clock (MAGCK) signal timing.

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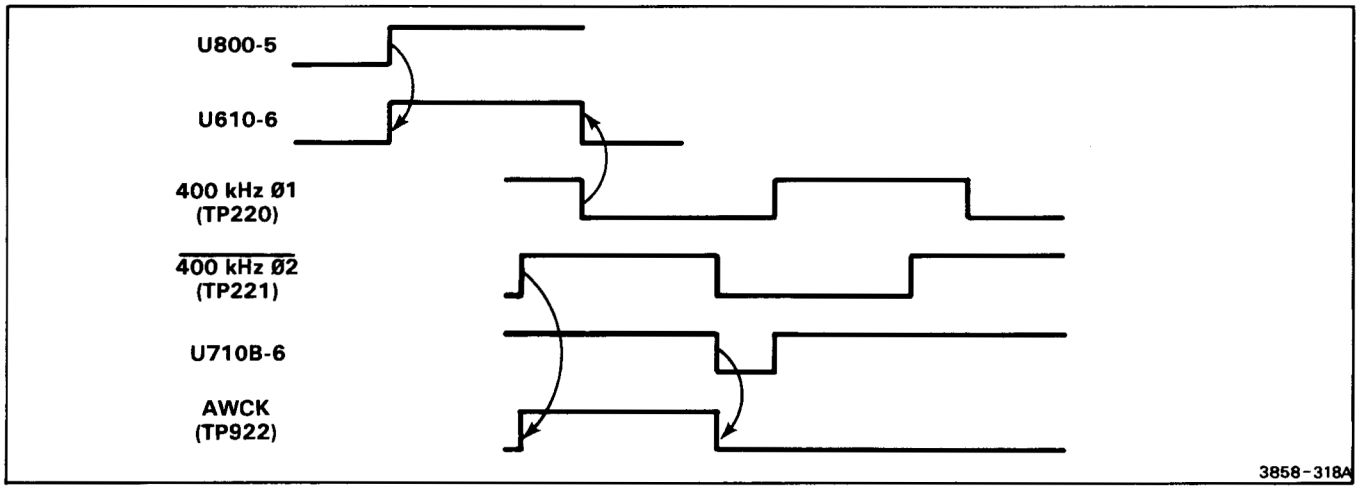

Figure 2-30. Acquire Waveform Clock (AWCK) generator.

15 ACQUIRE CONTROL

SERIAL DATA LATCHES (Self Test 39)

Parallel output 8-bit shift registers U1310, U1510, U1610 and U1710 distribute control and setup data from the microprocessor to the various Time Base circuits. In addition, parallel load 8-bit shift registers U1210 and U1320 transmit data from the Time Base back to the microprocessor.

The six shift registers are configured as a serial, 48-bit shift register. Serial data from the microprocessor is applied through the serial data in (SDI) line to the pin 2 data input of U1710. Serial clock 3 ($\overline{SCK3}$) then clocks the serial data through U1710, U1610, U1510 and U1310. When the serial data strobe (SDS) line is pulled high, the data in each shift register is latched to the output.

A low on the $\overline{GENSELA}$ line causes the state of the $\overline{AWCKE}$, INS, STG, TRIGRST, $\overline{ENDACQ}$, SO and the fast ramp count to be loaded into U1320 and U1210. When $\overline{GENSELA}$ is raised, SCK3 is allowed to clock the data through U1320, U1210 and gate U110E to the serial data out (SDO) line. The serial data is then fed back to the microprocessor via J110 pin 25B for use in self test and for calculating where samples should be placed in the display block of the WFM in the ETD mode.

POST-TRIGGER COUNTER (Self Tests 48 and 43)

Counters U1700, U1600, U1500, U1400 and U1300 form the post-trigger counter. The five counter devices are connected in series. Refer to Figure 2-31. The $\overline{VSCK}$ signal clocks the counters; the initialize ($\overline{INIT}$) line resets the counters to all zeros; and the $\overline{LOAD}$ line loads a preset count into the counters from the microprocessor (via the serial data latches). The preset value is related to the number of samples to be taken following the trigger. The sample counter is set up to overflow at the end of the selected post-trigger interval. The operator selects the post-trigger interval according to the amount of the signal that is to be displayed before and after the trigger. The microprocessor then translates this interval into the proper number of counts, depending on the time/division setting (see the examples in Table 2-12).

The combination of a low on $\overline{GENSELA}$ and a high on address line A4 causes gate U410C, U710C and U1010D to pull the $\overline{INIT}$ line low and initiate a waveform acquisition cycle.

When $\overline{INIT}$ is pulled low (see Fig. 2-32), the sample counter is cleared. It then begins counting from zero. The low on INIT also clears flip-flop U1200A, which sets the end hold off (EHO) line low and the trigger reset (TRIGRST) line high. The EHO and TRIGRST lines are transmitted to other circuits on the Time Base board and to the Trigger board. With the EHO line low and the TRIGRST line high, the trigger circuit is held off. The hold off period lasts for 1024 counts (to clear the CCDs of any previously acquired data). When the sample counter reaches 1024, pin 2 of U1500 is pulled low, which causes EHO to go high and TRIGRST to go low and enable the trigger circuitry.

Prior to the receipt of a trigger, the synchronized trigger gate ($\overline{STG}$) line is high. The high on STG combined with the high on EHO pulls the $\overline{LOAD}$ line low and causes the counter preset value to be loaded into the counter. The $\overline{LOAD}$ line remains low until a valid trigger is obtained, which causes the $\overline{STG}$ line to be pulled low. The counter is then allowed to count $\overline{VSCK}$ pulses. When the counter overflows, pin 12 of U1300 is pulled high. (See the detailed discussion of the Time Base modes for a further explanation of the operation of the post-trigger counter.)

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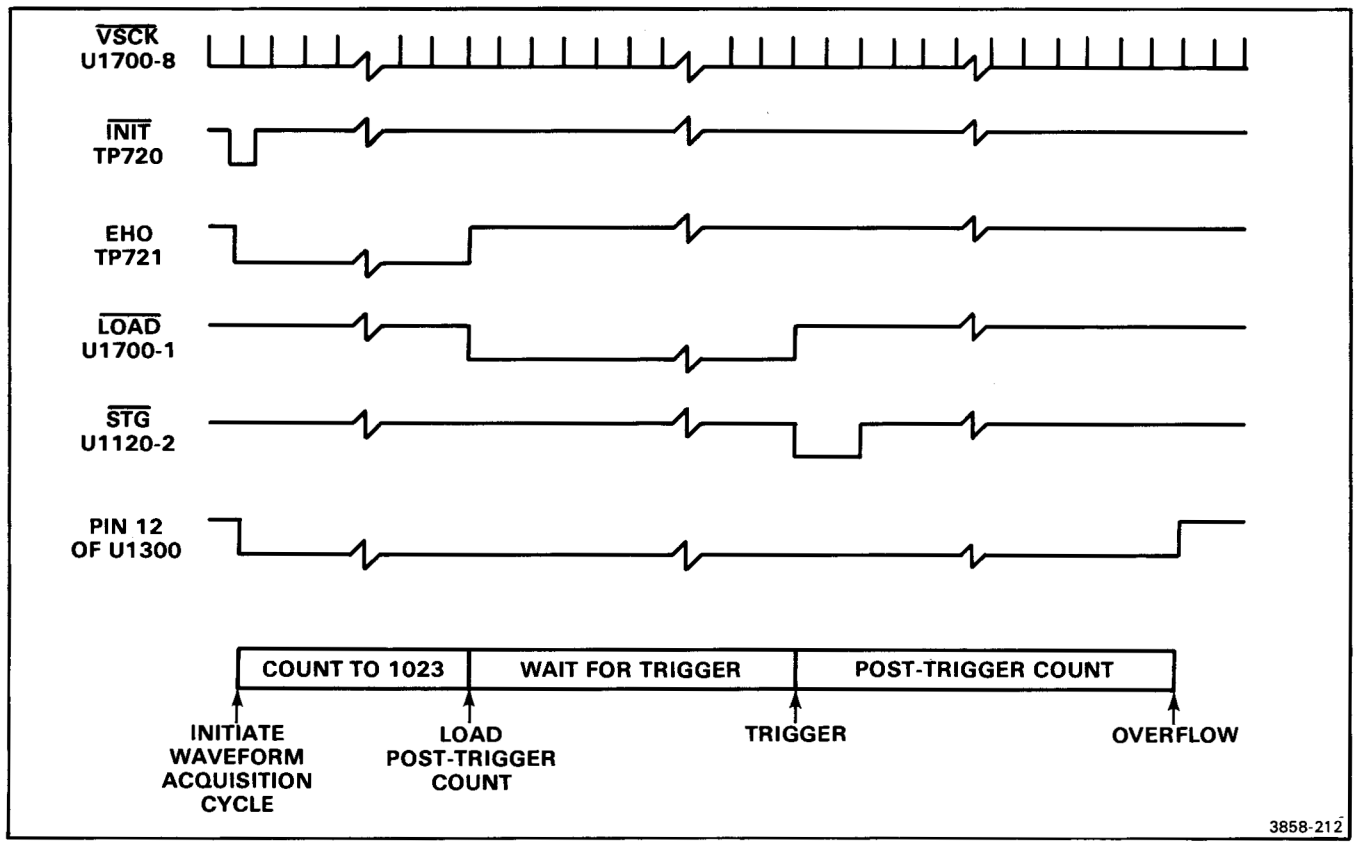

Figure 2-31. Post-trigger counter timing.

END ACQUIRE (Self Test 41)

The end acquire circuit controls the ENDACQ line. Depending on the time base mode, it lowers the line either when the sample counter reaches its maximum value (FISO) or the memory end acquire (MEA) line is pulled high, indicating that the acquire address generator in the Memory circuitry has reached its maximum count.

When the post-trigger counter reaches its maximum value (overflow), pin 12 of U1300 is pulled high. On the next leading edge of PCK at pin 13, the pin 9 output is set high, and pin 7 (which controls the INS line) is set low. In the roll and RD mode (FISO high), the high on pin 2 of U1010A is then transmitted to the J input U910A, causing the ENDACQ line to be lowered.

In the ERD and ETD modes, the low on FISO inhibits the high on pin 9 of U1200B from being applied to U910A. The MEA line from the Memory board then controls the ENDACQ line.

FAST-IN, SLOW-OUT LOGIC (Self Test 43)

Gates U1410F, U1410E and U310D, and flip-flop U910B control the switching of the Time Base from fast-in to slow-out. In the roll and RD modes, the unbuffered fast-in, slow-out (FISOUB) line is held high. U1410F and U1410E then set FISO and FISO to be low and high, respectively. The fast in (FI) line is then held low and the slow out (SO) line is held high for the duration of the waveform acquisition cycle.

In the ERD and ETD modes, FISOUB is held low, causing FISO to high and FISO to be low. When the Time Base is initially loaded with preset data, lows on pins 11 and 12 of U310D then pull FI high. The low on INIT sets SO (pin 9 of U910B) low.

When the post-trigger counter reaches its maximum count, pin 9 of U1200B is set high, which pulls the FI line low. The high on pin 9 of U1200B also pulls the J input to U910B high, which raises the SO line on the next leading edge of 400kHz(2).

ACQUIRE WAVEFORM CLOCK ENABLE

Flip-flops U1220B, and U1000A and U1000C, and gates U1100C and U1100B generate the acquire waveform clock enable signal (AWCKE). The purpose of this signal is to gate the AWCK signal such that the first AWCK pulse produced corresponds to the first sample of the waveform that is to be stored in memory. In the roll and

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TABLE 2-12
Sample Counter Presets

Pin #		U1300				U1400				U1500				U1600				U1700				Count Change Per Div. of TPOS Change
		3	4	10	11	3	4	10	11	3	4	10	11	3	4	10	11	3	4	10	11	
Dec. Value of Preset When High	BIT	2^{18}	2^{16}	2^{17}	2^{19}	2^{14}	2^{12}	2^{13}	2^{15}	2^{10}	2^{8}	2^{9}	2^{11}	2^{6}	2^{4}	2^{5}	2^{7}	2^{2}	2^{0}	2^{1}	2^{3}	
TIME/DIV EXT CK	↑	H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	H	L	L	H	100
20 s		H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	H	L	L	H	100
10 s	R	H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	H	L	L	H	100
5 s	O	H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	H	L	L	H	100
2 s	L	H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	H	L	L	H	100
1 s	L	H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	H	L	L	H	100
500 ms		H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	H	L	L	H	100
200 ms		H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	H	L	L	H	100
100 ms	↓	H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	L	H	H	H	100
50 ms	↑	H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	L	L	H	H	100
20 ms		H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	H	H	H	L	100
10 ms	R	H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	L	H	L	L	100
5 ms	D	H	H	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H	L	100
2 ms		H	H	H	L	H	H	H	H	L	H	H	H	H	H	L	H	H	L	L	L	100
1 ms		H	H	H	L	H	H	H	H	L	H	H	H	L	H	L	H	L	H	H	H	100
500 μs	↓	H	H	H	L	H	H	H	H	L	H	H	H	L	L	H	L	L	L	H	H	100
200 μs	↑	H	H	H	L	H	H	H	H	H	L	H	H	H	H	L	L	H	L	L	L	40
100 μs		H	H	H	L	H	H	H	H	H	L	H	H	H	H	L	L	H	L	L	L	40
50 μs	E	H	H	H	L	H	H	H	H	H	L	H	H	H	H	L	L	H	L	L	L	40
20 μs	R	H	H	H	L	H	H	H	H	H	L	H	H	H	H	L	L	H	L	L	L	40
10 μs	D	H	H	H	L	H	H	H	H	H	L	H	H	H	H	L	L	H	L	L	L	40
5 μs		H	H	H	L	H	H	H	H	H	L	H	H	H	H	L	L	H	L	L	L	40
2 μs	↓	H	H	H	L	H	H	H	H	H	L	H	H	H	H	L	L	H	H	L	L	40
1 μs	↑	H	H	H	L	H	H	H	H	H	L	H	H	H	H	L	L	L	L	L	L	20
500 ns	E	H	H	H	L	H	H	H	H	H	L	H	H	H	L	L	L	H	H	H	H	10
200 ns	T	H	H	H	L	H	H	H	H	H	L	H	H	H	L	L	L	H	L	H	H	4
100 ns	D	H	H	H	L	H	H	H	H	H	L	H	H	H	L	L	L	H	L	H	H	2
50 ns	↓	H	H	H	L	H	H	H	H	H	L	H	H	H	L	L	L	H	L	H	H	1

For Trigger Position = (TPOS) = 0

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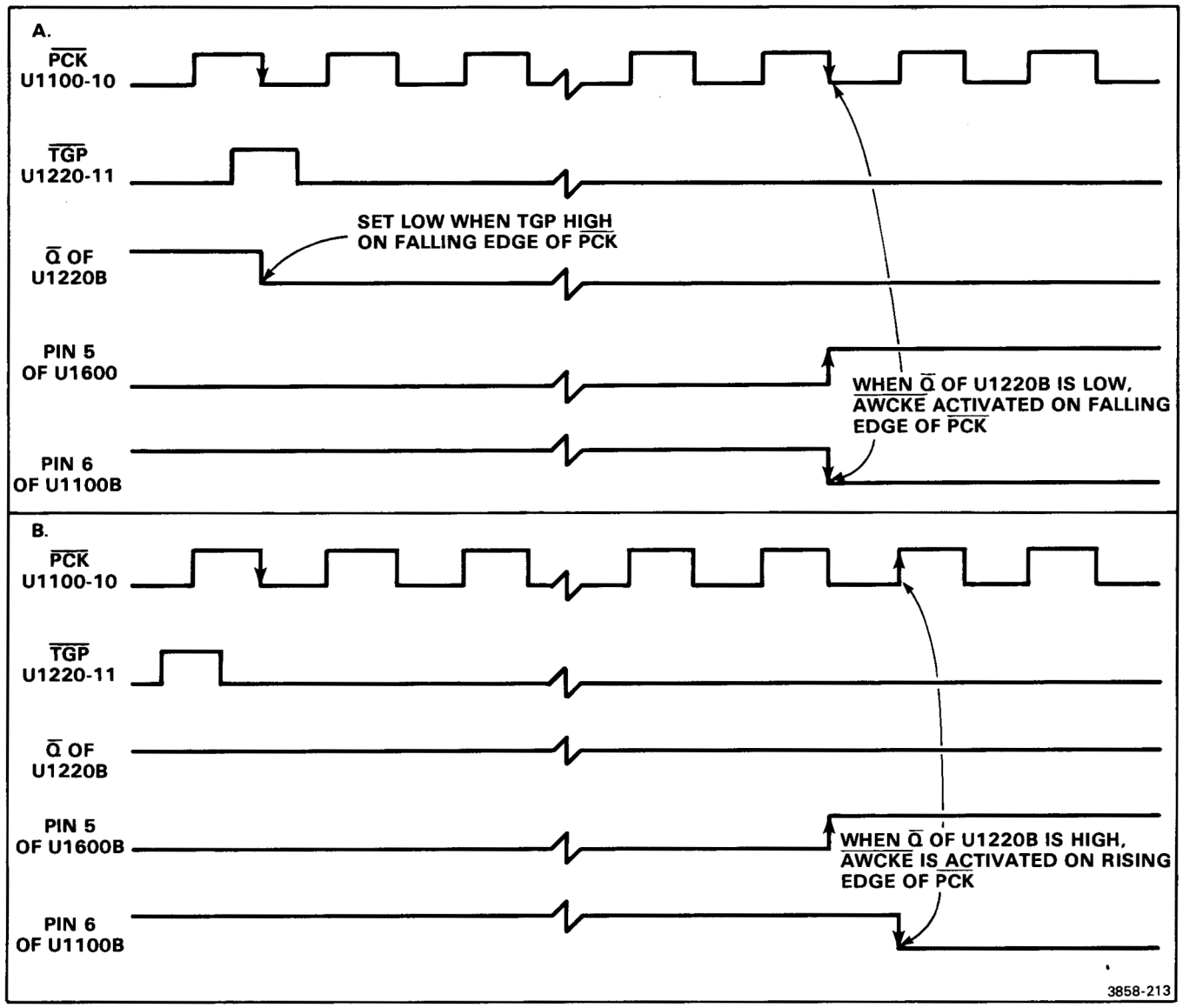

Figure 2-32. Acqurie Waveform Clock Enable (AWCKE) timing: (A) Top active on falling edge of PCKE; (B) Top low on falling edge of PCK.

RD modes, FISO is low, which gives the ENDACQ line control of AWCKE. The low on FISO forces both pin 8 of U1000C and the SO (from U910B-9) high. When the post-trigger counter is initialized, ENDACQ is also set high, which in turn sets AWCKE low, enabling AWCK pulses to be generated. ENDACQ remains high until the post-trigger counter overflows, at which time ENDACQ is pulled low, which in turn pulls AWCKE high and disables the acquire waveform clock generator and terminates the writing of acquired data in the WFM.

In ERD and ETD modes, FISO is high. SO, ENDACQ and pin 6 of U1100B then controls the AWCKE line. When the post-trigger counter is initialized, SO is set low, which holds AWCKE high and inhibits the generation of the AWCK pulses. When the post-trigger counter overflows, SO is pulled high. The state of pin 6 of U1100B then controls the AWCKE line.

In the ETD mode, the ERD line is low. The Q output of U1220B is thus set high when the EHO line goes low during the initialization of the post-trigger counter. When the post-trigger counter overflows, the clock rate changes from fast-in to slow-out (SO goes high). The post-trigger counter then counts to 16 and pulls pin 5 of U1600 high. This combined with the low on PCK causes pin 8 of U1100C to go high, pin 6 of U1100B to go low and pin 8 of U1000C to go low. The resulting high at pin 8 of U1000C pulls AWCKE low and enables the acquire waveform clock generator. Data from the CCD is then written into the WFM until the acquire address generator on the Memory board overflows, pulling the MEA line

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high and in turn pulling $\overline{\text{ENDACQ}}$ low. The low on $\overline{\text{ENDACQ}}$ raises $\overline{\text{AWCKE}}$ and halts the writing of data in the WFM.

In the ERD mode, the ERD line is high. U1220B then determines when pin 8 of U1100C is raised with respect to the $\overline{\text{PCK}}$ signal and thus synchronizes the writing of samples from the CCD with the occurance of the trigger event. In the ERD mode, the two CCD channels sample the signal alternately: channel A samples the signal on the leading edge of $\overline{\text{PCK}}$ and channl B samples the signal on the trailing edge of $\overline{\text{PCK}}$. The CCD thus acquires two samples during each period of the phase clock. Since the post-trigger counter counts PCK periods, however, it may be off by one sample point in indicating when to start writing the data into the WFM. This circuit compensates for the one period resolution of the post-trigger counter and ensures that the trigger point is accurately located on the display.

When the EHO line is low, the Q output of U1220B is set high. U1220B then waits for a trigger pulse. The trigger gate pulse (TGP) is used to determine whether the first sample taken after the trigger event was taken on the leading or the trailing edge of $\overline{\text{PCK}}$. TGP goes high following the trigger and stays high until the $\overline{\text{PCK}}$ signal goes low. Its width thus varies between 10 ns and 60 ns (see the description of the trigger gate input circuit for more details).

If TGP goes high when $\overline{\text{PCK}}$ is low (see Fig. 2-32), pin 7 of U1220B is then set low when $\overline{\text{PCK}}$ goes high; if TGP goes high when $\overline{\text{PCK}}$ is high, pin 7 of U1220B remains high when $\overline{\text{PCK}}$ goes high.

When the post-trigger counter overflows, then counts to 16, the state of pin 7 of U1220B determines whether $\overline{\text{AWCKE}}$ is activated on the leading edge of $\overline{\text{PCK}}$ ($\overline{\text{Q}}$ is high) or on the falling edge ($\overline{\text{Q}}$ is low).

When all the samples in the CCDs have been written into the WFM, MEA is pulled high, which activates ENDACQ and raises AWCKE.

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FAST RAMP TIME INTERPOLATOR

TRIGGER GATE INPUT (Self Test 51)

Differential amplifier Q221, Q220, Q620 and Q520 receive complementary ECL level trigger gates (TGE and $\overline{\text{TGE}}$) from the Trigger Board (P110 pin 10A and 10B). Q221 converts these gates into a TTL level trigger gate, which is applied to pin 10 of U1010C.

When a waveform acquisition cycle is initiated, EHO (pin 15 of U1130A and pin 14 of U1130B) is initially set low, which holds the Q outputs of U1130A and U1130B low. (Flip-flop U1030A is used for self test. For normal operation, the end down ramp ($\overline{\text{EDRD}}$) line is high, which sets the Q output of U1030A high. See the following discussion of the fast ramp self test circuit.) When the post-trigger counter has counted to 1023, EHO is set high, which removes the forced reset to U1220B.

When a trigger is received, pin 10 of U1010C is raised, which pulls the J input of U1130A high. On the next phase clock, the Q output of U1130A goes high. The high at pin 4 of U1010B is transmitted through U1010B to the J input of U1130B. On the next phase clock, the Q output of U1130B is set high. The $\overline{\text{Q}}$ output controls the synchronized trigger gate ($\overline{\text{STG}}$), which starts the post-trigger counter and halts the fast ramp.

The low on the $\overline{\text{Q}}$ output of U1130A pulls pin 9 of U1010C low, which terminates the high on TGP. The low on $\overline{\text{Q}}$ also pulls the TRIG'D line high. The TRIG'D line is connected to the MPU board, where the microprocessor uses it in all time base modes to determine when the front-panel TRIG'D LED should be lit. Also, in the ETD mode, the high on the TRIG'D line indicates that fast ramp data is ready to be read through the self test latches.

FAST RAMP SELF TEST

The fast ramp self test flip-flop (U1030A) adds one phase clock cycle delay between the trigger and the $\overline{\text{STG}}$ pulse when activated for calibration and self test purposes. When $\overline{\text{EDRD}}$ is high, the Q output of U1030A is set high. The Q output of U1130A thus bypasses U1030A and is transmitted unchanged through U1010B.

When $\overline{\text{EDRD}}$ goes low during the fast ramp circuit self test, the preset to U1030A is removed and its Q output is set low. When the Q output of U1130A goes high, it sets the J input of U1030A high. On the next phase clock, the Q output of U1030A then goes high and pulls the J input to U1130B high. An additional phase clock cycle is thus inserted between the trigger and STG.

FAST RAMP GENERATOR (Self Test 51)

The fast ramp generator is used only in the ETD mode to measure the time between the trigger event and the next waveform sample that the CCD takes after the trigger. Since the trigger and the phase clock are asynchronous, the time between the trigger and the first sample varies between 0 and 50 ns. A ramp (called the fast ramp) with a slew rate of 52 V/μs is used to measure this trigger-to-sample interval to within 1% in the fastest time/division setting.

Immediately following the receipt of a trigger, the fast ramp starts going negative from a fixed baseline level. It continues down until the second sample following the trigger has been taken. The fast ramp is thus allowed to

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run at least 50 ns to allow start-up non-linearities to end. When the second sample is taken, the ramp is stopped and allowed to slew back up (this time at a much slower rate) until it passes through a preset threshold level. The slew rate ratio of the fast ramp to the up-ramp is fixed at 200. By measuring the time duration of the up-ramp, the time interval between the trigger and the first sample can thus be calculated. The microprocessor performs this calculation.

The fast ramp generator consists of an integrator, a constant current source, a switchable current source and a switchable current sink (see Fig. 2-33). Prior to the receipt of a trigger, the switchable current source in combination with the switchable current sink and the integrator act as a baseline stablizer to set the starting point of the fast ramp. When the trigger occurs, the switchable current source is turned off. The ramp then begins going negative from a baseline level of approximately 2.5 V. The difference between the constant current source and the switchable current sink determines the fast ramp rate. The current sink conducts about 201 times more current than the constant current source, so the ramp goes negatve. It continues ramping down until $\overline{\text{STG}}$ goes low, which switches off the current sink. This leaves only the constant current source on, which starts the ramp positive, but at about $1/200^{\text{th}}$ the rate at which it went down. As it ramps up, a counter is incremented to count the time between the beginning of the up ramp and the point when the ramp passes through the threshold of the comparator, which stops the counter. The count is then loaded into the serial data latches and transmitted to the microprocessor.

Transistors Q620 and Q520 make up a switchable current source. In the quiescent state of the circuit (awaiting a trigger gate), TGE is at approximately 4 V and $\overline{\text{TGE}}$ is at 5V, which holds Q520 on and Q620 off. Approximately 20 mA of current is then conducted through R721 and Q520 to the emitters of Q521 and Q621, where it is split between the two transistors.

Transistors Q521 and Q621 form a comparator, with Q621 conducting just enough current to hold the source of FET voltage follower Q630 at the same level as the base of Q521. This level constitutes the baseline level for the fast ramp.

Operational amplifier U430A and Q530 make up the constant current source, which supplies approximately 5 μA of current in the current node.

Operational amplifier U430B, and Q531 and Q532, constitute a switchable current sink. In the quiescent state ($\overline{\text{STG}}$ is high), Q533 is off, and Q531 and Q532 sink approximately 10 mA from the current node. The Ramp Gain adjustment (R320) sets the ratio of the 5 μA current source and the 10 mA current sink so that the fast ramp falls 200 times faster than the up-ramp rises.

When a trigger is received, Q520 is turned off and Q620 is turned on, switching off the baseline current source. The voltage across the timing capacitor (C520) then begins ramping down as C520 discharges into the current sink.

C520 continues to discharge until the STG line goes low and turns on Q533. When Q533 turns on, it reverse-biases Q531 and Q532, switching off the 10 mA current sink. The 5 μA constant current source then begins charging C520, but at a slower rate than the discharge rate.

Comparator U830 senses the voltage at the source of Q630. The Ramp Offset adjustment (R732) sets the threshold level of U830 to a voltage below the ramp baseline level. U830 then switches its output high when the ramp goes above this threshold level, which in turn pulls the pin 10 input of counter U1620 low.

TGE and $\overline{\text{TGE}}$ remain active until the end of the acquisition cycle. When TGE goes low and $\overline{\text{TGE}}$ high at the beginning of the next acquisition cycle, the fast ramp generator is reset to its baseline level.

FAST RAMP COUNTER (Self Test 51)

The fast ramp counter consists of counters U1620, U1110A and U1110B. U1620 gates the 40 MHz clock and counts it down to 10 MHz. U1110A and U1110B in turn count the 10 MHz clock. At the start of the acquisition cycle, TRIGRST clears U1110A and U1110B. When $\overline{\text{STG}}$ goes low (at the beginning of the up-ramp) the Q output of U1130B enables U1620, allowing U1110B and U1110A to begin counting. They count until the up-ramp reaches the threshold level of U830 at which time pin 10 of U1620 goes low, halting the counting. Ramp Offset adjustment R732 adjusts the threshold level of U830, allowing a small adjustment in the time when the counter stops. This adjustable offset in the count varies the location in WFM where the acquired data is stored, which allows the trigger position to be aligned with the crt graticule and compensates for delays in the analog circuitry.

The additional clock cycle increases the down ramp time. By asserting $\overline{\text{EDRD}}$ on alternate acquire cycles the fast ramp length is forced to have a 50 ns variation (one clock cycle) which is translated during the up ramp internal to a time which the microprocessor reads and checks to be within limits. During this test triggering is off PCK and $\overline{\text{PCK}}$ which is synchronous with the clocking of U1130A and U1030A.

The microprocessor then latches the count at the outputs of U1110A and U1110B into the serial data latches, and reads it through the SDO line.

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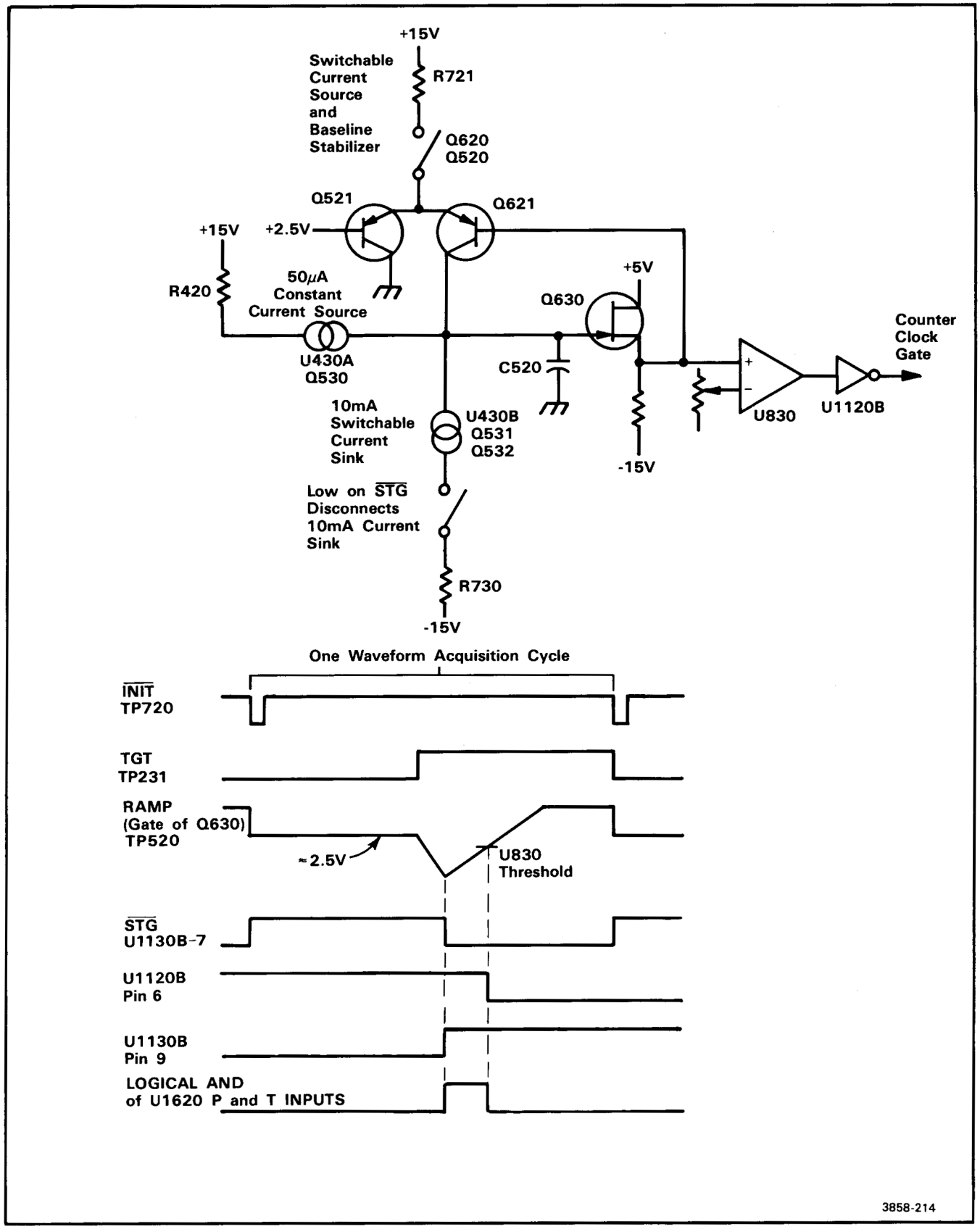

Figure 2-33. Simplified schematic of fast ramp generator.

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DETAILED DESCRIPTION OF TIME BASE MODES

This portion describes the sequence of events that occur within the Time Base circuitry from the time that the microprocessor initiates an acquisition cycle to the end of the cycle, for each time base mode.

Roll Mode

When the TIME/DIV switch is set to one of the roll mode positions (EXT CK OR 20 s/div to 100 ms/div), the microprocessor shifts time base setup data into the serial data latches. The phase clock is set to 400 kHz (for all roll mode TIME/DIV switch settings). The sample counter, which determines the frequency of the AWCK signal and thus the effective sampling rate of the 7D20 in the roll and RD modes, is set for an interval determined by the TIME/DIV setting (see Table 2-11). The FISO line is set low, which causes the AWCK signal to be transmitted through gate U1420A to produce the $\overline{\text{VSCK}}$ signal. The low on FISO also sets FI low and SO high.

Once the time base setup parameters have been latched, the microprocessor pulls $\overline{\text{GENSELA}}$ low and A4 high to initiate the waveform acquisition cycle. The resulting low on $\overline{\text{INIT}}$ clears the post-trigger counter to zero, and sets $\overline{\text{ENDACQ}}$ high, EHO low and TRIGRST high. With $\overline{\text{ENDACQ}}$ and SO high, and FISO low, $\overline{\text{AWCKE}}$ is low, enabling the acquire waveform clock generator to produce AWCK pulses.

When the acquisition cycle is initiated (and SO is pulled high), the phase clock signal begins clocking the two CCD channels and the post-trigger counter begins counting $\overline{\text{VSCK}}$ pulses. The two CCD channels sample the input signal differentially on the leading edge of the PCK signal, and apply the signal samples at the output of the CCD to the A-to-D converter. The resulting digitized signal samples are applied to the Memory board.

The sample counter then selects which of these samples are to be stored in the WFM by controlling how often the AWCK pulse is generated with respect to the phase clock pulses (see Table 2-11).

The samples are stored in a 1K section of the WFM in the order in which they are received. For example, the first sample is stored at WFM address 0, the second sample at address 1, etc. When the 1024th sample has been stored, the WFM wraps around and stores the 1025th sample at address 0. As more waveform points are acquired (sampled, digitized and written into the WFM), old data within the 1K block of the WFM is overwritten so that only the most recently acquired 1024 samples are kept. For each new sample acquired, between successive display address generator (located on the Memory Board) starting address is incremented by one, which creates the illusion on the crt of a strip chart recorder.

When the acquire cycle is initiated, the post-trigger counter begins counting $\overline{\text{VSCK}}$ pulses. Upon reaching 1023, the EHO line is raised, which pulls $\overline{\text{LOAD}}$ low and causes the post-trigger count to be loaded in the post-trigger counter. $\overline{\text{LOAD}}$ remains low (inhibiting the counter) until a trigger is received, causing the STG line to be pulled low. $\overline{\text{LOAD}}$ then goes high and the post-trigger count begins.

In the continuous roll mode, the microprocessor periodically reinitializes the post-trigger counter by pulsing INIT which keeps EHO low so that it is never allowed to overflow. The acquisition cycle is thus continuous.

When the front-panel HOLD NEXT pushbutton is pressed, the microprocessor loads the post-trigger counter with the count required to produce the post-trigger interval that the operator has selected. When a trigger event occurs, the post-trigger counter is allowed to count to overflow. The $\overline{\text{ENDACQ}}$ line is then pulled low, causing $\overline{\text{AWCKE}}$ to be raised and the AWCK pulses to be inhibited. The waveform within the window set by the post trigger-interval is thus held in the WFM.

REAL-TIME DIGITIZING MODE

When the TIME/DIV switch is set to one of the real-time digitizing (RD) modes (50 ms/division to 500 μs/division), the microprocessor sets up the Time Base for signal acquisition and storage in the same manner as described for the roll mode. The phase clock is set to sample the signal at a 400-kHz rate and the AWCK signal selects which of these samples are to be stored in the WFM according to the setting of the sample counter (see Table 2-11).

The samples are stored in the WFM in the same manner as in the roll mode, with the acquire address generator wrapping around each time the 1K of WFM is filled. The Display circuitry does not scan the WFM, however, until a complete waveform has been acquired.

When the post-trigger counter begins counting following the initialization of the Time Base, it counts from 0 to 1023 (to clear the CCD and WFM of old data), then raises the EHO line to end trigger hold-off. The high on EHO pulls $\overline{\text{LOAD}}$ low and causes the post-trigger counter to be loaded with the post-trigger count. $\overline{\text{LOAD}}$ remains low (inhibiting the counter) until a trigger is received. The trigger pulls the $\overline{\text{STG}}$ line low, which in turn raises $\overline{\text{LOAD}}$ and allows the post-trigger counter to begin counting from the preset value.

When the counter overflows, $\overline{\text{ENDACQ}}$ is pulled low, which raises $\overline{\text{AWCKE}}$. The acquire waveform clock generator is thus disabled, halting the writing of the waveform samples into the WFM. The microprocessor polls the $\overline{\text{ENDACQ}}$ line. When $\overline{\text{ENDACQ}}$ goes low, the microprocessor reads the address at the acquire address

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generator output, and uses it to set the start address for the display address generator.

While the Display circuitry is scanning the WFM and displaying the acquired waveform, the microprocessor activates GENSELA and A4, which resets the Time Base and begins another acquisition cycle. The waveform data acquired during this cycle is stored in another 1K block of the WFM. When the second waveform has been acquired, the Display circuitry begins scanning it while another waveform is acquired and stored in the first 1K block of WFM. The Time Base continues in this manner, switching back and forth between the two 1K blocks of memory, until either the TIME/DIV setting is changed or the HOLD or HOLD NEXT pushbutton pressed.

EXTENDED REAL-TIME DIGITIZING

The extended real-time (ERD) digitizing mode (200 μs through 2 μs) is a fast-in, slow-out mode. As with the other Time Base modes, when the TIME/DIV switch is set to one of the extended real time digitizing positions, Time Base set up information is latched into the serial data latches.

In this mode, the phase clock is set to a rate from 200 kHz to 20 MHz, depending on the horizontal sweep rate selected (see Table 2-11). With FISO high, the PCK is also used to produce the VSCK signal.

The sample clock multiplexer (U800) transmits the 800kHz signal to the acquire waveform clock generator. At the beginning of the acquisition cycle, the high on FISO also forces SO low, which in turn holds AWCKE high and inhibits the generation of AWCK pulses. When the acquire waveform clock generator circuit is enabled at the beginning of the slow-out phase of the acquisition cycle, it divides the 800kHz clock by two and synchronizes it with the Memory timing signals to produce the 400kHz AWCK signal.

Having latched the Time Base setup parameters, the microprocessor activates GENSELA and A4 to initiate the waveform acquisition cycle. The resulting low on INIT sets ENDACQ and EHO high, and TRIGRST low. The high on FISO also disables gate U1010A. The MEA line from the Memory board thus controls the ENDACQ line in the ERD mode. The low at pin 9 of U1200B combined with a high on FISO sets FI high. The low on INIT also clears the post-trigger counter to zero.

When the acquire cycle is initiated, the phase clock signal begins clocking the CCDs and the post-trigger counter begins counting VSCK clock pulses. The two CCD channels take alternate samples of the input signal in this mode (see discussion of CCD circuitry). Since the acquire waveform clock generator is not enabled at this time, the samples that pass through the CCDs are not written into the WFM.

While the CCDs are sampling the input signal, the post-trigger counter counts from 0 to 1023, then raises the EHO line to load the post-trigger counter and enable the trigger circuit (see the discussion of the RD mode). When a trigger is received, STG is lowered, which pulls LOAD high and allows the post-trigger counter to begin counting from the preset value. When the counter overflows (U1300 pin 12 goes high), the SO line is pulled high and the FI line is pulled low. The high on SO enables the acquire waveform enable flip-flop (U100A and U1000C) to pull the AWCKE line low when a low is received from pin 6 of U1100B (see the discussion of the acquire waveform clock enable circuit).

When SO goes high, the phase clock is reset for a 200 kHz rate. The Time Base is now in the slow-out phase of the acquisition cycle. Only the last 820 samples taken are used in this mode. The post-trigger count is set to move these samples to within 16 counts of the end of the CCD before overflow occurs. When the slow-out phase begins, the post-trigger counter counts 16 more VSCK signals to move the valid sample to the end of the CCDs. When the post-trigger counter reaches 16, pin 6 of U1100B is pulled low, which pulls AWCKE low, enabling AWCK pulses to be generated.

With the AWCK signal now being generated, the samples at the outputs of the two CCD channels are applied to the A-to-D converter. The resulting digitized signals are then written into a 1K block of WFM. The acquire address generator in the Memory circuitry causes the waveform to be stored in the WFM beginning with address 200. When the acquire address generator reaches its overflow count, the MEA line is pulled high, which in turn pulls ENDACQ low and AWCKE high to halt the writing of waveform data into the WFM. Although 824 samples are written into the WFM, only 820 are displayed. The Display circuitry then scans the newly acquired waveform and displays it on the crt.

While the Display is scanning this section of the WFM, the microprocessor activates GENSELA and A4 to initiate another acquisition cycle. As with the RD mode, this waveform is then stored in a second 1K block of the WFM, and when the storage of the second waveform is complete, the Display begins scanning this block of WFM. The Memory and Display circuitry switches back and forth between these two blocks of memory as additional waveforms are acquired.

EQUIVALENT TIME DIGITIZING

The equivalent time digitizing (ETD) mode (1 μs/division to 50 ns/division) is also a fast-in, slow-out mode. When the TIME/DIV switch is set to one of the ETD positions, the Time Base is set up in the same manner as is described for the ERD mode.

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When the acquisition cycle is initiated, the phase clock signal begins clocking the CCD and the post-trigger counter begins counting $\overline{\text{VSCK}}$ pulses. The two CCD channels sample the input signal differentially as in the roll and RD modes. In this case, however, only a few samples are taken for each acquisition cycle: from 10 to 205 depending on the TIME/DIV setting.

When the post-trigger counter has initially counted to 1023 and loaded the post-trigger count, it waits for a valid trigger. When the trigger is received, $\overline{\text{STG}}$ is lowered and the post-trigger counter begins counting. When the post-trigger counter overflows, the SO line is pulled high and the FI line low, eginning the slow-out phase of the acquisition cycle. The phase clock rate is switched to 400kHz and 16 more samples are taken at which time $\overline{\text{AWCKE}}$ is lowered, which in turn allows AWCK pulses to be generated.

The number of valid samples in the CCD varies in the ETD mode depending on the selected horizontal sweep rate. The microprocessor, however, sets the post-trigger counter such that the valid samples are moved to within 16 samples from the end of the CCD when the counter overflows. The post-trigger counter then counts 16 counts in the slow-out mode before AWCKE is pulled low to enable the acquire waveform clock generator. The acquire waveform clock generator thus begins producing AWCK pulses just as the valid samples reach the end of the CCD. The samples are then read into a 1K block of the WFM, the MEA line goes high and the waveform acquisition cycle is ended.

When the trigger event occurs, the fast ramp signal begins ramping down. It stops on the occurrence of the second phase clock after the trigger event (see discussion of fast ramp circuit). The fast ramp counter circuit then measures the time interval as the ramp runs up and converts this interval into the FAST RAMP count. The microprocessor reads the FAST RAMP count from the serial data latches. It then uses this count to offset the samples taken with respect to the trigger event in the process of creating the composite waveform.

To create the composite waveform, the microprocessor copies each sample from the 1K acquire block of WFM into a second 1K display block of the WFM. It stores the sample in the display block in the proper time relationship with respect to the trigger event (using the fast ramp data) and with respect to the resolution of the final waveform (if 100 samples of the signal were taken, then microprocessor would put the samples 10 WFM locations apart in the display block of the WFM).

The microprocessor then initiates another waveform acquisition cycle, stores the acquired samples in the acquire block of WFM, then transfers them to the display block. It continues this process until a complete composite waveform has been constructed. The number of acquisition cycles required to reconstruct the waveform depends on the sweep rate selected. Less samples are taken per cycle in the higher sweep rates and thus more waveform acquisition cycles are required to create the composite waveform.

The Display circuitry scans the display section of the WFM and displays the composite waveform on the crt.

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MAINTENANCE

This section contains information for performing preventive maintenance, troubleshooting, corrective maintenance, and testing and diagnostics for the 7D20 Programmable Digitizer. All support related items mentioned in this manual are listed in Table 3-1.

PREVENTIVE MAINTENANCE

Preventive maintenance, when performed on a regular basis, can prevent or forestall instrument breakdown and may improve instrument reliability. The severity of the environment to which the instrument is subjected determines the frequency of maintenance. A convenient time to perform preventive maintenance is preceding electrical adjustment of the instrument.

PLUG-IN PANEL REMOVAL

WARNING

To prevent personal injury or instrument damage, disconnect the 7D20 from the power source before cleaning or replacing parts.

The side panels, top-and-bottom frame rails and front panel reduce radiation of electromagnetic interference from the instrument. The side panels are held in place by grooves in the frame rails. To remove a panel, pry out with fingers, beginning at the rear of the appropriate side cover. To install a cover, position it over the frame rail grooves, then press down with fingers until the cover snaps into place. Pressure must be exerted all along the rails to secure the panel.

NOTE

The 7D20 will not slide into the mainframe if the side panels have been improperly installed (not firmly seated in the rails).

CLEANING

The 7D20 should be cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket and prevents efficient heat dissipation. It also provides an electrical conduction path that can result in instrument failure.

NOTE

The cabinet panels of the mainframe in which the 7D20 is installed reduces the amount of dust reaching the the interior of the instrument. Operation without the panels in place necessitates more frequent cleaning.

CAUTION

Avoid the use of chemical cleaning agents which might damage the materials used in this instrument. Use only Isopropyl alcohol or totally denatured ethyl alcohol. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

EXTERIOR

Loose dust accumulated on the outside of the instrument can be removed with a soft cloth or small brush. The brush is particularly useful for dislodging dirt in and around the side-panel ventilation holes and front-panel switches.

NOTE

Remove the side panels before cleaning them.

INTERIOR

Cleaning the interior of the instrument should only be occasionally necessary. The best way to clean the interior is to blow off the accumulated dust with dry, low-velocity air (approximately 5 lb/in^2). Remove any dirt that remains with a soft brush or a cloth dampened with a mild solution of detergent and water. A cotton-tipped applicator is useful for cleaning in narrow spaces, or for cleaning more delicate circuit components.

CAUTION

Circuit boards and components must be dry before applying power to prevent damage from electrical shorts.

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TABLE 3-1
Part Number Reference For Support Items

Purpose	Item	Quantity Required	Location
OPTIONAL ACCESSORIES Internal GPIB Cable for use with R7603 Option 20	Tektronix Part 020-0903-00.	1	Section 1 General Information "OPTIONAL ACCESSORIES"
LUBRICANT FOR THE TIME/DIV PANCAKE SWITCH	Contact lubricant-cleaner	1 container	Section 3 Maintenance "LUBRICATION"
	Silicone grease, Tektronix Part 006-1353-00	1 tube	
DISCHARGE STATIC VOLTAGE TO PREVENT DAMAGE OF STATIC-SENSITIVE COMPONENTS	Static Control Mat, Tektronix Part 006-3414-00.	1	"STATIC-SENSITIVE DEVICE CLASSIFICATION"
	Wrist strap, Tektronix Part 006-3415-00.	1	
TEST EQUIPMENT FOR GENERAL TROUBLESHOOTING	TEKTRONIX 577/177 Curve Tracer. TEKTRONIX 576 Curve Tracer. TEKTRONIX 7CT1N Curve Tracer Plug-in unit and a 7000-series oscilloscope. TEKTRONIX 5CT1N Curve Tracer Plug-in unit and a 5000-series oscilloscope.	1	"TROUBLESHOOTING EQUIPMENT"
	TEKTRONIX DM501A Digital Multimeter	1	
	TEKTRONIX 067-1051-00 Extender (board).	1	
	TEKTRONIX 067-0616-00 Extender.	3	
	TEKTRONIX 067-1090-00 Signature Analyzer. SONY/TEKTRONIX 308 Data Analyzer.	1	
INTEGRATED CIRCUIT EXTRACTING TOOL	Tektronix Part 003-0619-00.	1	"COMPONENT REMOVAL AND REPLACEMENT"
CIRCUIT BOARD REMOVAL TOOLS	#1 Philips screwdriver.	1	"CIRCUIT BOARDS"
	#2 Philips screwdriver.	1	
	1/4-inch nutdriver.	1	
	1/4-inch open-end or box-end wrench.	1	
	5/16-inch nutdriver.	1	
	1/16-inch Allen wrench.	1	
	Needle-nose pliers.	1	
	3/16-inch nutdriver.	1	
	small straight-slot screwdriver.	1	

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TABLE 3-1 (CONT)
Part Number Reference For Support Items

Purpose	Item	Quantity Required	Location
REPLACEMENT KIT FOR CIRCUIT-BOARD PINS	Tektronix Part 040-0542-01	1	"CIRCUIT-BOARD PINS"
CHECK GPIB TRANSFER CAPABILITY	TEKTRONIX 4051 Desktop Computer	1	"FUNCTIONAL CHECK PROCEDURE"
TEST EQUIPMENT FOR CHECKS AND ADJUSTMENT PROCEDURES	Refer to Table 4-2, Test Equipment.		Section 4 Checks and Adjustment "TABLE 4-2, TEST EQUIPMENT"
STANDARD ACCESSORIES	Service Manual	1	Refer to "Tabbed" Accessories page at the rear of this manual.
	Operators Manual	1	

LUBRICATION

Generally, there are no parts in this instrument that require a regular lubrication program during the life of the instrument.

PANCAKE SWITCH LUBRICATION

In most cases, factory lubrication should be adequate for the life of the instrument. However, if the switch has been disassembled for replacement of switch sub-parts, it can be lubricated as follows:

- Lubricate the contact surfaces on the circuit board(s) with a thin coat of contact lubricant-cleaner.

- Lubricate the outer surface of the contact carrier with silicone grease (Tektronix Part 006-1353-00). Be careful not to get this lubricant on the contacts.

The lubricants mentioned are available through any Tektronix Field Office.

VISUAL INSPECTION

The 7D20 should be inspected occasionally for loosely seated semiconductors or heat-damaged parts. The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged parts are found. Overheating usually indicates other trouble in the instrument; therefore, correcting the cause of overheating is important to prevent recurrence of the damage.

SEMICONDUCTOR CHECKS

Periodic checks of semiconductors are not recommended. The best check of semiconductor performance is actual operation in the instrument. More details on semiconductors are given under Troubleshooting later in this section.

ELECTRICAL ADJUSTMENT

To ensure accurate measurements, check the electrical adjustment of this instrument after each 2000 hours of operation, or annually if used infrequently. In addition, replacement of components may necessitate adjustment of the affected circuits. Complete adjustment instructions are given in Section 4, Checks and Adjustment. This procedure can be helpful in localizing certain troubles in the instrument, and in some cases, may correct them.

ADJUSTMENT AFTER REPAIR

After any electrical component has been replaced, the adjustment of that particular circuit should be checked, as well as the adjustment of other closely related circuits. The Performance Check procedure in Section 4, Checks and Adjustments, provides a quick and convenient means of checking instrument operation. In some cases, minor troubles may be revealed or corrected by adjustment.

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TROUBLESHOOTING

The following information is provided to facilitate troubleshooting of the 7D20 Programmable Digitizer. Information contained in other sections of this manual should be used in conjunction with the following data to aid in locating a defective component. An understanding of the circuit operation is helpful in locating troubles. See Section 2, Theory of Operation, for this information.

TROUBLESHOOTING AIDS

DIAGRAMS

Complete schematic diagrams are given on the foldout pages in Section 7, Diagrams and Circuit Board Illustrations. The circuit number and electrical value of each component in this instrument is shown on these diagrams. (See the first page of the Diagrams and Circuit Board Illustrations section for definitions of the reference designators and symbols used to identify components in this instrument.) Important voltages are also shown on some diagrams. The portions of circuits mounted on circuit boards are enclosed with heavy, solid-black lines. Each schematic diagram is divided into functional stage blocks, as indicated by the wide shaded lines. These functional blocks are described in detail in Section 2, Theory of Operation.

CIRCUIT BOARD ILLUSTRATIONS

To aid in locating circuit boards, an illustration showing the circuit board location appears on the back of the foldout page facing the schematic diagram. An illustration of the circuit board(s) is also included here to identify the physical location of components and waveform test points that appear on the respective schematic diagram. Each circuit board illustration and diagram is arranged in a grid locator with an index to facilitate rapid location of components contained in the corresponding schematic diagram.

SIGNATURE ANALYSIS TROUBLESHOOTING

The 7D20 Programmable Digitizer was designed to accommodate signature analysis for troubleshooting the digital circuitry. Signature analysis is a data compression technique that reduces a complex data stream (a sequence of logic levels occurring during a specific time window) to a series of unique four-digit hexadecimal signatures. The test procedure relies on stimulating (using a program stored in ROM) circuit nodes in a repeatable and predictable fashion. For example, a microprocessor system can be easily made to repeatedly increment through its address field, exercising much of the instrument circuitry.

Signature analysis instructions for the 7D20 appear later in this section under "Testing and Diagnostics".

COMPONENT COLOR CODING

This instrument contains composition resistors, metal-film resistors, and wire-wound resistors. The resistance values of wire-wound resistors are usually printed on the component body. The resistance values of composition resistors and metal-film resistors are color coded on the components, using the EIA color code (some metal-film resistors may have the value printed on the body). The color code is read starting with the stripe nearest the end of the resistor. Composition resistors have four stripes, which consist of two significant figures, a multiplier, and a tolerance value (see Fig. 3-1).

Metal-film resistors have five stripes consisting of three significant figures, a multiplier, and a tolerance value.

The values of common disc capacitors and small electrolytics are marked on the side of the component body. The white ceramic and eoxy-coated tantalum capacitors used in the instrument are color coded using a modified EIA code (see Fig. 3-1).

The cathode end of glass-encased diodes is indicated by a stripe, a series of stripes, or a dot. The cathode and anode ends of metal-encased diodes can be identified by the diode symbol marked on the body.

SEMICONDUCTOR LEAD CONFIGURATIONS

Lead configurations and index locators for semiconductor devices used in the 7D20 Programmable Digitizer are shown in Figure 3-2.

STATIC-SENSITIVE DEVICE CLASSIFICATION

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. See Table 3-2 for relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

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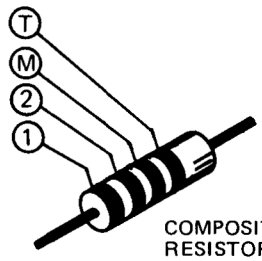
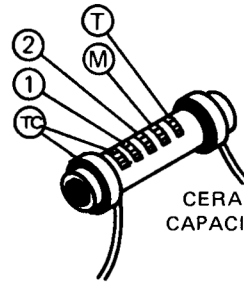
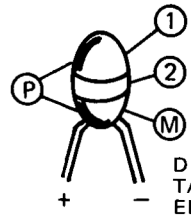
COLOR CODE



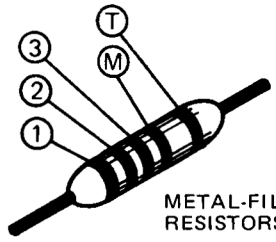
COMPOSITION RESISTORS



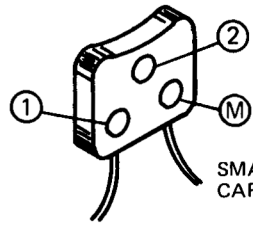
CERAMIC CAPACITORS



DIPPED TANTALUM ELECTROLYTICS



METAL-FILM RESISTORS



SMALL DISC CAPACITORS

(1) (2) and (3) - 1ST, 2ND, AND 3RD SIGNIFICANT FIGS. (T) AND/OR (TC) COLOR CODE MAY NOT BE PRESENT ON SOME CAPACITORS;

(M) - MULTIPLIER (T) - TOLERANCE; (P) - POLARITY AND VOLTAGE RATING

(TC) - TEMPERATURE COEFFICIENT.

COLOR	SIGNIFICANT FIGURES	RESISTORS		CAPACITORS			DIPPED TANTALUM VOLTAGE RATING
		MULTIPLIER (OHMS)	TOLERANCE	MULTIPLIER (pF)	TOLERANCE		
					OVER 10pF	UNDER 10pF	
BLACK	0	1	---	1	±20%	± 2pF	4VDC
BROWN	1	10	±1%	10	±1%	±0.1pF	6VDC
RED	2	10^2 or 100	±2%	10^2or 100	±2%	---	10VDC
ORANGE	3	10^3or 1 K	±3%	10^3 or 1000	±3%	---	15VDC
YELLOW	4	10^4 or 10K	±4%	10^4 or 10,000	+100% −0%	---	20VDC
GREEN	5	10^5 or 100 K	±1/2%	10^5or 100,000	±5%	±0.5pF	25VDC
BLUE	6	10^6 or 1 M	±1/4%	10^6 or 1,000,000	---	---	35VDC
VIOLET	7	---	±1/10%	10^7 or 10,000,000	---	---	50VDC
GRAY	8	---	---	10^{-2} or 0.01	+80% −20%	±0.25pF	---
WHITE	9	---	---	10^{-1} or 0.1	±10%	±1pF	3VDC
GOLD	---	10^{-1} or 0.1	±5%	---	---	---	---
SILVER	---	10^{-2} or 0.01	±10%	---	---	---	---
NONE	---	---	±20%	---	±10%	±1pF	---

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Figure 3-1. Color code for resistors and capacitors.

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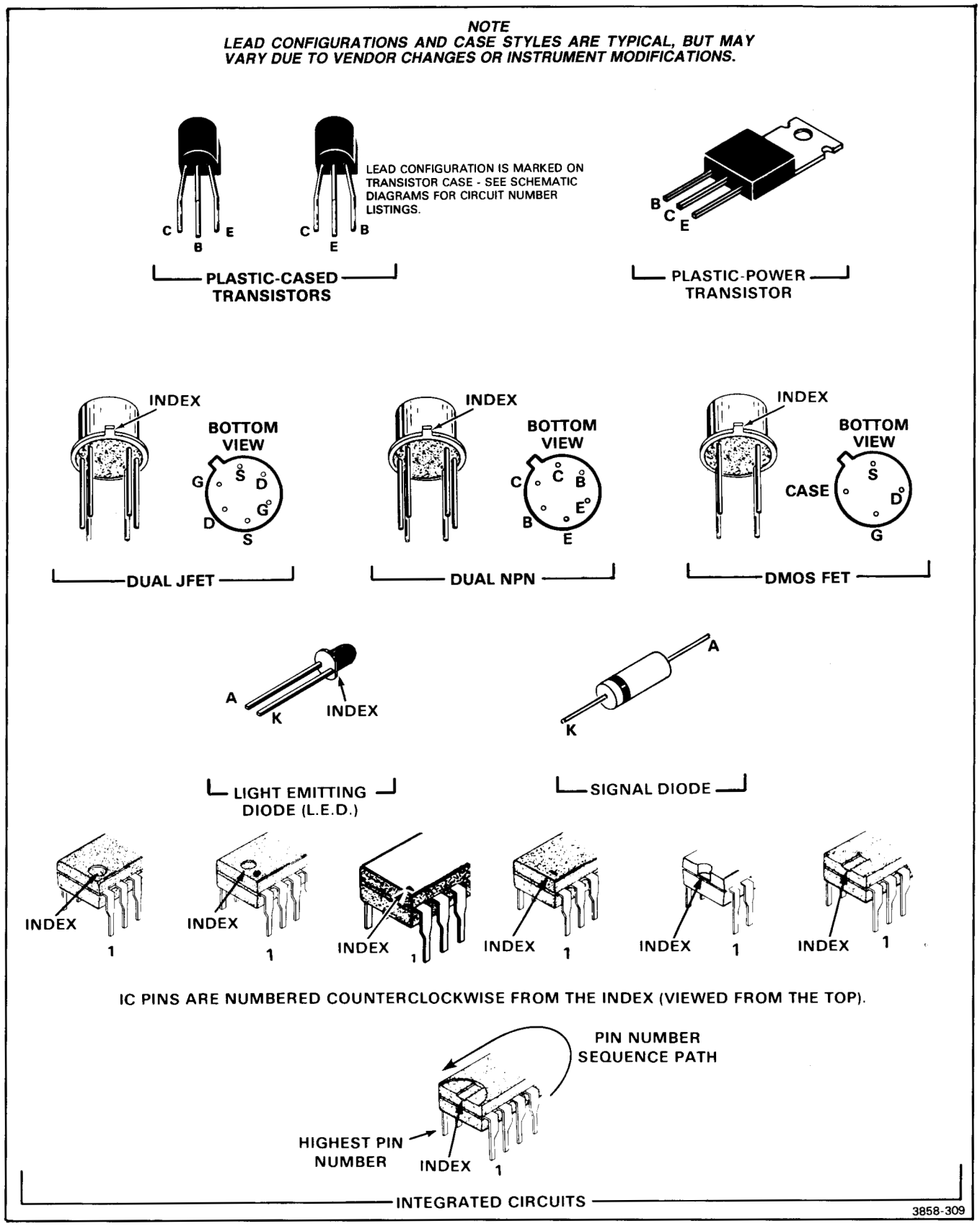

Figure 3-2. Semiconductor lead configuration.

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TABLE 3-2
Relative Susceptibility to Damage from Static Discharge

Semiconductor Classes	Relative Susceptibility Levels[1]
MOS or CMOS microcircuits, and discrete or linear microcircuits with MOS inputs (most sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear Microcircuits	7
Low-power Schottky TTL	8
TTL (least sensitive)	9

[1] **Voltage equivalent for levels.**

1 = 100 to 500 V
2 = 200 to 500 V
3 = 250 V
4 = 500 V
5 = 400 to 600 V
6 = 600 to 800 V
7 = 400 to 1000 V (est.)
8 = 900 V
9 = 1200 V

(Voltage discharged from a 100 pF capacitor through a resistance of 100 ohms).

Observe the following precautions to avoid damage:

1. Minimize handling of static-sensitive components.
2. Transport and store static-sensitive components or assemblies in their original containers on a metal rail, or conductive foam. Label any package that contains static-sensitive assemblies or components.
3. Discharge the static voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies or components should be performed only at a static free work station by qualified service personnel. We recommend use of the Static Control Mat, Tektronix Part 006-3414-00, and Wrist Strap, Tektronix Part 006-3415-00.
4. Allow nothing capable of generating or holding a static charge on the work station surface.
5. Keep the component leads shorted together whenever possible.
6. Pick up components by the body, never by the leads.
7. Do not slide the components over any surface.
8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.

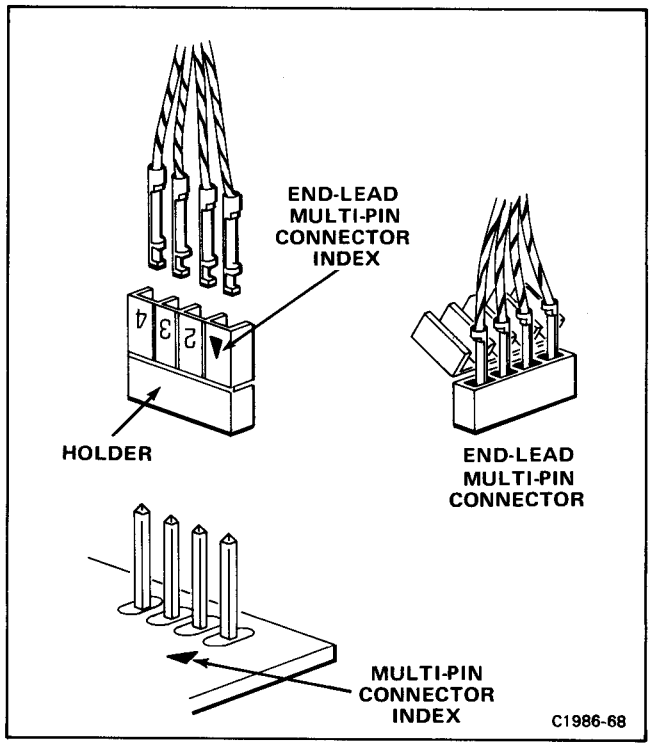

Figure 3-3. Orientation of multi-pin connectors.

9. Use a soldering iron that is connected to earth ground.
10. Use only special antistatic suction type desoldering tools.

MULTI-PIN CONNECTOR IDENTIFICATION

Pin 1 on multi-pin (harmonica, ribbon cable) connectors is designated with a triangle. A triangle, dot or square printed on circuit boards denotes pin 1. When a connection is made to a circuit board, the orientation of the triangle on the multi-pin holder is determined by the index (triangle, dot or square) printed on the circuit board (see Fig. 3-3).

TROUBLESHOOTING EQUIPMENT

The following equipment is useful for troubleshooting the 7D20 Programmable Digitizer:

1. Transistor Tester

   Description: Dynamic-type tester.

   Purpose: Test semiconductors.

   Recommended type: TEKTRONIX 577/177 Curve Tracer, TEKTRONIX 576 Curve Tracer, 7CT1N Curve Tracer plug-in unit and a 7000-series oscilloscope system, or a 5CT1N Curve Tracer plug-in unit and a 5000-series oscilloscope system.

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2. Digital Multimeter

Description: 10 megohm input impedance and 0 to 1 kilovolt range, ac and dc; ohmmeter, accuracy, within 0.1%. Test probes must be insulated to prevent accidental shorting.

Purpose: Check voltages and resistances.

Recommended type: TEKTRONIX DM501A Digital Multimeter.

3. Test Oscilloscope

Description: Frequency response, dc to 50 megahertz minimum; deflection factor, 1 millivolt to 5 volts/division. A 10X, 10-megohm voltage probe should be used to reduce circuit loading for voltage measurements.

Purpose: Check operating waveforms.

4. Calibration Fixtures

(A) Extender Set (board)

Purpose: Troubleshooting the circuit boards.

Recommended type: TEKTRONIX 067-1051-00 Extender.

(B) Extender Set (plug-in)

Purpose: Troubleshooting with 7D20 extended.

Recommended type: TEKTRONIX 067-0616-00 (3 required).

(C) Signature Analyzer

Description: Start/Stop gating inputs, 4 digit hexadecimal readout, Logic level indicator.

Purpose: Digital circuits troubleshooting.

Recommended types:

a. TEKTRONIX 067-1090-00 Signature Analyzer.

b. SONY/TEKTRONIX 308 Data Analyzer.

TROUBLESHOOTING TECHNIQUES

This troubleshooting procedure is arranged to check the simple trouble possibilities before proceeding with extensive troubleshooting. The first few checks ensure proper connection and operation of associated equipment. If the trouble is not located by these checks, the remaining steps aid in locating the defective component. When the defective component is located, replace it using the replacement procedures given under Corrective Maintenance.

1. CHECK CONTROL SETTINGS

Incorrect control settings can indicate a nonexistent trouble. If there is any question about the correct function or operation of any control on the 7D20, refer to the Operators Manual.

2. CHECK ASSOCIATED EQUIPMENT

Before proceeding with troubleshooting, check that the equipment used with this instrument is operating correctly. Also, check that the input signals are properly connected and that the interconnecting cables are not defective. Check the line-voltage source.

3. VISUAL CHECK

Visually check any part of the instrument where the trouble may be located. Many troubles can be found by visible indications such as unsoldered connections, broken wires, damaged circuits, and damaged components. Especially check that all cables are properly installed.

4. ISOLATE TROUBLE TO A CIRCUIT

To isolate the trouble to a circuit, refer to "Testing and Diagnostics," later in this section.

5. CHECK INSTRUMENT ADJUSTMENT

Check the electrical adjustment of this instrument, or of the affected circuit if the trouble appears in one circuit. If the apparent trouble cannot be isolated to a defective component, the trouble may only be a result of maladjustment. Complete adjustment instructions are given in Section 4, Checks and Adjustment.

6. CHECK VOLTAGES

Often the defective component can be located by checking for the correct voltages in the circuit. Typical voltages are given in Section 7, Diagrams and Circuit Board Illustrations.

NOTE

Voltages given in Section 7, Diagrams and Circuit Board Illustrations, are not absolute and may vary slightly between 7D20 Programmable Digitizers. To obtain operating conditions used to take these readings, see the Voltage Conditions adjacent to the schematic diagram.

7. CHECK INDIVIDUAL COMPONENTS

The following procedures describe methods of checking individual components in the 7D20. Components that are soldered in place (excluding integrated circuits) are best checked by first disconnecting one end. This isolates the measurement from the effects of surrounding circuitry.

CAUTION

To avoid electric-shock hazard, always turn off the mainframe power switch before removing or replacing components.

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Fuses

Check for open fuses by checking continuity with an ohmmeter.

WARNING

Before replacing an open fuse, determine the cause of the failure. Refer to the Power Supply Board and Interconnect diagrams and the adjacent board illustrations in the foldout section at the rear of this manual for component locations.

Transistors

A good check of transistor operation is actual performance under operating conditions. A transistor can most effectively be checked by substituting a new component for it (or one which has been previously checked). However, be sure that circuit conditions are not such that a replacement transistor might also be damaged. If substitute transistors are not available, use a dynamic tester. Static type testers are not recommended, because they do not check operation under simulated operating conditions.

Integrated Circuits

Integrated circuits can be checked with a test oscilloscope, signature analyzer, digital tester or by direct substitution.

CAUTION

Direct substitution must not be attempted with soldered in integrated circuits. The I.C., circuit board, or both, could be damaged due to the heat required to melt the solder from the connections. Refer to Soldering Techniques later in this section. Use care when checking voltages and waveforms around the integrated circuits so that adjacent leads are not shorted together. The integrated circuit test clip provides a convenient means of clipping a test probe to the in-line, multi-pin integrated circuits.

A good understanding of the circuit operation is essential to troubleshooting circuits using integrated circuits if a signature analyzer is not available. Operating conditions and other information for the integrated circuits are given in Section 2, Theory of Operation and Section 7, Diagrams and Circuit Board Illustrations.

Diodes

A diode can be checked for an open or shorted condition by measuring the resistance between terminals with an ohmmeter on a scale having a low internal source current, such as the R× 1k scale. The resistance should be very high in one direction and very low when the meter leads are reversed.

CAUTION

When checking diodes, do not use an ohmmeter scale setting that has a high internal current, because high currents may damage the diodes under test.

Resistors

Check the resistors with an ohmmeter. Resistor tolerances are given in Section 6, Replaceable Electrical Parts. Normally, resistors need not be replaced unless the measured value varies widely from the specified value.

Capacitors

A leaky or shorted capacitor can best be detected by checking resistance with an ohmmeter on the highest scale. Do not exceed the voltage rating of the capacitor. The resistance reading should be high after initial charge of the capacitor. An open capacitor can best be detected with a capacitance meter or by checking if the capacitor passes ac signals.

8. REPAIR AND ADJUST THE CIRCUIT

If any defective parts are located, follow the replacement procedures given under Component Replacement in this section. Check the performance of any circuit that has been repaired or that has had any electrical components replaced. Adjustment of the circuit may be necessary.

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CORRECTIVE MAINTENANCE

Corrective maintenance consists of component replacement and assembly repair. Special techniques required to replace components in the 7D20 Programmable Digitizer are given here.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, you should be able to obtain many of the standard electronic components from a local commercial source in your area. Before you purchase or order a part from any source other than Tektronix, Inc., please check the electrical parts list for the proper value, rating, tolerance and description.

SPECIAL PARTS

Some parts are manufactured or selected by Tektronix, Inc. to satisfy particular requirements, or are manufactured for Tektronix, Inc. to our specifications. Most of the mechanical parts used in this instrument were manufactured by Tektronix, Inc. To determine manufacturer of parts, refer to Parts List, Cross Index Mfr. Code Number to Manufacturer.

Also, some electrical parts are selected for a value that provides optimum circuit operation. These parts are identified by "SEL" next to the value on the schematic diagram. Criteria for these SELectable parts are provided in tables adjacent to the schematic diagram on which the part is located.

ORDERING PARTS

When ordering replacement parts from Tektronix, Inc., include the following information:

Instrument type.
Instrument serial number.
A description of the part; if electrical, include circuit number.
Tektronix part number.

SOLDERING TECHNIQUES

WARNING

To avoid electric-shock hazard and instrument damage, disconnect the 7D20 from the power source before soldering.

The reliability and accuracy of this assembly can be maintained only if proper soldering techniques are used when repairing or replacing parts.

The desoldering and removal of parts is especially critical and should be done only with a vacuum solder extractor; further, one approved by a Tektronix Inc., Service Center.

Use wire solder with rosin core, 63% tin, 37% lead. Contact your local Tektronix Inc. representative of field office for approved solders.

All circuit boards used in this instrument are multilayer. Conductive paths between the top and bottom board layers may connecct with one or any number of inner layers. Once this inner conductive path is broken (due mainly to poor soldering practices) between the layers, the board is unusable and must be replaced. Damage can void warranty.

CAUTION

Only an experienced maintenance person, proficient in the use of vacuum type desoldering equipment, should attempt repair of any board in this instrument.

When soldering on circuit boards or small wiring, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron can cause the etched circuit wiring to separate from the board base material, and melt the insulation from small wiring. Always keep the soldering-iron tip properly tinned to ensure the best heat transfer to the solder joint. Apply only enough heat to make a good solder joint. To protect heat-sensitive components, hold the component lead with a pair of long-nose pliers between the component body and the solder joint.

The following technique should be used to replace a component on any of the circuit boards.

Touch the tip of the vacuum desoldering tool directly to the solder to be removed.

CAUTION

Excessive heat can cause the etched circuit wiring to separate from the board base material.

Never allow the solder extractor to remain on the board for more than three seconds. Solder wick, spring-actuated or squeeze-bulb solder suckers, and heat blocks (for multi-pin components) must not be used. Damage can void warranty.

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NOTE

Some components are difficult to remove from the circuit boards due to a bend placed in each lead during machine insertion of the component. The bent leads held the component in position during a flow-solder manufacturing process which soldered all components at once. To make removal of machine inserted components easier, first remove the solder from the joint, then straighten the leads of the component on the back of the circuit board, using a small screwdriver or pliers.

When removing multi-pin components, do not heat adjacent conductors consecutively (see Fig. 3-4). Allow a moment for the circuit board to cool before proceeding to the next pin.

Bend the leads of the replacement components to fit the holes in the circuit board. Insert the leads into the holes in the board, or as originally positioned.

Touch the iron to the connection and apply enough solder to make a firm solder joint.

Cut off any excess lead protruding through the board.

Clean the areas around the solder connection with a flux removing solvent. Be careful not to remove the information printed on the circuit board.

COMPONENT REMOVAL AND REPLACEMENT

CAUTION

To avoid component damage, always disconnect the assembly from the power source before removing or replacing components.

The exploded-view drawing associated with the Replaceable Mechanical Parts list (located at the rear of this manual) may be helpful in the disassembly procedures that follow.

SEMICONDUCTORS

Semiconductors should not be replaced unless actually defective. If removed from their sockets during routine maintenance, return them to their original sockets. Unnecessary replacement of semiconductors may affect the adjustment of the instrument. When semiconductors are replaced, check the operation of circuits which may be affected.

Replacement semiconductors should be of the original type or a direct replacement. Lead configurations of the semiconductors used in this instrument are shown in Figure 3-2.

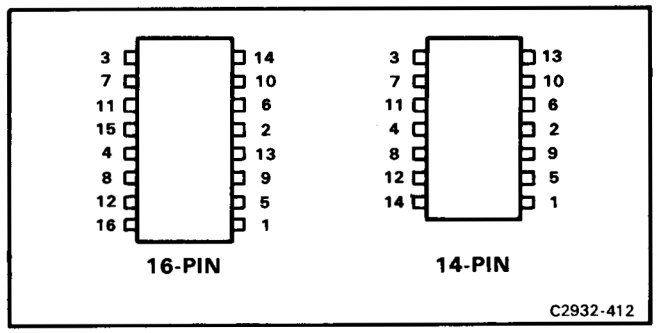

Figure 3-4. Recommended desoldering sequence.

CAUTION

Do not remove stickers affixed to the top of EPROMs. Removal of this sticker will allow light into the chip, and may cause partial erasure of its data.

An extracting tool should be used to remove the in-line integrated circuits to prevent damaging the pins. This tool is available from Tektronix, Inc.; order Tektronix Part 003-0619-00. If an extracting tool is not available, use care to avoid damaging the pins. Pull slowly and evenly on both ends of the integrated circuit. Try to avoid one end disengaging from the socket before the other end.

CIRCUIT BOARDS

If a circuit board is damaged beyond repair, replace the entire board assembly. Part numbers are listed in Section 6, Replaceable Electrical Parts, for completely wired boards.

Refer to the "Diagrams and Circuit Board Illustrations" section for the location of each circuit board.

Some parts mounted on the board must be retained for use with the new assembly, such as extension shafts, support posts, switch pushbutton knobs, lamps and board to front-panel wiring.

NOTE

Refer to Adjustment After Repair earlier in this section.

Tools Required

1. #1 Phillips screwdriver.
2. #2 Phillips screwdriver.
3. 1/4-inch nutdriver.
4. 1/4-inch open-end or box-end wrench.
5. 5/16-inch nutdriver.
6. 1/16-inch Allen wrench.
7. Needle-nose pliers.
8. 3/16-inch nutdriver.
9. Small straight-slot screwdriver.

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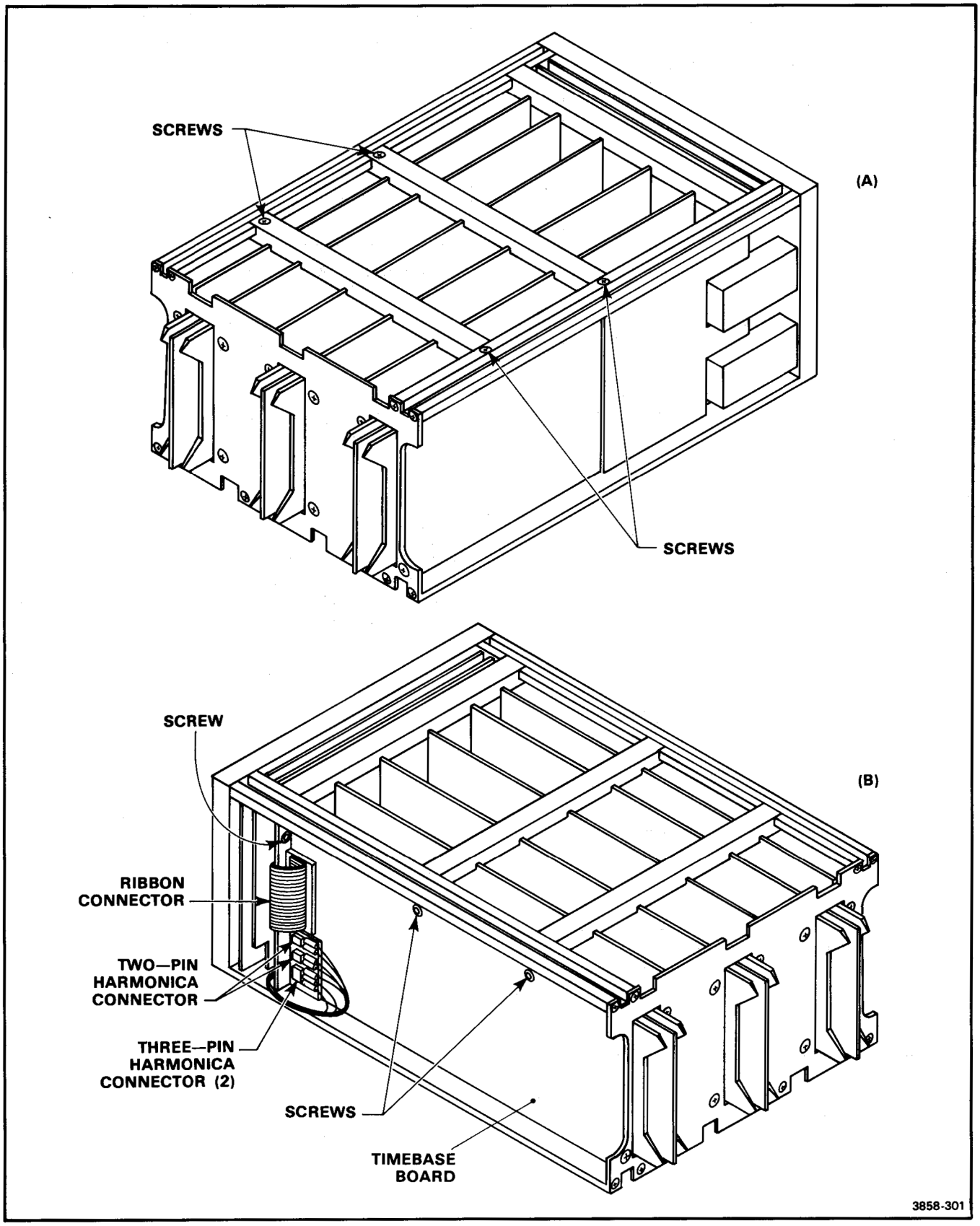

Figure 3-5. Board guide and Interconnect Board Removal.

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Board Guides

1. Place the 7D20 in its normal, upright position (A), with the front panel facing you.

2. Using a #2 Phillips screwdriver, remove the four flathead screws that fasten the upper board guides in place. See Figure 3-5.

3. Turn the 7D20 counterclockwise (B) to expose the Time-base board. Remove the two screws that secure the board to the upper board guides. See Figure 3-5.

4. Place the 7D20 in the upright position.

5. Remove the two upper board guides by lifting up on the right-hand end, then sliding the support to the right from under the left frame rail.

6. To replace the board guides, slide each into position, then press the guides down gently while positioning the boards into the guide slots. Fasten the two guides in place with the six screws.

Back Panel

1. Place the 7D20 on a workbench with the back panel facing you.

2. Using a #2 Phillips screwdriver, remove the eight fillister-head screws that secure the back panel to the four frame rails. See Figure 3-6.

3. Disconnect all coaxial cables that are clamped to the rear panel from their respective boards. (If only the rear panel is to be removed, the cables need not be disconnected; just remove the plastic cable clamp to the top of the rear panel.) These are:

   a. A1 CCD Board:
      J1 (brown on white)
      J2 (red on white)
      J3 (orange on white)
      J4 (yellow on white)

   b. A10 Trigger Board:
      J5 (green on white)
      J6 (blue on white)

NOTE

To prevent the side rails from springing apart when the front or rear panel is removed, replace the side covers before removing the front or rear panel.

4. Lift the back panel away from the frame rails, taking care not to snag the cables during removal.

5. To replace the back panel, reverse the previous steps. Be sure to connect each cable to the correct connector, and avoid pinching the cables when fastening the back panel to the frame rails.

Front Panel

1. Invert the 7D20 for access to the bottom of the instrument.

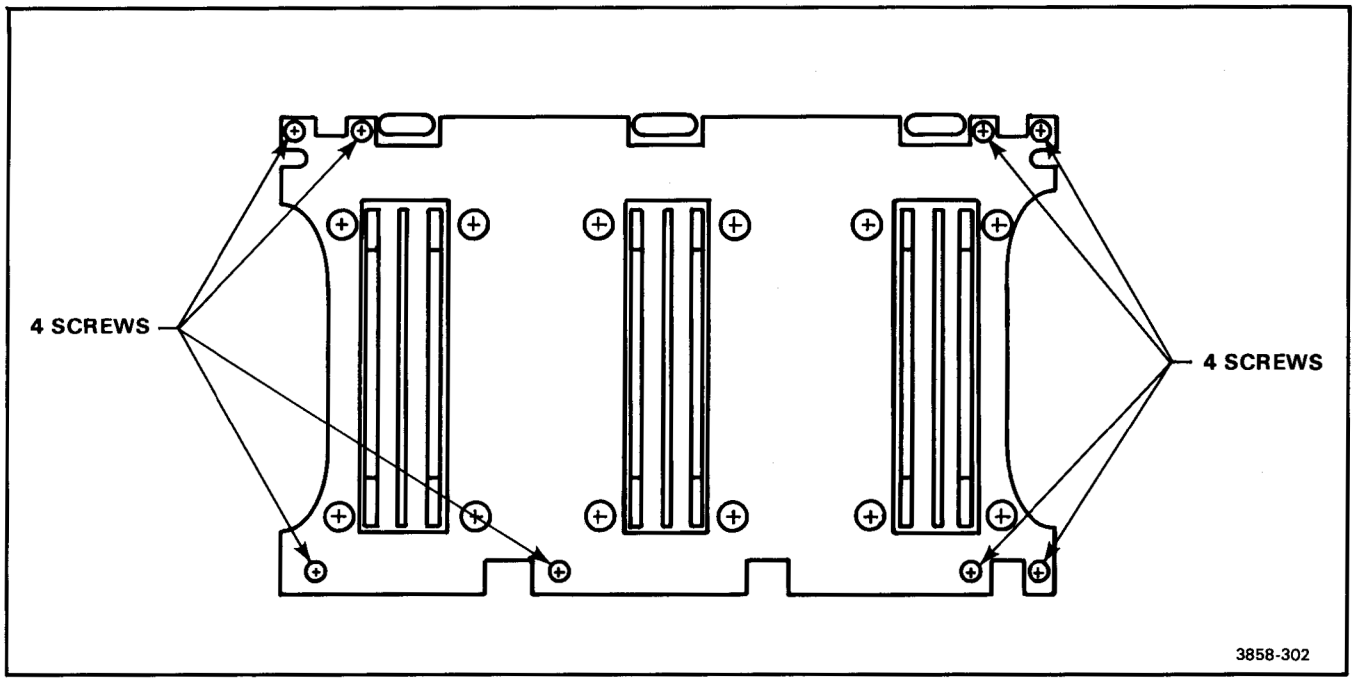

Figure 3-6. Back-panel removal.

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2. Using needle-nose pliers, squeeze the latch fingers to release the latch knob. Lift the latch knob from the 7D20. See Figure 3-7.

3. Position the 7D20 to permit access to the Preamp board. Remove the 6-32 nut that fastens the Attenuator frame to the front casting (see Fig. 3-8).

4. Using a #2 Phillips screwdriver, remove the eight flat-head screws that fasten the front casting to the front rails.

5. Disconnect the violet-on-white cable that attaches to the rear of the EXT TRIG jack on the front panel.

6. Disconnect the ribbon cable and the three harmonica connectors from the Interconnector board. Be sure to note where each cable is connected.

7. Lift the front-panel assembly away from the 7D20, taking care not to snag any cables.

Front-Panel Disassembly

The front-panel unit consists of two boards, the subpanel casting, and the front panel. To remove the front panel from the casting, remove all knobs and the GPIB cover, then proceed as follows:

1. Remove five screws from the circuit boards and two screws from the GPIB bracket.

2. Remove the two boards as an assembly.

3. Remove seven nuts, that fasten the front panel to the front subpanel.

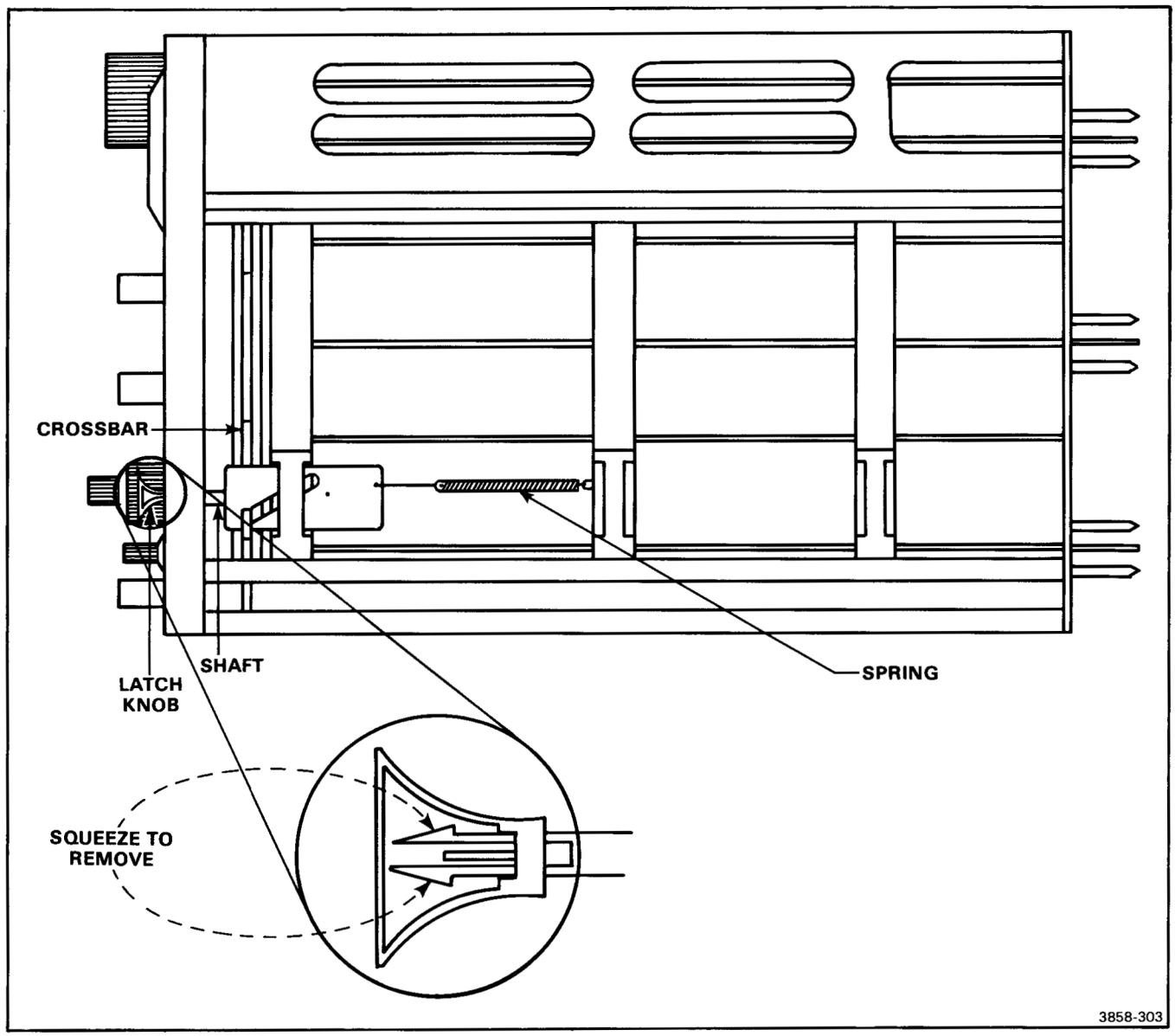

Figure 3-7. Latch assembly.

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4. Remove the front panel from the subpanel.

To remove only the circuit boards from the front casting, perform the following:

1. Remove the six fillister-head screws that secure the two boards to the front casting.
2. Remove the GPIB cover from the connector.
3. Remove the two fillister-head screws that fasten the GPIB connector to the front casting.
4. Remove all knobs except the position knobs. Be sure to note the indexing of the LEVEL and VARIABLE knobs to ensure proper positioning of each during re-assembly.
5. Separate the two boards from the front casting.
6. To re-assemble, reverse the procedure.

Separating The Front-Panel Boards

1. Remove the front-panel boards from the front casting.
2. Using a scriber or small screwdriver, pry the fingers that secure the ground contact to each potentiometer body, and lift the ground washer off each potentiometer.
3. Remove the nylon washer from each potentiometer.
4. Pull the boards apart, keeping them parallel until the interboard connector pins are free. If there is a burr on the potentiometer shaft, it may require smoothing before the boards can be separated.
5. To reconnect the two boards, align them, checking to see that no components or connector pins are misaligned or out of place.

NOTE

When the two boards are separated, the LEDs are supported only by their leads. Be careful not to bend any of them because it will make reassembly difficult.

6. Slide the boards together until the spacers contact the board. Make sure that each lamp is positioned to enter the hole provided for it.
7. Replace the nylon washers and grounding washers on the two potentiometers.

Switch Replacement

The front-panel assembly has a number of switches that light when pressed. To replace one, perform the following:

1. Remove the front-panel assembly and separate the boards.
2. Locate the mounting posts of the switch to be replaced.
3. Working from the back of the circuit board, use a flat object to press the two mounting posts in until they are flush with the back of the board.

CAUTION

Do not pry the switch from the front of the board. Doing so could damage the circuit board pads and runs.

4. Grip the switch firmly and pull it out of the board.
5. Align the new switch properly, then press it into place.
6. Re-assemble and install the front-panel assembly.

A11 Timebase Board

1. Remove the side panels.
2. Remove the two Phillips-head screws that secure the Timebase Board to the board guides. See Figure 3-5.
3. Rock the rear end of the Timebase Board up and down while pulling it to the rear of the 7D20, until it is free of its receptacle. Then tip the top edge of the board outward and lift the board up and out of the lower guide.
4. Lift the board out of the 7D20, using care not to damage any components.
5. To replace, set the board in the lower guide, swing it inward until it aligns with the connector, then insert it firmly into the end connector.
6. Fasten the board into place with the two screws.

A9 MPU Board

1. Remove the fillister-head screw that secures the MPU Board ground lead to the 7D20 frame.
2. Remove the board guides.
3. Rock the rear end of the MPU Board up and down while pulling the board to the rear of the 7D20.
4. When the board is free of the receptacle, lift it out of the 7D20. Use caution not to bend or damage components while removing the board.

CAUTION

The 7D20 has static-sensitive components. Be sure to observe all special precautions mentioned under the heading "Static-Sensitive Device Classification" in this section.

A8 Memory Board

1. Remove the board guides.
2. Rock the board up and down while pulling it to the rear of the 7D20.
3. When the board is free of the receptacle, lift it out of the 7D20. Use care not to bend or damage any components.

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4. To replace, put the board in the slots in the lower guide, then insert the board into its socket. Finally replace the upper guide.

A6 Display Board

1. Remove the board guides.
2. Rock the rear end of the Display Board up and down while pulling it to the rear of the 7D20.
3. When the board is free of the receptacle, lift it out of the 7D20. Use care not to bend or damage any components.
4. To replace, put the board in the slots in the lower guide, then insert the board into its socket. Finally replace the upper guide.

A5 CCD Board

1. Remove the board guides.

CAUTION

Charge-coupled devices tolerate no static discharge whatsoever; the slightest potential can destroy a charge-coupled device. See the instructions in this section for the proper precautions to take when working with such devices.

2. Using long-nosed pliers, disconnect the two coaxial cables. Note the color code on each cable for use when re-connecting the cables: The front-most cable is red on white, connecting to J2; the rear-most cable is brown on white, connecting to J1.
3. Invert the 7D20.
4. Remove the two remaining coaxial cables from the CCD Board. These are orange on white, connecting to J3; and yellow on white (rearmost), connecting to J4. Return the 7D20 to its upright position.
5. Rock the CCD Board up and down while pulling it toward the rear of the 7D20, being careful not to contact any of the charge-coupled devices or damage the board.
6. When the board is free, lift it out of the 7D20.
7. To replace, insert the board into its receptacle. Connect the four coaxial cables to the board, as mentioned in steps 2 and 4.

A10 Trigger Board

1. Remove the back panel.
2. Remove the board guides.
3. Disconnect the violet-on-white coaxial cable from the board.
4. Rock the Trigger Board up and down while pulling it to the rear of the 7D20.
5. When the board is free of its receptacle, pull it out the rear of the 7D20.
6. To replace the board, insert the board into its receptacle, reconnect the trigger cable, replace the back panel, and replace the board guides.

A7 Power Supply Board

1. Remove the board guides.
2. Remove the back panel.
3. Rock the Power Supply Board up and down while pulling it to the rear of the 7D20.
4. When the board is free of its receptacle, pull it out of the 7D20.
5. To replace the board, insert the board into its receptacle, re-install the back panel, and re-install the board guides.

A3 Interconnect Board Removal

1. Remove the board guides.
2. Remove the back panel.
3. Remove the Timebase, MPU, Memory, Power Supply, Display, and CCD boards from the 7D20.
4. Remove the fillister-head screw that secures the Interconnect board to the side rail. See Figure 3-5.
5. Disconnect the violet-on-white coaxial cable from the Trigger Board and the front-panel assembly and remove it from the 7D20.
6. Disconnect the two three-pin and one two-pin harmonica connectors, and the ribbon cable from the Interconnect Board. Note the color code and position of each cable.
7. Pull the Interconnect Board out the side of the 7D20, disconnecting it from the Preamp Board. Use care to avoid damaging any components while removing the board.

A4 Preamp Board

NOTE

To remove the Preamp Board, it is necessary to remove all other boards in the 7D20 except the front-panel assembly. The Preamp Board is designed to permit easy access for troubleshooting, so it should not be necessary to remove it unless replacement is required.

1. Remove the back panel.
2. Remove the board guides.
3. Remove the Interconnect Board.

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4. Disconnect the six coaxial cables from the Preamp Board. Note the position of each of the cables for reconnection.

5. Using a 5/16-inch nutdriver, remove the nut that secures the attenuators to the front casting. See Figure 3-8.

6. Remove the four nuts and screws that secure the ground straps (three on the top rail, one on the bottom rail) to the frame rails.

7. Remove the two screws that fasten the preamp adjustment shield to the Preamp Board. Unsnap the shield and lift it from the board.

8. Slide the Preamp Board out of the 7D20.

Attenuator Covers and Relays

1. Remove the two Phillips-head screws that secure the adjustment shields in place.

2. Using a 3/16-inch nutdriver, remove the standoffs and washers that secure the rear of each attenuator cover to the Preamp Board.

3. Lift each cover away from the board, rear-end first, sliding the cover backwards to clear the attenuator body.

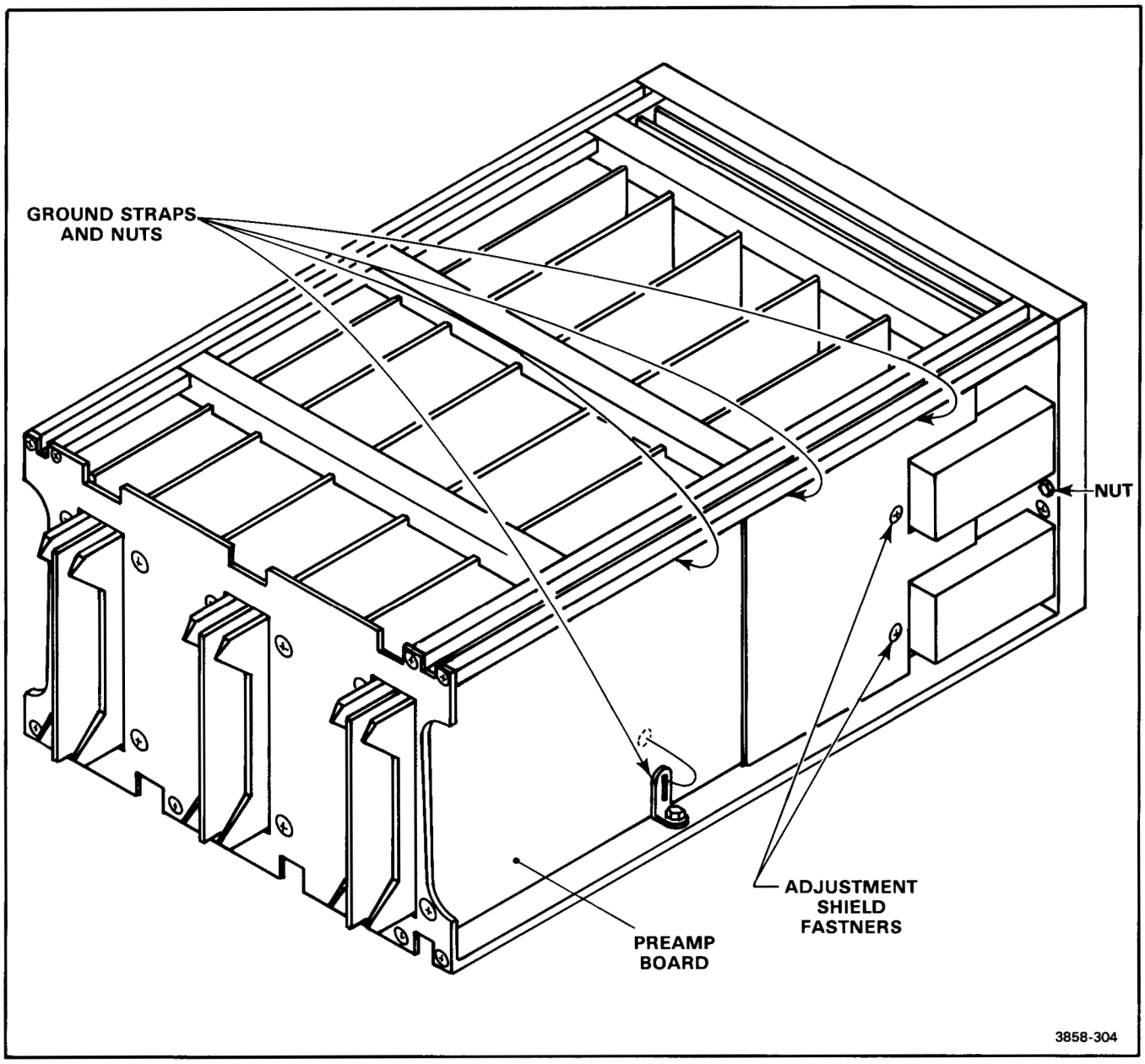

Figure 3-8. Preamp Board removal.

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4. Remove the four screws that fasten the relay holder in place, and lift it off.
5. Remove relays, as required, by lifting the relay up from the board.
6. To re-install, plug the relay into the hybrid assembly, secure it with the holder, then reverse the remaining steps.

Attenuator

1. Perform steps 1 through 3 of Attenuator Covers and Relays removal procedure.
2. Perform steps 1 through 7 of Front Panel removal procedure.
3. Remove the four nuts that fasten the attenuator frame to the attenuator bracket.
4. Unsolder the rear connections to the attenuator.
5. Lift the attenuator away from the Preamp Board.
6. To replace, reverse the previous steps.

Plug-in Latch

1. Using needle-nose pliers, squeeze the lock mechanism and pull the knob of the latch shaft. See Figure 3-7.
2. Remove the latch shaft return spring.
3. Remove the front-panel assembly.
4. Remove the clips that hold the latch crossbar in place.
5. Lift the crossbar out of its groove, then out of the 7D20.
6. To replace, insert the crossbar and shaft into the grooves, re-install the clips, and press the latch knob on to the shaft until it snaps into place.
7. Attach the spring to the shaft.
8. Re-install the front-panel assembly on the 7D20.

INTERCONNECTING PINS

Two methods of interconnection are used in this instrument to electrically connect the circuit boards with other boards and components. When the interconnection is made with a coaxial cable, a special end-lead connector plugs into a socket on the board. Other interconnections are made with a pin soldered into the board. Two types of mating connectors are used for these interconnecting pins. If the mating connector is mounted on a plug-on circuit board, a special socket is soldered into the board. If the mating connector is on the end of a lead, an end-lead pin connector is used that mates with the interconnecting pin. The following information provides the removal and replacement procedure for the various types of interconnecting methods.

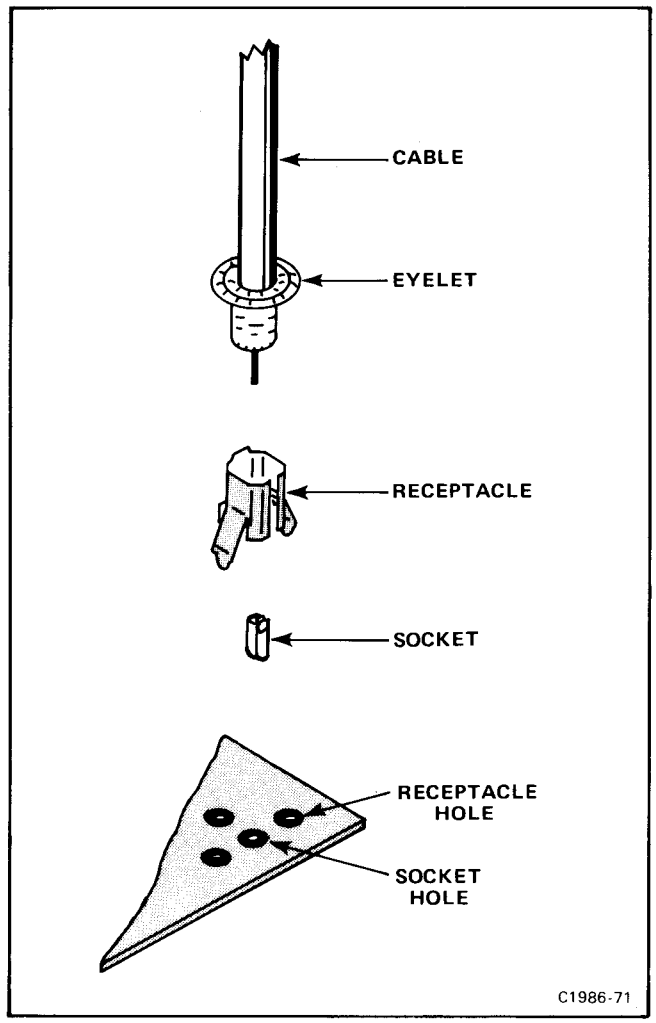

Figure 3-9. Coaxial-end lead connector assembly.

Coaxial-Type End-Lead Connectors

Replacement of the coaxial-type end-lead connectors requires special tools and techniques; only experienced maintenance personnel should attempt to remove or replace these connectors. We recommend that the damaged cable or wiring harness be replaced as a unit. For cable or wiring harness part numbers, see Section 8, Replaceable Mechanical Parts. An alternative solution is to refer the replacement of the defective connector to your local Tektronix Field Office or representative. Figure 3-9 gives an exploded view of a coaxial end-lead connector assembly.

Circuit-Board Pins

A circuit-board pin replacement kit (including necessary tools, instructions, and replacement pins with attached ferrules) is available from Tektronix, Inc. Order Tektronix Part. 040-0542-01. Replacing circuit-board pins on multi-layer boards is not recommended. (The multi-layer boards in this instrument are listed under Soldering Techniques in this section.)

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To replace a damaged pin, first disconnect any pin connectors. Then remove the solder from the connection using a vacuum desoldering tool. (See Soldering Techniques.) Remove the damaged pin from the board with a pair of pliers, leaving the ferrule (see Fig. 3-10) in the circuit board if possible. If the ferrule remains in the circuit board, remove the spare ferrule from the replacement pin and press the new pin into the hole in the circuit board. If the ferrule is removed with the damaged pin, then press the replacement pin, with attached spare ferrule, into the circuit board. Position the replacement pin in the same manner as the original. Solder the pin to the circuit board on each side of the board. If the original pin was bent at an angle to mate with a connector, carefully bend the new pin to the same angle. Replace the pin connector.

Circuit-Board Pin Sockets

The pin sockets on the circuit boards are soldered to the back of the board. To remove or replace one of these sockets, first unsolder the pin (see Soldering Techniques). Then straighten the tabs on the socket and remove the socket from the board. Place the new socket in the circuit board hole and press the tabs down against the board. Solder the tabs of the socket to the circuit board; be careful not to get solder inside the socket.

NOTE

The spring tension of the pin sockets ensures a good connection between the circuit board and the pin. This spring tension can be destroyed by using the pin sockets as a connecting point for spring-loaded probe tips, alligator clips, etc.

Multi-Pin Connectors

The pin connectors used to connect the wires to the interconnecting pins are clamped to the ends of the associated leads. To remove or replace damaged multi-pin connectors, remove the old pin connectors from the end of the lead and clamp the replacement connector to the lead.

NOTE

Some multi-pin connectors are equipped with a special locking mechanism. These connectors cannot be removed by pulling the wire(s). To remove the connectors from the pin(s) grasp the plastic holder and pull.

To remove an individual wire from the holder insert a scribe in the hole on the side of the holder and slide the extended portion under the holder. This will allow the wire to be removed from the holder.

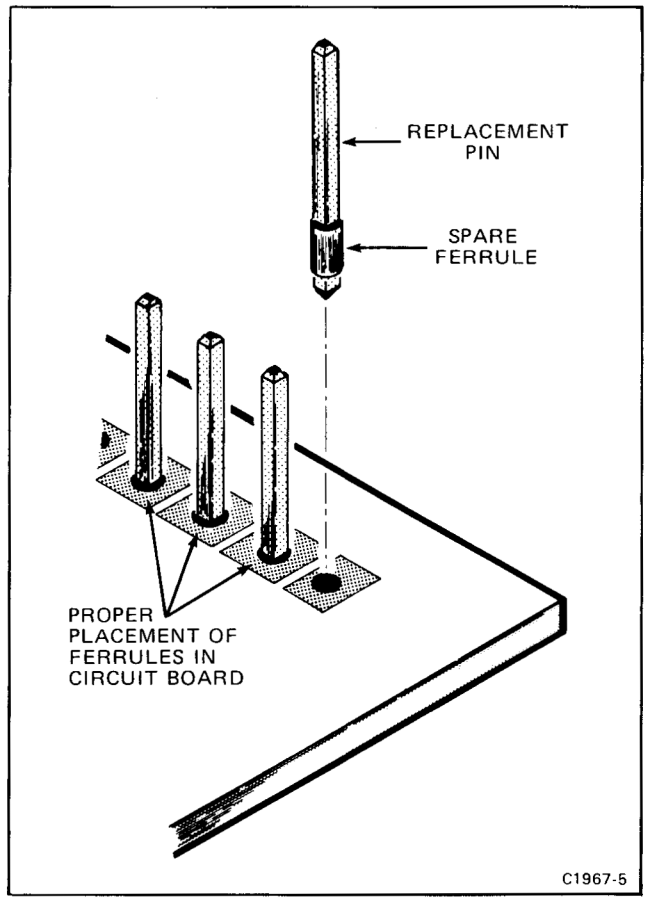

Figure 3-10. Exploded view of circuit-board pin and ferrule.

Some of the pin connectors are grouped together and mounted in a plastic holder; the overall result is that these connectors are removed and installed as a multi-pin connector (see Troubleshooting Aids). If the individual end-lead pin connectors are removed from the plastic holder, note the order of the individual wires for correct replacement in the holder.

ADJUSTMENT AFTER REPAIR

After any electrical component has been replaced, the adjustment of that particular circuit should be checked, as well as the adjustment of any closely related circuits. See section 4 for a complete adjustment procedure.

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TESTING AND DIAGNOSTICS

This part of the Maintenance Section describes the self-contained system with which the 7D20 can diagnose internal electrical trouble. Signature tables, for use with signature analysis, are located in section 7 behind the diagrams.

INTRODUCTION

The 7D20 Programmable Digitizer is designed so that if a trouble occurs, it can be quickly diagnosed with a minimum of test equipment.

Each time the 7D20 is turned on, it tests itself comprehensively with a series of 63 "Self-Tests." (Self-Tests are described in the Testing Facilities part of this section, which follows.) After the Self-Test sequence has been performed, the result will be displayed on the crt of the host oscilloscope as SELFTEST PASS or FAIL N (where N is the number of the individual Self-Test that failed.)

When the message SELFTEST PASS is displayed, the operator can use the 7D20 with confidence that it is operating correctly.

If a FAIL N message identifies a faulty circuit module, a service technician can command the 7D20, via its front-panel controls, to repetitively stimulate that circuit module with the same stimulus that detected the problem. The technician can then diagnose and correct the difficulty with a signature analyzer or an oscilloscope, as required by the test. (Signature analysis is discussed in Background Information on Signature Analysis, in this section.) This repetitive stimulus method of troubleshooting is called Circuit Exercise. Circuit Exercise is explained in the Troubleshooting Modules part of this section.

If the 7D20 becomes totally unresponsive, refer to What To Do if the 7D20 Does Not Respond to Front-Panel Controls, in this section.

Signature analysis tables, for those modules where signature analysis is suited, are provided in section 7 of this manual.

TESTING FACILITIES

The 7D20 contains extensive built-in testing capabilities designed to verify its operating integrity. In the case of failure this facility may be used to identify a particular subset of circuitry where the failure resides. Due to the nature of isolating particular parts of the circuit, some tests can be run completely without operator intervention and are referred to as Self-Tests. Other tests require minimal operator assistance or special precautions and are therefore subdivided and referred to as Extended Tests.

The Self-Test routine can be used in three situations, as follows:

1. Self-Test is performed automatically at power-up. This may isolate a particular module that should be trouble-shot before the 7D20 is used.

2. Self-Test can be manually initiated by the operator to verify the result of the power-up Self-Test.

3. The operator can start a Self-Test any time he suspects a problem.

Refer to the Self-Test part, which follows, for further details.

The Extended Tests are tests which are performed only when the operator suspects trouble. There are three Extended Tests, as follows:

1. The GPIB Test, which requires that the GPIB cable be disconnected. It is not performed at power-up for that reason.

2. The EAROM Test, which ages the EAROM and should therefore be used sparingly to prolong the life of the EAROM. (The EAROM Extended Test is different than the EAROM Self-Test, which does not age the EAROM.)

3. The Front-Panel Test, which requires user interaction.

Refer to the Extended Test part, which follows, for more details.

SELF-TEST

Self-Test is a means of verifying that the 7D20 is operating correctly. Self-Test consists of a series of 63 tests for various parts of the 7D20 circuitry.

The Self-Test is performed automatically each time the 7D20 is powered-up. The operator can also initiate a Self-Test at any time via the 7D20 front panel or via the GPIB. If necessary, the operator can run a particular self-test repeatedly via the Circuit Exercise menu. (This is useful for troubleshooting.)

The power-up Self-Test treats the first eight tests differently than does a Self-Test initiated via the front panel or via the GPIB. The power-up Self-Test uses as little of the kernel as possible (the MPU, one PROM, the address and data lines) to test the entire kernel. When a problem is located with this test method, the functional

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part of the kernel will probably be able to provide an error display. If any of the first eight tests fails Self-Test, the MEMORY DISPLAY pushbuttons will display the number of that test and the CSW button will blink. To continue the Self-Test, press the CSW button. Self-Test will then resume with test nine.

To initiate a Self-Test via the 7D20 front panel or via the GPIB, the 7D20 must be operational. Therefore it will be able to provide an error display, and the Self-Test will include all 63 tests.

How to Start a Self-Test

To start a Self-Test via the front panel, proceed as follows:

1. Press *f*.
2. Press MENU/TEST.

The crt will then display the Test Menu. Item 1 will be EXECUTE SELFTEST. (If a submenu is displayed instead, press the MEMORY DISPLAY 6 button to display the Test Menu.)

3. Press the MEMORY DISPLAY 1 button.

The Self-Test will then start checking the 7D20's circuitry.

After the Self-Test has been performed, the result will be displayed on the crt of the host mainframe and by the MEMORY DISPLAY pushbuttons.

If all 63 circuits pass their tests, the 7D20 will be reset to the state it was in before Self-Test was initiated, and all waveform memories will be initialized. A "SELFTEST PASS" message will appear in the prompt field of the crt, and the controller will be notified with an Operation Complete service request (SRQ).

If the Self-Test finds a fault, the following indications will be made:

- The 7D20 MEMORY DISPLAY pushbuttons will light. The CSW button will light to indicate that a test failed, and the numbered buttons will light to identify that test. When read in descending order, the numbers will match the code displayed on the the crt. Table 3-3 shows how to interpret the lighted MEMORY DISPLAY numbered pushbuttons and Table 3-4 lists the tests and their display codes.
- The crt display will read FAIL N, where N is the number of the test that failed. N can have up to six digits.
- The crt display will present the SELFTEST FAILURE menu, which is:

SELFTEST FAILURE
1. CONTINUE SELFTEST
2. EXIT SELFTEST.

The operator can then continue the Self-Test by pressing the MEMORY DISPLAY 1 button. The crt will continue to show FAIL whether or not the rest of the Self-Test finds any faults. When the entire Self-Test has been made, the crt display will read SELFTEST FAIL with no display code.

To leave the Self-Test mode, press the MEMORY DISPLAY 2 button. The crt display will then read SELFTEST FAIL, and the 7D20 will return to normal operating mode.

Repetitive Self-Testing

To help locate an intermittent fault, it is helpful to be able to perform Self-Test repetitively. The Self-Test routine will run repetitively when the Cycle jumper (P410) is removed. P410 is located between U410 and U510 on the MPU Board.

When P410 is installed, the Self-Test operates normally.

EXTENDED TESTS

There are three Extended Tests, as follows:

EAROM Test

Because it tests the "store" capability of the EAROM, the EAROM Test routine is a more thorough test of the

TABLE 3-3
Lighted MEMORY DISPLAY Buttons vs Test Indicated

MEMORY DISPLAY Buttons						Test No.	Display Code
$6(2^5)$	$5(2^4)$	$4(2^3)$	$3(2^2)$	$2(2^1)$	$1(2^0)$		
off	off	off	off	off	on	1	1
off	off	off	off	on	off	2	2
off	off	off	off	on	on	3	21
on	on	on	on	off	on	61	65431
on	on	on	on	on	off	62	65432
on	on	on	on	on	on	63	654321

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TABLE 3-4
Self-Tests

Test Number	Display Code*	Name of Circuit Being Tested	Circuit Module
1	1.	PROM U400	MPU
2	2.	PROM U300	MPU
3	21.	PROM U200	MPU
4	3.	PROM U500	MPU
5	31.	PROM U700	MPU
6	32.	PROM U600	MPU
7	321.	RAM U900	MPU
8	4.	RAM U800	MPU
9	41.	EAROM	MPU
10	42.	A/D Converter	MPU
11	421.	CH 1 Position DAC	MPU
12	43.	CH 2 Position DAC	MPU
13	431.	Power Supply	Power Supply
14	432.	Address Bus and RMA Latch	Memory
15	4321.	Display Address Generator	Memory
16	5.	Display Address Generator (normal clocking)	Memory
17	51.	Data Bus and RMD Latch	Memory
18	52.	WMS Generator	Memory
19	521.	Waveform RAM 1 (U910)	Memory
20	53.	Waveform RAM 2 (U810)	Memory
21	531.	Waveform RAM 3 (U710)	Memory
22	532.	Waveform RAM 4 (U610)	Memory
23	5321.	Waveform RAM 5 (U510)	Memory
24	54.	Waveform RAM 6 (U410)	Memory
25	541.	Waveform RAM 7 (U310)	Memory
26	542.	Waveform RAM 8 (U210)	Memory
27	5421.	Block Select	Memory
28	543.	Display Interrupt Generator	Display
29	5431.	Horizontal Counter	Display
30	5432.	Horizontal DAC	Display
31	54321.	Horizontal Vector Filter	Display
32	6.	Horizontal Output	Display
33	61.	Waveform Data Bus	Display
34	62.	Vertical DACs	Display
35	621.	Vertical Expand	Display
36	63.	Vertical Vector Filter	Display
37	631.	Vertical Output	Display
38	632.	Z Axis	Display
39	6321.	Time-Base Data Registers	Time Base
40	64.	Acquire Address Generator	Memory
41	641.	INS,SO, and EOA Flip-Flops	Time Base
42	642.	AWCK Generator	Time Base
43	6421.	Valid Sample Counter	Time Base
44	643.	Phase Clock Generator	Time Base
45	6431.	Trigger Data Registers	Trigger
46	6432.	Trigger Level DAC	Trigger
47	64321.	Trigger Generator	Trigger
48	65.	Post-Trigger Counter	Trigger
49	651.	Trigger Source/Coupling	Trigger

***Display code is shown by the lighted MEMORY DISPLAY pushbuttons.**

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TABLE 3-4 (CONT)
Self-Tests

Test Number	Display Code*	Name of Circuit Being Tested	Circuit Module
50	652.	Auto Trigger	Trigger
51	6521.	Fast Ramp	Trigger
52	653.	CH 1 Position	Preamplifier
53	6531.	CH 1 Step Attenuator	Preamplifier
54	6532.	CH 1 Decade Attenuator	Preamplifier
55	65321.	CH 1 5 mV/Div	Preamplifier
56	654.	CH 2 Position	Preamplifier
57	6541.	CH 2 Step Attenuator	Preamplifier
58	6542.	CH 2 Decade Attenuator	Preamplifier
59	65421.	CH 2 Invert	Preamplifier
60	6543.	CH 2 5 mV/Div	Preamplifier
61	65431.	CCD Signal-Driver	CCD
62	65432.	Multiplexer	CCD
63	654321.	A/D Converter	CCD

***Display code is shown by the lighted MEMORY DISPLAY pushbuttons.**

EAROM than the self-test. After the EAROM Test is finished, the current front-panel settings will be restored.

NOTE

The operating life of the EAROM is shortened by repeatedly storing data in the non-volatile part of its memory. This normally occurs only on power-down. Because the EAROM Extended Test simulates power-down, use the EAROM Extended Test sparingly. (The EAROM Self-Test does not affect the life of the EAROM.)

To select the EAROM Test via the front panel, proceed as follows:

1. Press *f*.
2. Press MENU/TEST. The oscilloscope mainframe will then display the Test Menu, and item 3 will be Extended Test. (If a submenu is displayed instead, press the MEMORY DISPLAY 6 button to display the Test Menu.)
3. Press the MEMORY DISPLAY 3 button to select the Extended Test submenu. Item 2 of the Extended Test submenu will be EAROM Test.
4. Press the MEMORY DISPLAY 2 button to start the EAROM test. The EAROM Test will take place and the result will be displayed in the prompt field as EAROM PASSED or EAROM FAILED.

GPIB Test

The GPIB Test routine will test the GPIB chip, which is U720 on the LED Board. It will not test the two driver ICs (U730 and U735). The GPIB test will put meaningless data on the bus, and may report false results if someone else is using the bus, so the bus connector should be removed before calling this routine.

The GPIB routine is selected via the front-panel Extended Test submenu. When the test is complete, the result will be displayed in the prompt field.

To select the GPIB Test via the front panel, proceed as follows:

1. Press *f*.
2. Press MENU/TEST. The host mainframe will then display the Test Menu, and item 3 will be Extended Test. (If a submenu is displayed instead, press the MEMORY DISPLAY 6 button to display the Test Menu.)
3. Press the MEMORY DISPLAY 3 button to select the Extended Test submenu. Item 1 of the Extended Test submenu will be GPIB Test.
4. Press the MEMORY DISPLAY 1 button to start the GPIB test. The GPIB Test will take place and the result will be displayed in the prompt field as GPIB PASSED or GPIB FAILED.

NOTE

If, after the 7D20 is powered ON, it is desired to have the GPIB Test running repetitively for trouble shooting. This can be accomplished by removing the Ext. Bus Exerciser hardware jumper on the MPU board, P510. This will cause the GPIB bus to run repetitively until the jumper (strap) is replaced, or the 7D20 is powered OFF.

The GPIB test routine is as follows:

1. Software resets GPIB chip U720, and enables a byte-out (BO) interrupt.

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3. Enter talk-only mode.
4. Check for IRQ.
5. Write $FE to Data Out register.
6. Check contents of Data Out register by echoing back through the Command Pass Through register.
7. Repeat parts 5 and 6 while "walking" the zero-bit through the data lines.
8. Reconfigure GPIB chip U720 for normal operation (use a software reset, load the address register, etc.).

Front-Panel Test

To test the front-panel buttons and the LEDs that light them, proceed as follows:

1. Press *f*.
2. Press MENU TEST. The host mainframe will then display the Test Menu, unless one of its submenus was in use when the Test Menu was last used. If this happens, item 6 of the submenu will be TEST MENU. Press the MEMORY DISPLAY 6 pushbutton to cause the 7D20 to display the Test Menu.

   Item 3 of the Test Menu will be *EXTENDED TEST*.
3. Press the MEMORY DISPLAY 3 button. The host mainframe will then display the Extended Test submenu, and Item 3 will be FRONT PANEL TEST.
4. Press the MEMORY DISPLAY 3 button. The Front-Panel Test will start. The LEDs for all the front-panel pushbuttons, except MENU/TEST, will light. The MENU/TEST LED will blink. Pressing each pushbutton will change its state. To exit the Front-Panel Test, press the MENU/TEST button. The 7D20 will then initialize to the state it had before the Front-Panel Test, and the Test Menu will not be displayed.

TROUBLESHOOTING MODULES

This procedure uses Circuit Exercise (CE) mode to repetitively stimulate a circuit so that its output will be repeatable. The circuit output can be analyzed with a signature analyzer, or by using an oscilloscope to check waveforms against those given here. The technician will need to refer to the Theory of Operation (Section 2 of this manual) and the schematic diagrams to determine the problem.

To facilitate troubleshooting, the stimulus for individual CE tests is the same as the stimulus used for the corresponding Self-Test. No additional test equipment is needed to provide the stimulus; it is provided by the 7D20 firmware. Each CE test isolates a block of circuitry so that the technician can concentrate on troubleshooting without having to determine a method of isolating or stimulating the defective module.

In the past, when using self-tests to isolate defective circuits, the troubleshooting procedure chosen sometimes involved a different stimulus than the test that located the trouble. The danger in using different methods to locate and troubleshoot a problem is that when the method of troubleshooting is different, it can indicate that no problem exists. A superior method is using the same stimulus to locate and to troubleshoot difficulties.

Some troubles may occur that are more easily diagnosed with the 7D20 in its normal mode of operation. For example, if Test 13 fails it means there is trouble in the Power Supply. The technician will need to use a voltmeter to locate the faulty voltage, then diagnose the cause.

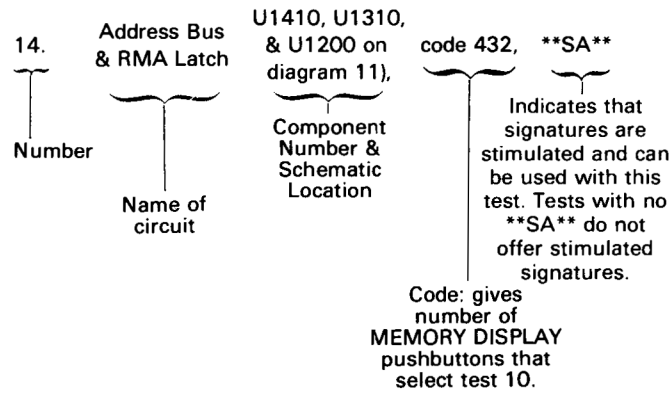
For those new to signature analysis, the discussion "Background Information on Signature Analysis," in this section, may be of interest.

The Troubleshooting Modules part concludes with details of what to do if the 7D20 does not respond to its front-panel controls.

CIRCUIT EXERCISE

Most of the 7D20 circuits can be diagnosed with the same stimulation used by the self-test routines. In circuit-exercise mode, any self-test routine can provide continuous stimulation while a technician probes the circuit.

The 63 self-tests are described after this discussion. The heading for each test includes the number, the name of the subject circuitry, component numbers and schematic location of the principal parts, the code (which MEMORY DISPLAY pushbuttons must be pressed to select that test), and whether the test offers signature analysis. For example, the entry for Test 14 is:



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To select a self-test in circuit-exercise mode, proceed as follows:

1. Press *f* MENU. The 7D20 will present the Test Menu on the crt of the host mainframe, and item 4 will be CIRCUIT EXERCISER. (If a submenu is displayed instead, press the MEMORY DISPLAY 6 button to display the Test Menu).

2. Press MEMORY DISPLAY 4 to select circuit exercise mode. The 7D20 will display

   REFER TO SERVICE MANUAL
   PRESS "*f* TEST" TO EXIT

   on the crt of the host mainframe. Table 3-4 gives the codes that designate the individual self-tests. Find the test codes here. If you want to leave the circuit-exercise mode before a test is started, press *f* TEST and the 7D20 will return to normal operation.

3. Select the desired test by pressing the MEMORY DISPLAY buttons. (For example, if you want to exercise the Block Select circuitry on the Memory Board, press MEMORY DISPLAY buttons 5, 4, 2, and 1. See the "Description of Circuit Exercises and Self Tests" heading, which follows, for details of the tests.) The buttons will light when pressed so you can verify the code you entered.

4. To start the test, press the COPY button. The test will run continuously. If the 7D20 passes the test, the COPY button will light. The CSW button will light and stay lighted even if only one failure occurs.

5. To stop the circuit-exercise test, press the CSW button. The 7D20 will return to normal operating mode.

Circuit tests with **SA** listed after their names can be used to stimulate digital circuitry that is being probed with a signature analyzer.

Signature tables are located in Section 7, Diagrams and Circuit Board Illustrations.

Routines that measure voltages or use timing loops cannot successfully use signature analysis. Both of these routines can take varying amounts of time, resulting in unstable signatures.

Description of Circuit Exercises and Self-Tests

1. PROM U400 (diagram 12), code 1

   Runs check-sum test—determines whether the PROM's content is intact and that it is in the correct socket.

   If this test fails, place the MPU Board (A9) on an extender and use the following Signature Analysis tests. Be sure to adhere to the setups for each table. SA Table 1.0 checks the address and control lines to the PROM. SA Table 1.1 verifies that the PROM is installed in the correct socket and that its contents are correct.

2. PROM U300 (diagram 12), code 2

   Runs check-sum test—determines whether the PROM's content is intact and that it is in the correct socket.

   If this test fails, place the MPU Board (A9) on an extender and use the following Signature Analysis tests. Be sure to adhere to the setups for each table. SA Table 1.0 checks the address and control lines to the PROM. SA Table 1.2 verifies that the PROM is installed in the correct socket and that its contents are correct.

3. PROM U200 (diagram 12), code 21

   Runs check-sum test—determines whether the PROM's content is intact and that it is in the correct socket.

   If this test fails, place the MPU Board (A9) on an extender and use the following Signature Analysis tests. Be sure to adhere to the setups for each table. SA Table 1.0 checks the address and control lines to the PROM. SA Table 1.3 verifies that the PROM is installed in the correct socket and that its contents are correct.

4. PROM U500 (diagram 12), code 3

   Runs check-sum test—determines whether the PROM's content is intact and that it is in the correct socket.

   If this test fails, place the MPU Board (A9) on an extender and use the following Signature Analysis test being sure to adhere to the setups for each table. SA Table 1.0 checks the address and control lines to the PROM. SA Table 1.4 verifies that the PROM is installed in the correct socket and that its contents are correct.

5. PROM U700 (diagram 12), code 31

   Runs check-sum test—determines whether the PROM's content is intact and that it is in the correct socket.

   If this test fails, place the MPU board (A9) on an extender and use the following Signature Analysis tests being sure to adhere to the setups for each table. SA Table 1.0 checks the address and control lines to the PROM. SA Table 1.5 verifies that the PROM is installed in the correct socket and that its contents are correct.

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6. PROM U600 (diagram 12), code 32

   Runs check-sum test—determines whether the PROM's content is intact and that it is in the correct socket.

   If this test fails, place the MPU board (A9) on an extender and use the following Signature Analysis tests being sure to adhere to the setups for each table. SA Table 1.0 checks the address and control lines to the PROM. SA Table 1.6 verifies that the PROM is installed in the correct socket and that its contents are correct.

7. RAM U900 (diagram 12), code 321

   Runs pseudo-random-byte-sequence (PRBS) twice; once straight and once complemented.

   If this test fails, place the MPU board on an extender and use Signature Analysis Table 1.0 to check the address and control lines to the RAM.

8. RAM U800 (diagram 12), code 4

   Stores contents of U800 in U900, then runs pseudo-random-byte-sequence (PRBS) twice as in Self-Test 7. When complete, replaces U800's original contents.

   If this test fails, place the MPU board on an extender and use Signature Analysis Table 1.0 to check the address and control lines to the RAM.

9. EAROM (U100 on diagram 12), code 41

   Tests RAM part of EAROM by loading 1's and 0's into it (contents are first saved in U800 and U900). The test then loads the complement of the first pattern and tests the EAROM a second time. (The two patterns are hexadecimal A's and 5's.) The original contents are then retrieved from RAMs U800 and U900; check-sums verify that correct data is returned. If a new EAROM is installed, it will fail its first Self-Test because it will not have received good data until all six stored settings have been initialized and stored via the Master Menu Store command.

   If this test fails, first recall all six stored settings to check that they all contain valid data. If any of the stored settings are bad the EAROM may be aging and may need replacement. To check for aging, run the EAROM Extended Test. The EAROM Extended Test is described in the Extended Test part of Testing Modules, in this section.

NOTE

The operating life of the EAROM is shortened by repeatedly storing data in the non-volatile part of its memory. This normally occurs only on power-down. Because the EAROM Extended Test simulates power-down, use the EAROM Extended Test sparingly. (The EAROM Self-Test does not affect the life of the EAROM.)

If all stored settings are bad, place the MPU Board on an extender and use the following Signature Analysis (SA) test. SA Table 1.0 will check the address and chip select lines to the EAROM.

10. A/D Converter (U525 on diagram 12), code 42

    This test checks that the ADC takes between 1 and 6 ms to make a conversion. If not, test indicates an error. If the conversion time is within limits, the test checks the ADC's conversion accuracy by reading the Gnd and +2.5 V potentials with results accurate to ± 10%. If not, test indicates an error.

    If this test fails, place the MPU Board on an extender and run circuit exercise 42. Use an oscilloscope to troubleshoot the indicated circuitry. The SA Start/Stop line provides a stable oscilloscope trigger.

11. Ch 1 Position DAC (U320 on diagram 12), code 421

    This test loads Ch 1 Position DAC with test pattern, sets MPU Board's analog multiplexer so that ADC will read Ch 1 Position DAC. The result is compared with test limits.

    If this test fails, place the MPU Board on an extender and run circuit exercise 421. Use an oscilloscope to troubleshoot the indicated circuitry. Waveform Figure 3-11 illustrates a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger.

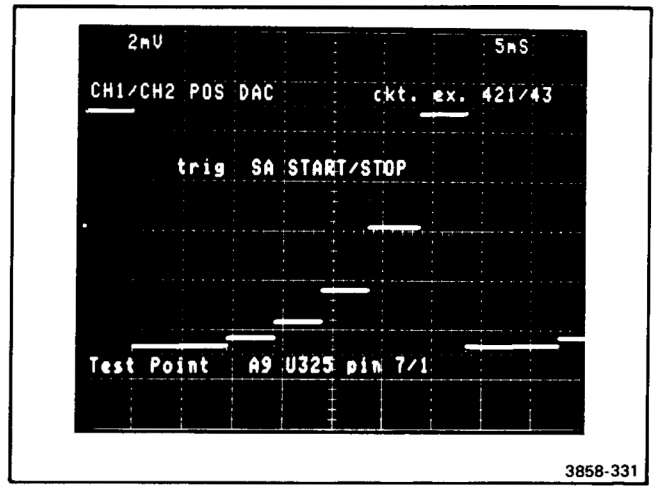

Figure 3-11. Waveform for Ch 1/Ch 2 Position test.

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12. Ch 2 Position DAC (U420 on diagram 12), code 43

    Same Self-Test as for test 11, Ch 1 Position DAC.

    If this test fails, place the MPU Board on an extender and run circuit exercise 43. Use an oscilloscope to troubleshoot the indicated circuitry. Waveform Figure 3-11 illustrates a typical output of this test. The SA Start/Stop line will provide a stable oscilloscope trigger.

13. Power Supply (on diagram 10), code 431

    This test reads scaled Power Supply voltages via A Bus multiplexer U610 on diagram 10. The test then compares the result with test limits (±3%; all power supply voltages are scaled to +4 V).

    If this test fails, place the Power Supply Board (A7) on an extender and run circuit exercise 431. Use an oscilloscope to troubleshoot the indicated circuitry. The SA Start/Stop line provides a stable oscilloscope trigger for viewing test output.

14. Address Bus & RMA Latch (U1410, U1310, U 200 on diagram 11), code 432, **SA**

    This test checks for short circuits between the data and address lines of the waveform memory. Test 14 has the following steps:

    a. Set the Processor Read/Write Select (PRWS) line low to select memory during acquire cycles.

    b. Set Read Memory Address (RMA) mode to latch row activity during an acquire cycle.

    c. Write a walking-zero address pattern to waveform memory, starting at address $3FFE.

    d. Check the contents of the RMA.

    e. Set RMA mode to latch column A of MPU activity, then repeat steps c and d.

    f. Set RMA mode to latch row A of MPU activity, then repeat steps c, d, and e, thirteen times. This "walks" the zero through all 14 address bits.

    (The zero is also walked through the Data Bus for Signature Analysis.)

    If this test fails, place the Memory Board on an extender and run circuit exercise 432. Use the following Signature Analysis tests. SA Table 3.0 verifies the address lines and MPU control lines on the board. SA Table 3.1 verifies the MA (memory address) bus lines. If these signatures are wrong it may be necessary to use an oscilloscope to troubleshoot the Memory Timing and Synchronization circuitry. SA Table 3.2 verifies the Data Bus from the MPU to the Memory Board.

15. Display Address Generator (DAG; U700, U600, U500, diagram 11), code 4321, **SA**

    This test checks that the DAG loads correctly and that the address reaches its destination. Test 15 has the following steps:

    a. First, set the $\overline{\text{DAGSSE}}$ (Display Address Generator Single-Step Enable) line low so that the DAG will not count.

       Then, strobe the $\overline{\text{End Display Cycle}}$ line via U1400 on diagram 8. Along with clearing Refresh, this places the DAG in a stable mode for loading.

    b. Load DAG with 001.

    c. Check contents of DAG via Read Memory Latch (RMA) U200 on diagram 11. This requires two reads of the RMA Latch (one of y row and one of y column).

    d. Repeat steps b and c, "walking" the one-bit through all DAG Bits.

    If this test fails, place the Memory Board on an extender and run the circuit exercise indicated by the Signature Table used. SA Table 4.0 will verify the Display Address Generator and its MPU control. SA Table 3.2 verifies the Data Bus from the MPU to the Display Address Generator. If the signatures are correct and the test still fails, the trouble is probably in the Display/Acquire Address Multiplexer or its control.

16. Display Address Generator (DAG) Normal Clocking (U700, (U600, U500, diagram 11), code 5

    This test presets the DAG to zero, then clocks it with 400 kHz for 3 ms and reads the resultant count via the RMA. A comparison with the desired count will tell whether the DAG is counting correctly. Test 16 has the following steps.

    a. Set the $\overline{\text{DAGSSE}}$ (Display Address Generator Single-Step Enable) line low to disable normal clocking of the DAG.

    b. Strobe the $\overline{\text{End Display Cycle}}$ line via U1400 on diagram 8, and Clear Refresh. This places the DAG in a stable mode for loading (counter must not be enabled during loading).

    c. Load DAG with zero.

    d. Set Refresh and clear $\overline{\text{DAGSSE}}$. This enables the counter and permits normal (Refresh) counting.

    e. Wait 3 ms.

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f. Read contents of DAG via Read Memory Address (RMA) latch U200 on diagram 11. This requires two reads of the RMA latch (one of y row and one of y column).

g. Compare reading with test limits.

If this test fails, place the Memory Board on an extender and run circuit exercise 5. Use an oscilloscope to check that the Display Address Generator is counting properly, at a 400 kHz rate. (Check the 10 outputs, from LSB to MSB, to see that each one counts at half the rate of its less-significant neighbor.) The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test.

17. Data Bus and RMD Latch (U1600, U1700, U300, diagram 11), code 51

This test checks the ability of the microprocessor unit (MPU) to write to the memory data (MD) bus. Test 17 has the following steps:

a. Set the Processor Read/Write Select (PRWS) line low to select memory during acquire cycles.

b. Set the Read Memory Address (RMA) mode to column A of MPU (the RMA and Read Memory Data (RMD) latches will latch MPU acquire cycle activity).

c. Write $FE to address $3FFF.

d. Read content via RMD latch U300.

e. Repeat steps c and d while "walking" the zero-bit through the data lines.

If this test fails, place the Memory Board on an extender and run the circuit exercise indicated by the Signature Table used. SA Table 3.1 verifies the MD (memory data) and MPU data buses. If SA Table 3.1 signatures are bad SA Table 3.2 verifies the data bus to the Data Multiplexer. If the signatures are good and circuit exercise 51 fails, the problem is in the RMD latch or its control.

18. Waveform Memory Select (WMS) Generator (U1420B, U820A, U1520B, U720A, U620D on diagram 11), code 52

This test ascertains if the microprocessor unit (MPU) writes to waveform memory using only acquire cycles if so instructed and only display cycles if so instructed. Test 18 includes the following steps:

a. Set the Processor Read/Write Select (PRWS) line low so that the MPU accesses waveform memory during acquire cycles. Set the Read Memory Address (RMA) mode to Column A of the MPU (it latches only MPU acquire-cycle activity).

b. Write $AA to location $3FFF.

c. Read the Read Memory Data (RMD) latch, U300, to compare the RMD contents with $AA.

d. Set PRWS line high so that MPU access is selected during display cycles.

e. Write $55 to location $3FFF.

f. Read the RMD latch to compare RMD contents with $AA. It should be $AA, not $55. If the MPU did access the Memory Board during a display cycle, the RMD latch that is set to acquire cycles will not change.

g. Set RMD mode to Column D of MPU (it latches only MPU display cycle activity).

h. Write $C3 to location $3FFF.

i. Read the RMD latch to compare its contents with $C3.

j. Set the PRWS line low to select MPU waveform memory access during acquire cycles.

k. Write $3C to location $3FFF.

l. Read the RMD latch to compare its contents with $C3. If the MPU accessed the Waveform memory during an acquire cycle the RMD, that is set to display cycles, will not change.

If this test fails, place the Memory Board on an extender and run circuit exercise 52. Use an oscilloscope to troubleshoot the indicated circuitry. Compare the waveform with the one shown in Figure 3-12. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test.

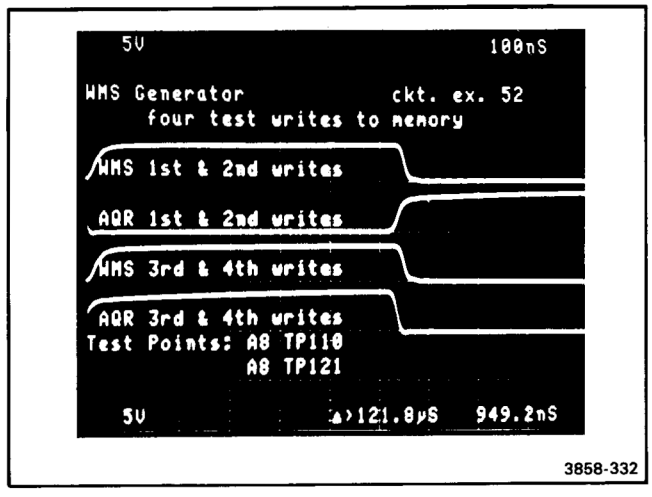

Figure 3-12. Waveform for WMS Generator test.

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19-26. Waveform RAMs 1-8 (U910, code 521; U810, code 53; U710, code 531; U610, code 532; U510, code 5321; U410, code 54; U310, code 541; U210, code 542; on Memory Board, diagram 11)

This test checks that all storage locations of the memory are good. A pseudo-random byte sequence (PRBS) is stored in memory during acquire cycles, then read out and compared with the original PRBS. This process is then repeated with complemented data during display cycles to verify that it then reads out complemented data. The tests consist of the following steps:

a. Set the $\overline{\text{AAGSSE}}$ (Acquire Address Generator Single-Step Enable) line low to prevent writing to memory during acquire time.

b. Set the processor read/write select (PRWS) line low to select memory during acquire time.

c. Write pseudo-random byte sequence (PRBS) to all RAMs.

d. Check content of the RAM under test.

e. Set the PRWS line high to select memory during display time.

f. Complement the data in all RAMs.

g. Check content of the RAM under test.

If this test fails, place the Memory Board on an extender and run circuit exercise 432. SA Table 3.1 verifies the MA and MD buses and control lines to the waveform RAMS. If the signatures are good, the problem is probably in the RAM chip or the waveform data (WD) bus and its control.

27. Block Select (U800 on diagram 11), code 5421

This test checks register file U800, on diagram 11, for correct address selection and bit integrity of its four-by-four matrix structure. Test 27 consists of the following steps:

a. Load the block-select file (Dispblk X, Dispblk Y, Aqrblk 1, and Aqrblk 2) with $0F, $0F, $0F, and $0E.

b. Check the contents of the block-select file with the RMA latch. Four read operations of the RMA are necessary (X Col, Y Col, Ch 1 Col, and Ch 2 Col modes are read).

c. Repeat steps a and b while "walking" the zero-bit through all 16 positions in the file.

If this test fails, place the Memory Board on an extender and run circuit exercise 5421. Use an oscilloscope to verify the control lines to U800, the Block Select IC. SA Table 3.2 verifies the Data Bus to the Block Select. SA Table 3.1 verifies the MD (memory data) bus to, not the output of, the Block Select circuit.

28. Display Interrupt Generator (U500A, U500B, U1600E, on diagram 8), code 543

This test checks that strobing the $\overline{\text{End Display Cycle}}$ signal will reset Display Interrupt Generator U500B, on diagram 11, which will assert a low on the $\overline{\text{DISPINTR}}$ line. The $\overline{\text{DISPINTR}}$ line is tested in two places. First, it is tested on the Memory Board via the RMA latch; and second, $\overline{\text{DISPINTR}}$ is tested on the MPU Board by enabling the FIRQ (Display Interrupt) to the processor and checking for the correct response. The $\overline{\text{DISPINTR}}$ line is then set high by strobing START DISPLAY CYCLE and repeating the same two tests.

a. Force display to end by asserting a low on $\overline{\text{End Display Cycle}}$.

b. Check that the $\overline{\text{DISPINTR}}$ line is low via a read memory address (RMA) on the Memory Board.

c. Enable Fast Interrupt Request (FIRQ) mode and check that the MPU actually handled the interrupt.

d. Assert a low on $\overline{\text{Display Length Counter Single Step}}$, and start the display with a low on $\overline{\text{Start Display Cycle}}$. This puts the display in a "display-forever" mode.

e. Via the RMA Latch, check that the $\overline{\text{DISPINTR}}$ line is high.

f. Enable FIRQ mode and check that MPU did not handle the interrupt.

g. Disable FIRQ.

If this test fails, place the Display Board on an extender and run circuit exercise 543. Use an oscilloscope to troubleshoot the Display Interrupt Generator.

If the front-panel controls do not function, you will not be able to start a circuit exercise. In this event, run the External Bus Exercise routine and use an oscilloscope to troubleshoot the Display Interrupt Generator. (For information about External Bus Exercise, see WHAT TO DO IF 7D20 DOES NOT RESPOND TO FRONT-PANEL CONTROLS, in this section.) The SA Start/Stop line will provide a stable trigger while using the External Bus Exercise for troubleshooting.

29. Horizontal Counter (U120A, U120B, U200A, U200B, also U310, U210, U100C), code 5431

This test checks that $\overline{\text{DISPINTR}}$ occurs after the appropriate number of clocks for 1024- and 820-point displays, respectively. The test then sets HMAG

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mode and again checks for DISPINTR. Test 29 includes the following steps:

a. Force display to end by asserting a low on End Display Cycle.

b. Select a 1024-point display.

c. Assert a low on Start Display Cycle to start the display.

d. Measure the time from start of display until a low occurs on DISPINTR, and compare that time with test limits.

e. Repeat steps a-d for an 820-point display.

f. Repeat steps a-d for a horizontally magnified 820-point display.

g. Repeat steps a-d for a horizontally magnified 1024-point display.

If this test fails, place the Display Board on an extender and run circuit exercise 5431. Use an oscilloscope to troubleshoot the Horizontal Counter. Waveform Figure 3-13 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

30. Horizontal DAC (U720, U1020, U820, U320, U520, U620, diagrams 8 & 9), code 5432
31. Vector Filter (U1215, U1325, diagram 9), code 54321
32. Horizontal Output (U230B, U230A, diagrams 9 & 13), code 6

These tests furnish different digital inputs to test the Horizontal DAC's conversion accuracy, and to check the operation of the Horizontal Vector Filter and the Horizontal Output circuit. Although the three tests are usually run sequentially in self-test, a single test can be made as a circuit exercise. The tests stimulate the inputs as given in Table 3-5. The test 30, 31, and 32 sequence consists of the following steps:

a. Assert End Display Cycle to reset the display length counter (DLC).

b. Set DLC to self-test mode by selecting Display Length Counter Single Step as the clock source.

c. Disable the front-panel HORIZ POSITION control by setting the Horiz Pos line low.

d. Select a Y-T display by setting YT/XY high.

e. Start a display by asserting the Start Display Cycle level. (Removes the reset from the counter.)

f. As listed in Table 3-5, stimulate the Clock, 820 Gain Comp, and Dots lines; then make the designated checks.

30) Horizontal DAC (5432). If this test fails, place the Display Board on an extender and run circuit exercise 5432. Use an oscilloscope to troubleshoot the Horizontal DAC. Waveform Figure 3-14 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

31) Horizontal Vector Filter (54321). If this test fails, place the Display Board on an extender and run circuit exercise 54321. Use an oscilloscope to troubleshoot the Horizontal Vector Filter. Waveform Figure 3-15 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

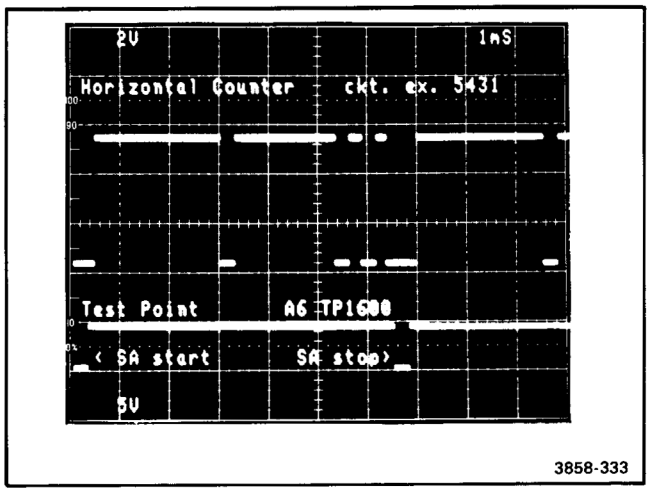

Figure 3-13. Waveform for Horizontal Counter test.

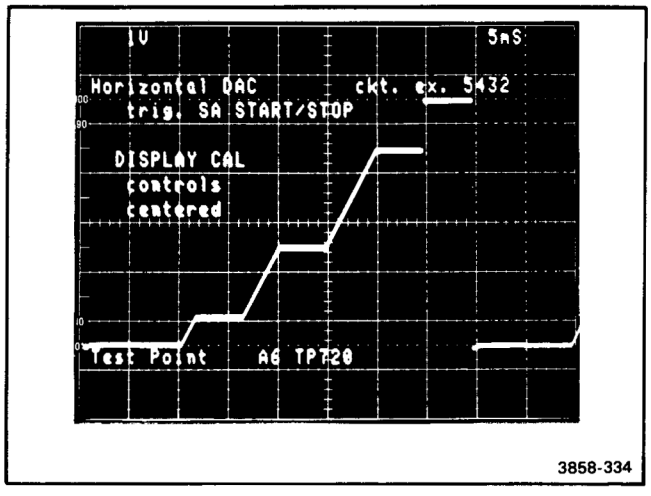

Figure 3-14. Waveform for Horizontal DAC test.

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TABLE 3-5
Stimulus and Checks for Horizontal Tests

Test/Step	Number of Clocks	820 Gain Comp	$\overline{\text{Dots}}$	Compare Voltage at	With
30 a	7	on	off	TP720	limits
30 b	7	off	off	TP720	a + offset
30 c	124	off	on	TP720	b + offset
30 d	413	off	on	TP720	c + offset
30 e	816	off	on	TP720	d + offset
30 f	816	on	off	TP720	e + offset
31 g	7	on	on	TP1421	limits
31 h	7	on	off	TP1421	g + offset
31 i	816	on	on	TP1421	h + offset
31 j	816	on	off	TP1421	i + offset
32 k	7	on	off	U230A-1	limits
32 l	816	on	off	U230A-1	k + offset

32) Horizontal Output (6). If this test fails, place the Display Board on an extender and run circuit exercise 6. Use an oscilloscope to troubleshoot the Horizontal Output. Waveform Figure 3-16 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

33. Waveform Data Bus (U420, U320, U520, U620, diagram 8), code 61
34. Vertical DACs (U410, diagram 8; U610, U700, U810, U905, U800, U810, diagram 9), code 62
35. Vertical Expand (U1100, Q1015, Q1001, U1010, diagram 9), code 621
36. Vertical Vector Filter (U1215, U1315, diagram 9), code 63
37. Vertical Output (U240A, U240B, diagrams 5 & 9), code 631

These tests supply different data to various circuits to test the continuity, conversion accuracy, expansion accuracy, action of the Vector Filter, and operation of the Vertical Output. Although the five tests are run sequentially by self-test, an individual test can be made as a circuit exercise. The tests stimulate the inputs as given in Table 3-6. The test 33-37 sequence consists of the following steps:

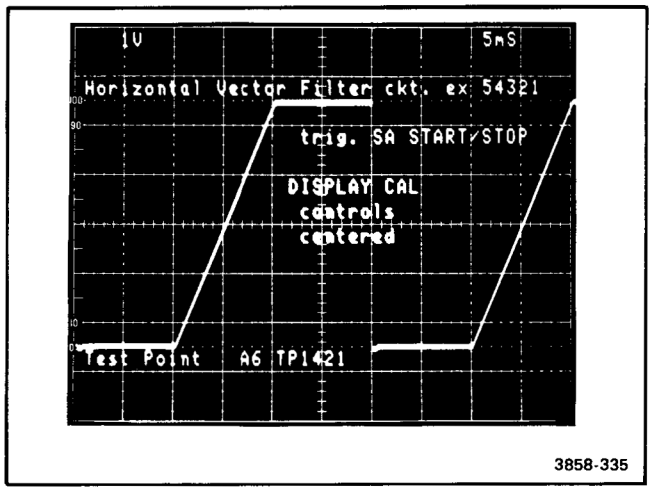

Figure 3-15. Waveform for Horizontal Vector filter test.

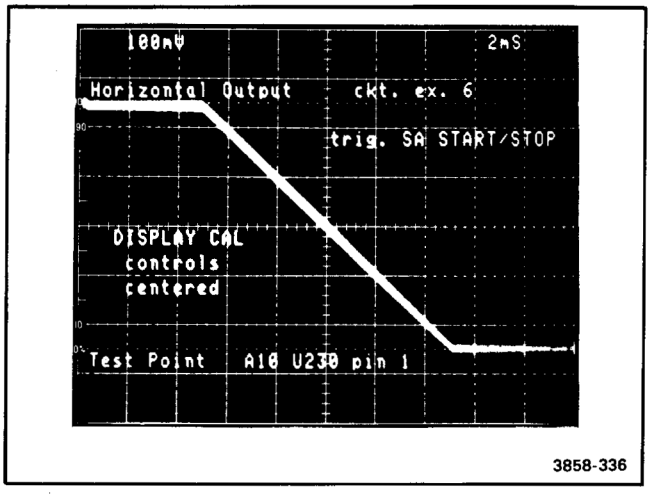

Figure 3-16. Waveform for Horizontal Output test.

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a. Set $\overline{\text{AAGSSE}}$ (Acquire Address Generator Single Step Enable) low to prevent acquire writes.

b. Set $\overline{\text{DAGSSE}}$ (Display Address Generator Single Step Enable) low to prevent the display address generator from being clocked.

c. Assert a low on YT/$\overline{\text{XY}}$ (U1305 pin 9 on diagram 8) for an X-Y display.

d. Disable front-panel HORIZ POSITION control and 820 Gain Compensation.

e. Set DISPBLKX (display block x) and DISPBLKY (display block y) to $0000.

f. Clear the display address generator. The display now comes from data stored in waveform memory location $0000.

g. As listed in Table 3-6, provide display data and control the Vertical Expand, Vertical Display Offset, and $\overline{\text{Dots}}$ inputs; then make the designated comparisons.

TABLE 3-6
Stimulus and Checks for Vertical Tests

Test/Step	Display Data	Vertical Expand	Vertical Display Offset	$\overline{\text{Dots}}$	Compare Voltage at	With
33 a	0F	x1	80	on	TP720	limits
33 b	6A	x1	80	on	TP720	a + offset
33 c	C3	x1	80	on	TP720	b + offset
33 d	F0	x1	80	on	TP720	c + offset
e	0F	x1	80	on	TP900	limits
34 f	6A	x1	80	on	TP900	e + offset
34 g	C3	x1	80	on	TP900	f + offset
34 h	F0	x1	80	on	TP900	g + offset
34 i	80	x1	0F	on	TP900	h + offset
34 j	80	x1	6A	on	TP900	i + offset
34 k	80	x1	C3	on	TP900	j + offset
34 l	80	x1	F0	on	TP900	k + offset
34 m	00	x1	80	on	TP900	l + offset
34 n	00	x0.5	80	on	TP900	m + offset
34 o	00	x0.4	80	on	TP900	n + offset
34 p	00	x0.25	80	on	TP900	o + offset
q	00	x0.20	80	on	TP900	p + offset
35 r	66	x1	80	on	U1010 pin 6	limits
35 s	66	x2	80	on	U1010 pin 6	r + offset
35 t	66	x2.5	80	on	U1010 pin 6	s + offset
35 u	66	x4	80	on	U1010 pin 6	t + offset
35 v	66	x5	80	on	U1010 pin 6	u + offset
35 w	00	x5	80	on	U1010 pin 6	v + offset
35 x	FF	x5	80	on	U1010 pin 6	w + offset
36 y	00	x1	80	on	TP1240	limits
36 z	00	x1	80	off	TP1240	y + offset
36 aa	FF	x1	80	off	TP1240	z + offset
36 bb	FF	x1	80	on	TP1240	aa + offset
37 cc	00	x1	80	on	U240B-7	limits
37 dd	FF	x1	80	on	U240B-7	cc + offset

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33) Waveform Data Bus (61). If this test fails, place the Display Board on an extender and run circuit exercise 61. Use an oscilloscope to troubleshoot the Waveform Data Bus. Waveform Figure 3-17 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

34) Vertical DAC (62). If this test fails, place the Display Board on an extender and run circuit exercise 62. Use an oscilloscope to troubleshoot the Vertical DAC. Waveform Figure 3-18 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

35) Vertical Expand (621). If this test fails, place the Display Board on an extender and run circuit exercise 621. Use an oscilloscope to troubleshoot the Vertical Expand. Waveform Figure 3-19 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

36) Vertical Vector Filter (63). If this test fails, place the Display Board on an extender and run circuit exercise 63. Use an oscilloscope to troubleshoot the Vertical Vector Filter. Waveform Figure 3-20 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

37) Vertical Output (631). If this test fails, place the Display Board on an extender and run circuit exercise 631. Use an oscilloscope to troubleshoot the Vertical Output. Waveform Figure 3-21 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

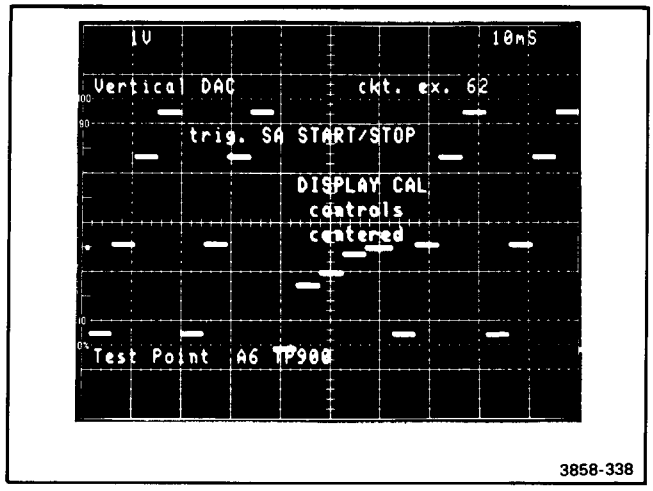

Figure 3-18. Waveform for Vertical DAC test.

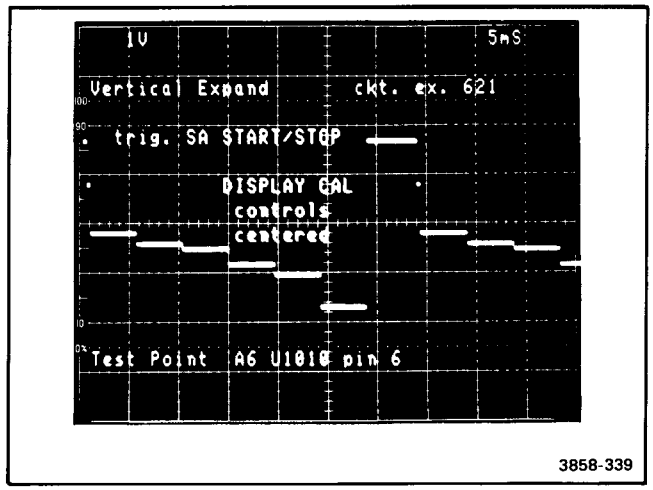

Figure 3-19. Waveform for Vertical Expand test.

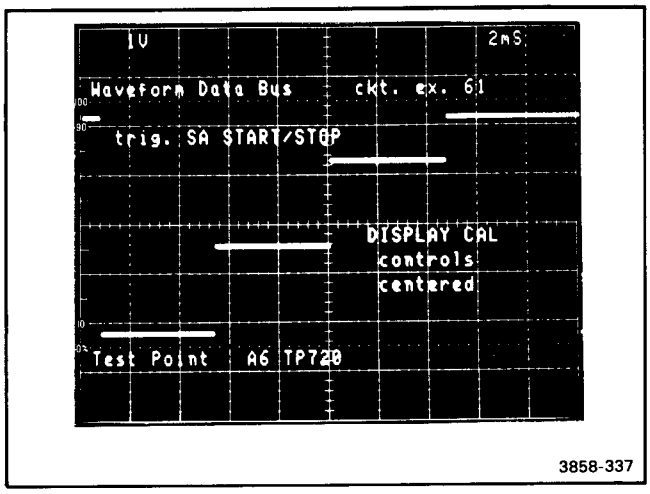

Figure 3-17. Waveform produced by Waveform Data Bus test.

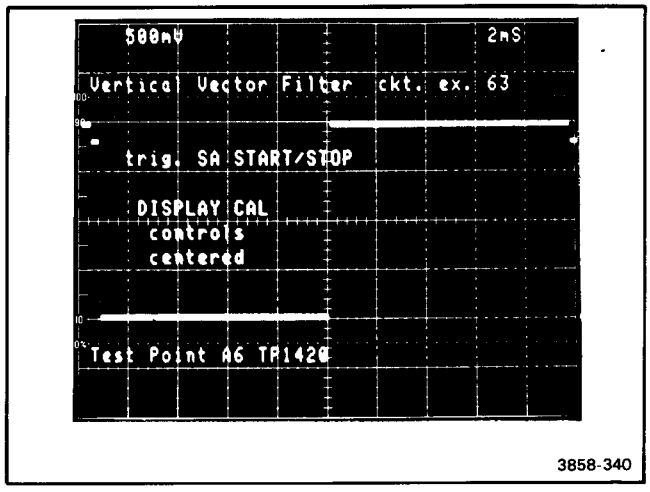

Figure 3-20. Waveform for Vertical Vector Filter test.

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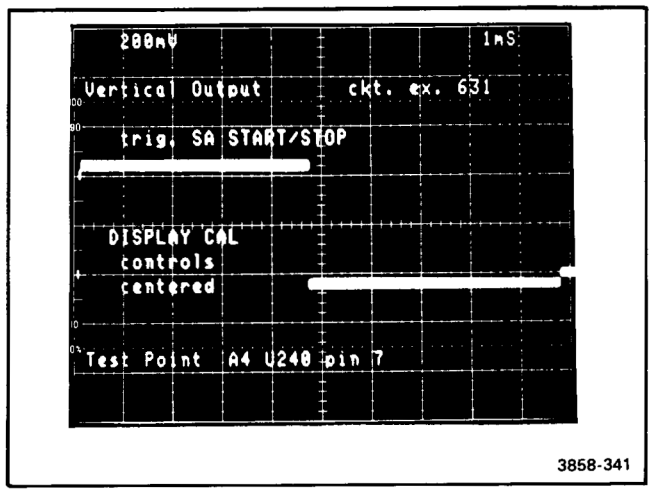

Figure 3-21. Waveform for Vertical Output test.

38. Z-Axis (U510, U200B, U1500A, U1600F, U300A,B,D, U100A,D, Q110, diagrams 8 and 13), code 632

This test checks that the Blanking Logic circuit can be controlled by $\overline{\text{DISPINTR}}$ (Display Interrupt), $\overline{\text{Blank}}$, $\overline{\text{Dots}}$, and $\overline{\text{CHBLNK}}$ (Character Blank) with data from memory. Test 38 consists of the following steps:

a. Set the $\overline{\text{AAGSSE}}$ (Acquire Address Generator Single-Step Enable) line low to prevent acquire writes.

b. Assert a low on $\overline{\text{End Display Cycle}}$ to force a $\overline{\text{DISPINTR}}$.

c. Clear:
- the $\overline{\text{Blank}}$ line,
- the $\overline{\text{FSBLANK}}$ line,
- the $\overline{\text{Dots}}$ line, and
- the Display Address Generator.

d. Assert a low on $\overline{\text{DAGSSE}}$ (Display Address Generator Single-Step Enable) to prevent normal clocking from incrementing the DAG.

e. Load display block Y (DISPLYBLK Y) with $00 (use address $0000 in waveform RAM).

f. Check that the Aux Z Axis line is high for between-displays blanking.

g. Strobe the Start Display cycle line to start the display. This will clear the $\overline{\text{DISPINTR}}$ line.

h. As listed in Table 3-7, provide display data and control the $\overline{\text{Blank}}$, $\overline{\text{CHBLNK}}$ (Character Blank), and $\overline{\text{Dots}}$ lines, then check the duty cycle of the Aux Blank signal.

TABLE 3-7
Stimulus and Outputs for Z-Axis Tests

Display Data	$\overline{\text{Blank}}$	$\overline{\text{FSBlank}}$	$\overline{\text{Dots}}$	AuxBlank Duty Cycle
FF	on	off	off	100%
FF	off	off	on	50%
FF	off	off	off	25%
FE	off	on	off	25%
FD	off	on	off	25%
FB	off	on	off	25%
F7	off	on	off	25%
FE	off	on	off	25%
DF	off	on	off	25%
BF	off	on	off	100%
7F	off	on	off	100%

If this test fails, place the Display Board on an extender and run circuit exercise 632. Use an oscilloscope to troubleshoot the Z-Axis. Waveform Figure 3-22 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

39. Time Base Data Registers (U1710, U1610, U1510, U1310, U1320, U1210, and U110B on diagram 15), code 6321, **SA**

This test checks that data can be transferred both to and from the Time Base Data Registers. Test 39 has the following steps:

a. Shift data from ROMs to data registers.

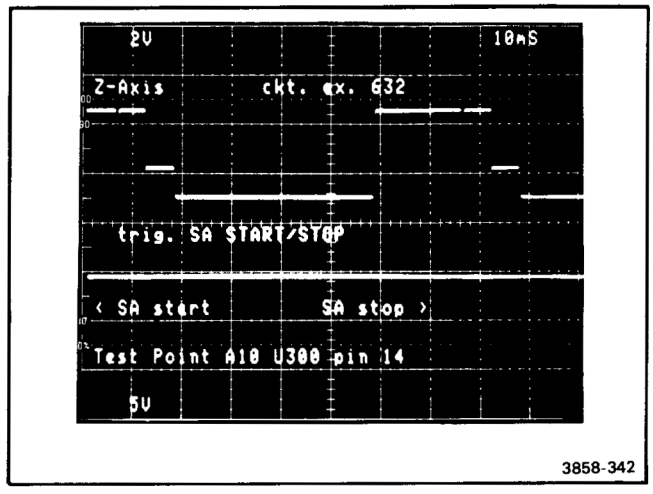

Figure 3-22. Waveform for Z-Axis test.

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b. Produce a serial data strobe, SDS. (This is for signature analysis of the outputs.)

c. Shift data out of data registers and compare it with ROM data.

d. Repeat steps a through c 16 times.

If this test fails, troubleshoot the Timebase Board using circuit exercise 6321. SA Table 6.0 verifies the controls and outputs of the serial bus.

40. Acquire Address Generator (AAG; U900, U1100, U1000 on diagram 11), code 64, **SA**

This test circulates a zero through the AAG. Test 40 consists of the following steps:

a. Assert a low on $\overline{\text{AAGSSE}}$ (Acquire Address Generator Single-Step Enable) to enable single-step operation.

b. Load $FE into the AAG (via $\overline{\text{ASA}}$).

c. Use the $\overline{\text{AAGSS}}$ (Acquire Address Generator Single Step) line to clock the AAG.

d. Use two Read Memory Address (RMA) operations for Ch 1 row and Ch 1 column to check the contents of the AAG.

e. Repeat steps a-d while "walking" the zero-bit through the preset range.

If this test fails, troubleshoot the Memory Board using circuit exercise 64. SA Table 5 verifies Acquire Address Generator and its MPU control; SA Table 3.2 verifies the Data Bus from the MPU to the Acquire Address Generator. If the signatures are correct and the test still fails, the trouble is probably in the Display/Acquire Address Multiplexer or its control.

41. INS, SO, and EOA Flip-Flops (U1200B, U910B, and U910A on diagram 15), code 641, **SA**

INS, SO, and EOA stand for input strobe, slow out, and end-of-acquire. This test checks that the flip-flops that activate the INS, SO, and EOA lines on the Timebase Board operate correctly. Test 41 has the following steps:

a. Set the FISO line (fast in, slow out; on the Time Base) high to indicate 200 μs to 50 ns/division range,

b. Set free run.

c. Set Acquire Address Generator Single-Step Enable (AAGSSE) to permit the acquire address generator (U900, U1000, U1100 on diagram 11) to be incremented by Acquire Address Generator Single Step (AAGSS),

d. Set post-trigger counter (U1300, U1400, U1500, U1600, U1700) to 7FFFF.

e. Load FF into the acquire address generator.

f. Produce Initialize new Acquire (AQRINIT) strobe (from U1010D on diagram 15).

g. Within 40 μs of AQRINIT, latch U1320 and U1210, shift data out and check that the INS line is high and that the SO and $\overline{\text{ENDACQ}}$ (End of Acquire) lines are low.

h. One hundred milliseconds after AQRINIT, Latch U1320 and U1210, and check that the INS and $\overline{\text{ENDACQ}}$ lines are low and that the Slow Out (SO) line is high.

i. Clock the acquire address generator with AAGSS. This sets MEA high. (MEA means memory end acquire.)

j. Latch U1320 and U1210 and check that the INS and $\overline{\text{ENDACQ}}$ lines are low and that SO is high.

k. Set the Fast In, Slow Out (FISO) and Extended Real-Time (ERD) lines low.

l. Set the AWCK (acquire write clock) to select the 400 kHz signal as the AW source.

m. Set post-trigger counter to 7FFFF.

n. Produce an AQRINIT strobe.

o. Within 2 ms of AQRINIT, latch U1320 and U1210.

p. Check that the INS and SO lines are high, and that $\overline{\text{ENDACQ}}$ is low.

q. Three milliseconds after AQRINIT. Latch U1320 and U1210 and Check that the INS, SO, and $\overline{\text{ENDACQ}}$ lines are low.

If this test fails, troubleshoot the Timebase Board using circuit exercise 641. SA Table 7 verifies the operation of the flip-flops. If signatures around the Post Trigger Counter are wrong, SA Table 6 verifies the Serial Bus for proper operation. If an oscilloscope is used to troubleshoot the circuit, Waveform Figure 3-23 shows normal operation of the flip-flops in this test. The SA Start/Stop line provides a stable oscilloscope trigger while this test is used for troubleshooting.

42. Acquire Write Clock (AWCK) Generator (U900, U500A, U500B, U600A, U600B, U800 on diagram 14), code 642

This test checks that the frequency of the AWCK signal is within test limits. Eight frequencies (400,

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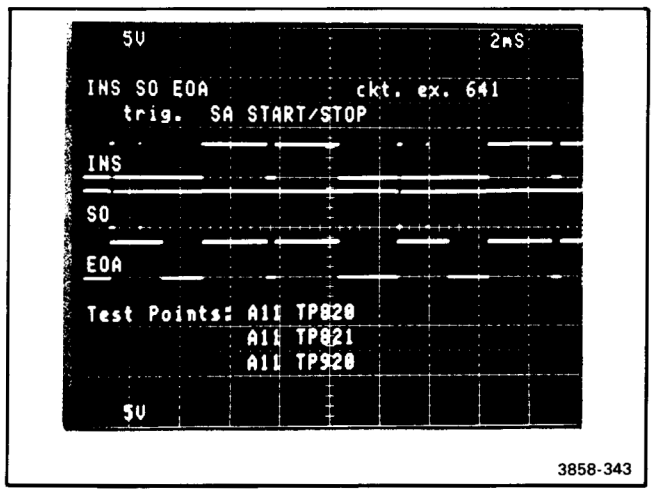

Figure 3-23. Waveform for INS, SO, and EOA tests.

200, 100, 50, 20, and 2 kHz, 200 Hz and 20 Hz) are checked. Test 42 consists of the following steps:

a. Select 400 kHz as AWCK frequency and set FISO low.

b. Prevent any clocks to the Acquire Address Generator (AAG) with a low on $\overline{\text{AAGSSE}}$ (Acquire Address Generator Single Step Enable).

c. Initialize the AAG by loading it with $000.

d. Initialize the post-trigger/valid sample counter to ensure the AWCK does not terminate during the test.

e. Establish time for wait loop to <1000 counts.

f. Enable clocks to the AAG with a high on $\overline{\text{AAGSSE}}$. This lets the AAG start counting.

g. Wait for time specified in step e, then stop AAG with a low on $\overline{\text{AAGSSE}}$.

h. Read AAG via the Read Memory Address (RMA) latch—compare count with test limits.

i. Repeat steps a-h for 200, 100, 50, 20, and 2 kHz, 200 Hz and 20 Hz.

If this test fails, troubleshoot the Timebase Board using circuit exercise 642. Use an oscilloscope to look for missing or incorrect clock rates. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

43. Valid Sample Counter (U1300, U1400, U1500, U1600, and U1700 on diagram 15), code 6421

This test verifies that the post-trigger/valid-sample counter functions properly through a trigger reset mode. Test 43 has the following steps:

a. Select 400 kHz Acquire Write Clock (AWCK) frequency and set Fast In, Slow Out (FISO) low.

b. Initialize the valid-sample counter. (STROBE, $\overline{\text{INIT}}$ U1010B)

c. Latch U1320 and U1210 just prior to the time that Trigger Reset (TRIGRST) should go low; check that it did not go low.

d. Repeat parts a and b, then latch U1320 and U1210 just after the time TRIGRST should go low; check that it did go low.

If this test fails, troubleshoot the Timebase Board using circuit exercise 6421. Use an oscilloscope to check that the Vaid Sample Counter counts properly to 1024 and that the counter is then loaded. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

44. Phase Clock (PCK) Generator (U1630, U1520B, U1730, U1530, U1520A, U1420B, U1220A on diagram 14), code 643

This test verifies that the PCK is functional at its various rates. Test 44 has the following steps:

a. Select 200 kHz PCK frequency and set the Fast In, Slow Out (FISO) line high.

b. Initialize the post-trigger counter.

c. Delay the time from initialize until just before Trigger Reset (TRIGRST) should go low. Latch U1320 and U1210 (diagram 15), shift data out and check TRIGRST.

d. Repeat steps b and c, waiting until TRIGRST should be low.

e. Repeat steps a-d with 400 and 800 kHz, 2, 4, 8 and 20 MHz PCK frequencies.

If this test fails, troubleshoot the Timebase Board using circuit exercise 643. Use an oscilloscope to verify that all clock rates are present and have the correct rate. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

45. Trigger Data Registers (U101B, U101D, U210, U201, U200 on diagram 13), code 6431, **SA**

This test checks that data can be transferred both to and from the Trigger Data Registers. Test 45 has the following steps:

a. Shift data from ROMs to data registers.

b. Produce a serial data strobe, SDS. This makes signature analysis on outputs possible.

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c. Shift data out of the data registers and compare it with ROM data.

d. Repeat steps a-c 16 times.

If this test fails, place the Trigger Board on an extender and run circuit exercise 6431. SA Table 9.0 verifies the operation of the data registers.

46. Trigger Level DAC (U310 on diagram 13), code 6432

This test checks that the Trigger-Level digital-to-analog converter (DAC) gives the right output for four different digital inputs. Test 46 includes the following steps:

a. Clear peak-to-peak (P-P) mode by setting a low on the P-P output of U200.

b. Set Trigger level to $0F.

c. Read output of DAC U310 (TP400) via A bus.

d. Compare with test limits.

e. Repeat steps b-d for Trigger levels of $6A, $C3, and $F0.

If this test fails, place the Trigger Board on an extender and run circuit exercise 6432. Use an oscilloscope to troubleshoot the circuit. Waveform Figure 3-24 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting. SA Table 9.0 verifies the MPU's ability to properly stimulate the DAC via the serial bus.

47. Trigger Generator (U900, U530 on diagram 13), code 64321

This test checks that the Trigger Generator triggers on the selected slope and ignores the unselected slope. Test 47 includes the following steps:

a. Set these conditions:
FISO (Fast In, Slow Out)
PCK = 20 MHz (Phase Clock)
HF Rej and LF Rej (no trigger input signal)
Slope = +

b. Clear these conditions:
Peak-to-peak
Free run
FRT (Fast Ramp Test)

c. Set Trigger Level to -2 divisions, and allow about 55 ms settling time.

d. Initialize the post-trigger/valid-sample counter, and wait for a low on TRIGRST (Trigger Reset).

e. Set Trigger Level to +2 divisions, allow about 55 ms settling time, and check for a high on $\overline{\text{STG}}$ (Synchronous Trigger Gate; no trigger).

f. Set Trigger Level to -2 divisions, allow about 55 ms settling time, and check for a low on $\overline{\text{STG}}$ (Triggered).

g. Repeat steps b-f with minus slope, and reversed Trigger Levels (+2 divisions in steps c and f, -2 divisions in step e).

If this test fails, place the Trigger Board on an extender and run circuit exercise 64321. Use an oscilloscope to troubleshoot the circuit. Waveform Figure 3-25 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger while using this test for troubleshooting.

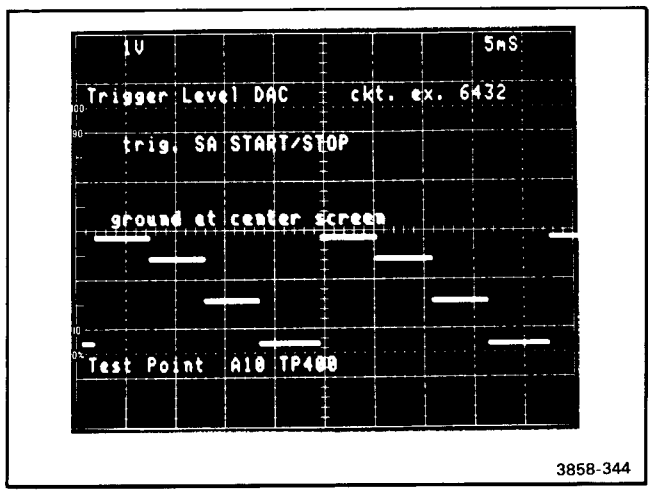

Figure 3-24. Waveform for Trigger Level DAC test.

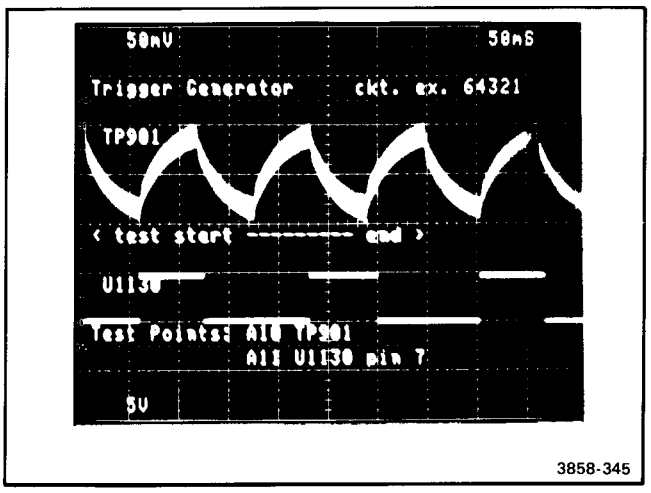

Figure 3-25. Waveform for Trigger Generator test.

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48. Post Trigger Counter (U1700, U1600, U1500, U1400, U1300 on diagram 15), code 65

This test checks that the Post-Trigger counter accepts new data and counts correctly. Test 48 includes the following steps:

a. Set these conditions:
FISO (Fast In, Slow Out)
PCK = 200 kHz (Phase Clock)
PCK Trigger
Freerun

b. Clear these conditions:
ERD (Extended Real-Time Digitizing)
AAGSSE (Acquire Address Generator Single-Step Enable)
AAGINIT (Acquire Address Generator Initialize)

c. Set post-trigger count to $7FFAA.

d. Produce an acquire INIT signal.

e. Delay until just before $\overline{\text{AWCKE}}$ (Acquire Write Clock Enable) goes low, latch U1320 and U1210, shift data out and check $\overline{\text{AWCKE}}$ for proper level.

f. Set post-trigger count to $7FF55 and set Pseudo Real Time (PRT).

g. Produce an acquire INIT signal.

h. Wait until just after $\overline{\text{AWCKE}}$ goes low, and repeat steps d and e.

i. Set Phase Clock (PCK) to 8 MHz and set post-trigger count to $2AAFF.

j. Produce an acquire INIT signal.

k. Wait until just before $\overline{\text{AWCKE}}$ goes low, and repeat steps d and e.

l. Set post-trigger count to $555FF.

m. Produce and acquire INIT signal.

n. Wait until just after $\overline{\text{AWCKE}}$ goes low, and repeat steps d and e.

If this test fails, troubleshoot the Timebase Board using the various following methods: SA Table 6.0 to verifies the MPU's ability to stimulate the Post-Trigger Counter via the serial bus. Circuit exercise 65 provides a stable stimulus for troubleshooting the circuit with an oscilloscope. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test.

49. Trigger Source/Coupling (U710, U200, U900 on diagram 13), code 651

This test checks that the trigger source and coupling circuitry are functional to a limited degree by using the line trigger to stimulate the circuit. Test 49 has the following steps:

a. Set these conditions:
FISO (Fast In, Slow Out)
PCK = 20 MHz (Phase Clock)
Line trigger
DC coupling
Zero division Trigger Level

b. Allow 50 ms settling time, then clear Freerun and Fast Ramp Test (the pin 12 output of U200).

c. Start an Acquire cycle by strobing Initialize (INIT; TP720 diagram 15).

d. Check that an $\overline{\text{STG}}$ (Synchronous Trigger Gate) pulse occurs within 50 ms.

e. Change coupling to AC, then repeat steps b, c, and d.

f. Change coupling, to DC HF Rej, then repeat steps b, c, and d.

g. Change coupling to AC HF Rej, then repeat steps b, c, and d.

h. Change coupling to AC LF Rej, repeat steps b, c, and d; check that no $\overline{\text{STG}}$ occurs.

If this test fails, place the Trigger Board on an extender and run circuit exercise 651. Use an oscilloscope to troubleshoot this circuit. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test. SA Table 9.0 verifies the MPU's ability to stimulate the Source and Coupling hardware.

50. Auto Trigger (U900 on diagram 13), code 652

This test checks that the microprocessor will produce a trigger in the absence of a trigger event. Test 50 consists of the following steps:

a. Set these conditions:
FISO (Fast In, Slow Out)
PCK = 20 MHz (Phase Clock)
High Frequency Reject
Low Frequency Reject

b. Assert a low on Freerun and clear FRT (Fast Ramp Test; when set, FRT selects PCK as trigger for fast ramp test).

c. Start an Acquire cycle by strobing $\overline{\text{INIT}}$ (Initialize; TP720 on diagram 15).

d. Wait for 50 μs, then produce a Freerun trigger pulse.

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e. Check for a low on $\overline{STG}$ (Synchronous Trigger Gate).

If this test fails, place the Trigger Board on an extender and run circuit exercise 652. Use an oscilloscope to troubleshoot this circuit. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test.

51. Fast Ramp (diagram 16), code 6521

This test checks trigger jitter and the accuracy of the fast ramp. Test 51 consists of the following steps:

a. Set these conditions:
FISO (Fast In, Slow Out)
ETD (Equivalent-Time Digitizing)
PCK Trigger (set Fast Ramp Test mode to select Phase Clock Trigger)

b. Start an Acquire cycle by strobing INIT (TP720 on diagram 15).

c. Read the fast ramp value.

d. Repeat steps b and c 64 times.

e. Calculate average fast ramp and jitter values.

f. Set EDR (End Down Ramp) delay.

g. Repeat steps b and c another 64 times.

h. Compute new average fast ramp and jitter values. Subtract average from previous average (step e) and compare resulting difference (gain) with test limits; compare jitter with test limits.

If this test fails run the Fast Ramp Gain/Count test, which is included in the hierarchy of test menus in this section. Refer to the Fast Ramp Adjustment step in Section 4, Checks and Adjustment. Adjust and/or troubleshoot the Fast Ramp circuit as necessary.

52. Ch 1 Position (diagrams 4 and 5), code 653

This test grounds Ch 1 input and sets Ch 1 to 20 mV/ Division. MPU Board Ch 1 position DAC establishes Ch 1 position voltage for center screen. Selects Analog Bus to "read Ch 1 output," then converts and compares the result with test limits.

Next, the test sets Ch 1 position voltage for +5 divisions of deflection, reads the Ch 1 Preamplifier output and compares it with test limits.

Lastly, the test sets Ch 1 position voltage for -5 divisions of deflection, reads the Ch 1 Preamplifier output and compares it with test limits.

If this test fails run circuit exercise 653, and use an oscilloscope to troubleshoot the Channel 1 Preamplifier. Waveform Figure 3-26 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test. SA Table 8.0 verifies that the MPU controls the Preamplifier correctly.

53. Ch 1 Step Attenuator (U910, Q910, Q911, Q920, Q921, Q922 on diagram 4), code 6531

This test sets Ch 1 sensitivity to 20 mV/Division and grounds Ch 1 input. MPU Board Ch 1 position DAC establishes Ch 1 position voltage for -5 divisions. The $\overline{ICS}$ (Input current source) is set on and injects +100 mV to the attenuators. The test checks that the preamplifier output is within test limits.

Next, the test sets the Ch 1 sensitivity to 50 mV/Division and leaves the position voltage at -5 divisions and $\overline{ICS}$ on. The test then verifies that the preamplifier output is within test limits.

Finally, the test sets the Ch 1 sensitivity to 10 mV/Division. $\overline{ICS}$ is still on and the position is set to -5 divisions. The test verifies that the preamplifier output is within test limits.

If this test fails run circuit exercise 6531, and use an oscilloscope to troubleshoot the Channel 1 Step Attenuator. Waveform Figure 3-27 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test. SA Table 8.0 verifies that the MPU controls the preamplifier correctly.

54. Ch 1 Decade Attenuator (A12 Attenuator), code 6532

This test sets Ch 1 sensitivity to 10 mV/Division and grounds Ch 1 input. MPU Board position DAC establishes Ch 1 position voltage for -5 divisions. The $\overline{ICS}$ (input current source) is set on and injects +100 mV to the attenuators. The test checks that the preamplifier output is within test limits.

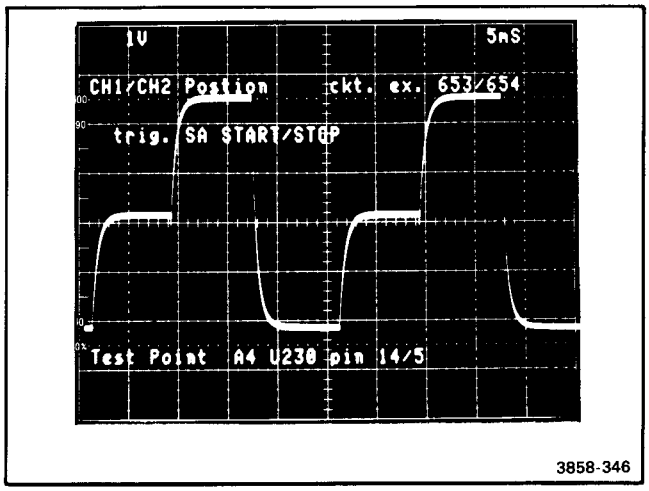

Figure 3-26. Waveform for Ch 1/Ch 2 Position test.

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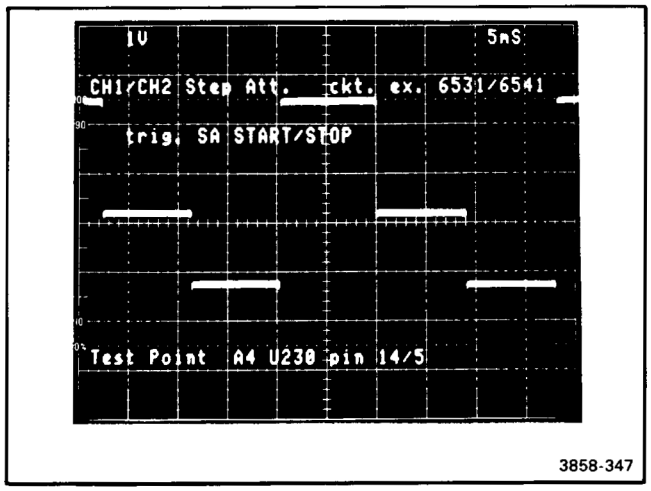

Figure 3-27. Waveform for Ch 1/Ch 2 Step Attenuator test.

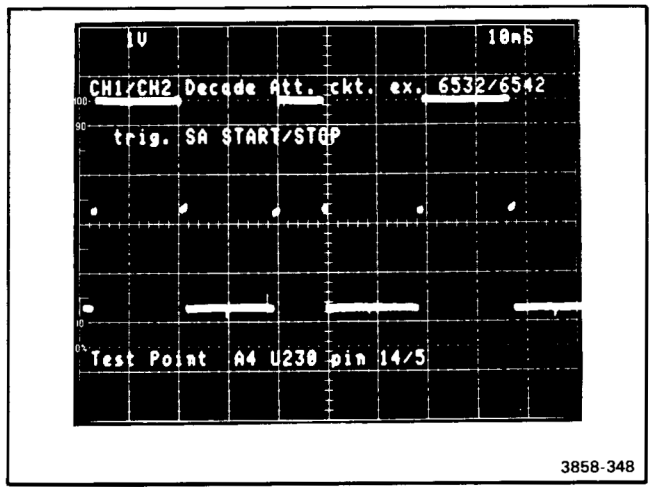

Figure 3-28. Waveform for Ch 1/Ch 2 Decade Attenuator test.

Next, the test sets the Ch 1 sensitivity to 100 mV with the front 10X attenuator, leaves $\overline{ICS}$ on and the position voltage set for -5 divisions. The test then checks that the preamplifier output is within test limits.

Finally, the test sets the Ch 1 sensitivity to 100 mV with the back 10X attenuator, and leaves $\overline{ICS}$ on and the position voltage set for -5 divisions. The test then verifies that the preampifier output is within test limits.

If this test fails, run circuit exercise 6532 and use an oscilloscope to troubleshoot the Channel 1 Decade Attenuator. Waveform Figure 3-28 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test.

55. Ch 1 5 mV/Div (U710 on diagram 5), code 65321

To test the 5 mV/Division sensitivity the test sets the overall sensitivity to 10 mV/Division (20 mV at front panel with the 5 mV compensation circuit activated), and the MPU Board Ch 1 position DAC establishes Ch 1 position voltage for -5 divisions. The test checks that the preamplifier output is within test limits.

Next, the test turns on the $\overline{ICS}$ (input current source) to +100 mV to the attenuators and leaves the sensitivity and position set as mentioned previously. Again, the test checks to verify that the preamplifier output is within test limits.

If this test fails, run circuit exercise 65321 and use an oscilloscope to troubleshoot the Channel 1 Decade Attenuator. Waveform Figure 3-29 is a typical output of this test. The SA Start/Stop line will provide a stable oscilloscope trigger for troubleshooting this test. SA Table 8.0 will verify the MPU control of the preamplifier.

56. Ch 2 Position (diagrams 4 and 5), code 654

This test grounds Ch 2 input and sets Ch 2 sensitivity to 20 mV/Division. The MPU Board Ch 2 position DAC establishes the Ch 2 position voltage for center screen. The test then selects the Analog Bus to "read Ch 2 preamplifier output," converts and compares the result with test limits. Next, the test sets Ch 2 position voltage for +5 divisions of deflection, reads the Ch 2 preamplifier output and compares it with test limits.

Finally, the test sets Ch 2 position voltage for -5 divisions of deflection, reads the Ch 2 preamplifier output and compares it with test limits.

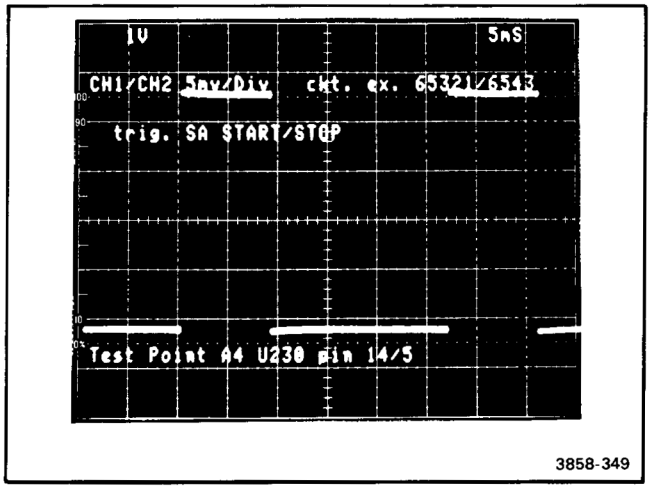

Figure 3-29. Waveform for Ch 1/Ch 2 5 mV/Div test.

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If this test fails run circuit exercise 654, and use an oscilloscope to troubleshoot the Channel 2 Preamp circuitry. Waveform Figure 3-26 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test. SA Table 8.0 verifies MPU control of the preamplifier.

57. Ch 2 Step Attenuator (U930, Q940, Q941, Q950, Q951, and Q952 on diagram 4), code 6541

This test sets Ch 2 sensitivity to 20 mV/Division and grounds Ch 2 input. The MPU Board Ch 2 position DAC establishes Ch 2 position voltage for −5 divisions. The $\overline{ICS}$ (input current source) is set on and injects +100 mV to the attenuators. The test checks that the preamplifier output is within test limits.

Next, the test sets the Ch 2 sensitivity to 50 mV/Division and leaves $\overline{ICS}$ on and the position at −5 divisions. The test then verifies that the preamplifier output is within test limits.

Finally, the test sets the Ch 2 sensitivity to 10 mV/Division. The $\overline{ICS}$ is still on and the position is set to −5 divisions. The test verifies that the preamplifier output is within test limits.

If this test fails run circuit exercise 6541, and use an oscilloscope to troubleshoot the Channel 2 Preamp circuitry. Waveform Figure 3-27 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test.

58. Ch 2 Decade Attenuator (A13 Attenuator), code 6542

First the test sets the Ch 2 sensitivity to 10 mV/Division and grounds the Ch 2 input. The MPU Board Ch 2 position DAC establishes Ch 2 position voltage for −5 divisions. The $\overline{ICS}$ (input current source) is set on and injects +100 mV to the attenuators. The test checks that the preamplifier output is within test limits.

Next, the test sets the Ch 2 sensitivity to 100 mV/Division with the front 10X attenuator, leaves $\overline{ICS}$ on and the position voltage set for −5 divisions. The test then checks that the preamplifier output is within test limits.

Finally, the test sets the Ch 2 sensitivity to 100 mV, this time with the back 10X attenuator, and leaves $\overline{ICS}$ on and the position voltage set for −5 divisions. The test then verifies that the preamplifier output is within test limits.

If this test fails run circuit exercise 6542, and use an oscilloscope to troubleshoot the Channel 2 Decade Attenuator. Waveform Figure 3-28 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test.

59. Ch 2 Invert (U740 on diagram 5), code 65421

This test grounds Ch 2 input, sets Ch 2 to 20 mV/Division, and sets Ch 2 to invert. The MPU Ch 2 position Board DAC establishes the Ch 2 position voltage for +5 divisions. The test then selects the Analog bus to "read Ch 2 preamp output," converts the result and compares it with test limits. Next, the test sets $\overline{ICS}$ (input current source) to inject +100 mV to the attenuators while the rest of the test stays as it was in the previous setup, reads the Ch 2 preamplifier output and compares it with test limits.

Finally, the test changes the sensitivity to 50 mV/Division, reads the Ch 2 preamplifier output and compares it with test limits.

If this test fails run circuit exercise 65421, and use an oscilloscope to troubleshoot the Channel 2 inversion circuitry. Waveform Figure 3-30 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test. SA Table 8.0 will verify MPU control of the Preamplifier

60. Ch 2 5 mV/Div (U740 on diagram 5), code 6543

To test the 5 mV/Division sensitivity, the test sets the overall sensitivity to 10 mV/Division (20 mV/Division at the front panel with the 5 mV compensation circuit activated), and the MPU Board Ch 2 position DAC establishes Ch 2 position voltage for −5 divisions. The test then checks that the preamplifier output is within test limits.

Next, the test turns the $\overline{ICS}$ (input current source) on, injecting 100 mV to the attenuators and leaves the sensitivity and position set as mentioned previously. Again, the test checks to verify that the preamplifier output is within test limits.

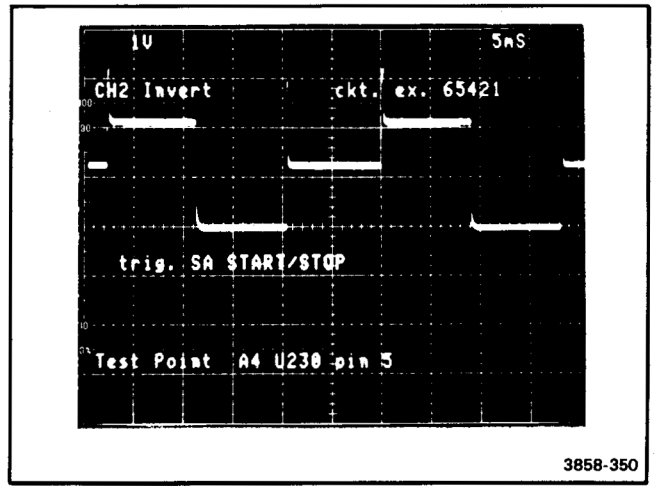

Figure 3-30. Waveform for Ch 2 Invert test.

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If this test fails, run circuit exercise 6543 and use an oscilloscope to troubleshoot the Channel 2 Decade Attenuator. Waveform Figure 3-29 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test. SA Table 8.0 verifies MPU control of the Preamplifier.

61. CCD Signal Driver (Diagram 6), code 65431

    This test checks that the CM1 and CM2 voltages are within test limits.

    This is accomplished by setting the ABus2 to read first CM1 then CM2, converting both and comparing results with test limits.

    If this test fails, place the CCD Board on an extender and run circuit exercise 65431. Use an oscilloscope to troubleshoot the CCD Signal Driver circuitry.

62. CCD Multiplexer (Diagram 7), code 65432

    This test checks the outputs of CCDs U440 and U460 on diagram 6 and the CCD multiplexers on diagram 7. The test first grounds the inputs of Ch 1 and Ch 2, and positions their traces to center screen. Next, the test sets ABus1 to read the output of the CCD multiplexer via U1050 (on diagram 7), and compares that reading with test limits. The output voltage will be the average of the Ch 1 and Ch 2 CCD multiplexer output voltages.

    This process will be repeated three times. The first repeat will be with Ch 1 and Ch 2 set to +4 divisions. The second repeat will be with Ch 1 and Ch 2 set to −4 divisions, and the third repeat will be with Ch 1 set to +4 and Ch 2 set to −4 divisions.

    If this test fails, place the CCD Board on an extender and run circuit exercise 65432. Use an oscilloscope to troubleshoot the CCD Multiplexer circuitry. Waveform Figure 3-31 is a typical output of this test. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test.

63. CCD A/D Converter (Diagram 7), code 654321

    This test grounds the inputs to the attenuators, uses the MPU position DACs to set Ch 1 position to +4 divisions and Ch 2 − 4 divisions. Then U930, the A/D converter, is checked by using Read Memory Data (RMD) latch U300 on the Memory Board to latch the selected CH 1 or CH 2 Acquire Write to waveform memory. The A/D converter (ADC) is tested with Ch 1, Ch 2, and Add data. Each time data is latched that data is compared with test limits.

If this test fails, place the CCD Board on an extender and run circuit exercise 654321. Use an oscilloscope to troubleshoot the CCD A/D Converter. Waveform Figure 3-32 is a typical input to the ADC by this test. The SA Start/Stop line provides a stable oscilloscope trigger for troubleshooting this test.

BACKGROUND INFORMATION ON SIGNATURE ANALYSIS

Signature analysis is a troubleshooting method for isolating faults, usually to the component level in complex logic circuits. Signature analysis testing relies on exercising circuit nodes in a repeatable fashion. The type of exercise is relatively unimportant, as long as the events at the node under test are repeatable. For example, a microprocessor system can easily be made to repeatedly increment (loop) through its address fields, exercising a good portion of the instrument's circuitry. Or, as in most cases, exercise routines are stored in ROM, then retrieved and run to exercise circuitry.

Once a means of exercising the circuitry has been implemented, actual signatures at circuit nodes can be

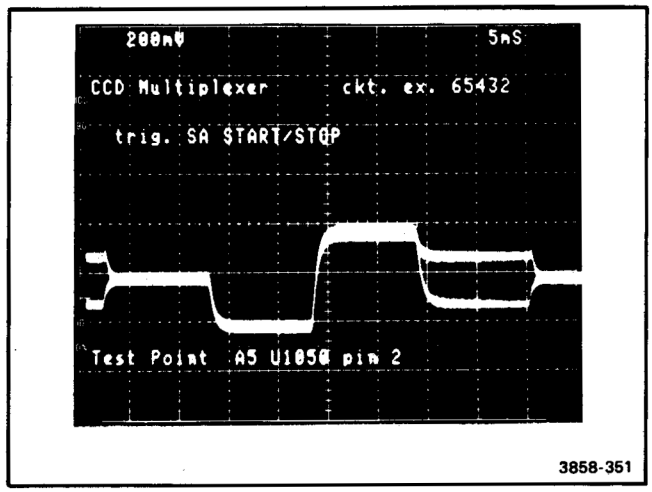

Figure 3-31. Waveform for CCD Multiplexer test.

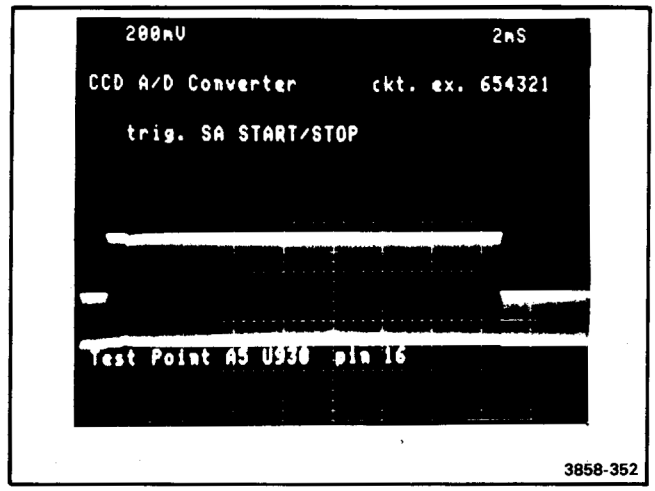

Figure 3-32. Waveform for CCD A/D Converter test.

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taken. Individual signatures are taken over a specific number of system clock cycles (gate time), determined by how the signature analyzer is electrically connected into the system. The actual signature is presented to the user as a four-digit hexadecimal number that is a numerical representation of the complex sequence of events occurring at the node under test. Individual signatures may be composed of the characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, C, F, H, P and U.

The signatures taken at various nodes are compared to "signature sets" containing known good signatures for each particular test node. (All signatures for these procedures were taken with a TEKTRONIX 067-1090-00 Signature Analyzer. Use of other signature analyzers may produce faulty results.) An incorrect signature indicates a problem. Bad signatures can be traced (in terms of data flow) to the point of error in much the same way a bad waveform can be traced to its source in analog circuitry.

However, there is an important difference between analog signal tracing and digital signature tracing. In analog signal tracing, clues to faults are indicated by deviations from the desired waveshape (clipping, oscillations, power supply noise, etc.). In signature tracing, however, subtle differences in signatures from those desired mean nothing. A wrong signature just indicates trouble, not a particular type of trouble.

There are several cases where certain wrong signatures may provide clues, though. A signature of 0000 may be an indication that a test node is shorted to ground (0000 is the "ground" signature). Likewise, a node with a faulty signature the same as the V_{cc} signature may be shorted to the positive supply. When two or more nodes have the same bad signature, they may also be shorted together.

WHAT TO DO IF 7D20 DOES NOT RESPOND TO FRONT-PANEL CONTROLS

Before any of the Self-Test or other diagnostic routines can be used, the microprocessor (MPU) must be running and able to communicate with the front-panel controls. There are two strap-selectable options on the MPU Board to verify this when the 7D20 does not communicate properly with the user.

The two options are Forced-Instruction Freerun and External Bus Exercise. Select the appropriate test option as follows:

- If the host oscilloscope crt and the 7D20 front panel both have abnormal displays, run the Forced-Instruction Freerun test. Use signature analysis (SA Table 1.0) to locate the problem, which will probably be in the kernel.
- If the oscilloscope crt display is operating and the 7D20 does not respond to the front-panel controls, run the External Bus Exercise (regardless of the 7D20 front-panel display). Use signature analysis (SA Table 2.0) to locate the problem, which will probably be in the front-panel input/output circuitry.
- If there is no crt display and only the 7D20 CSW and WFM buttons are lighted, a Self-Test error is indicated. Run the External Bus Exercise (SA Table 2.0) and use an oscilloscope to troubleshoot the Display Interrupt circuitry.

The first option is Forced-Instruction Freerun (FIF). The FIF option will electrically isolate the data bus from the MPU and force the MPU data lines to the machine code (01011111_2 or 5F hex) for a CLRB instruction (clear the B register). The MPU will then freerun, executing just CLRB operations while the program counter runs the address lines successively through the entire addressable range. An oscilloscope or a signature analyzer can be used to check the address lines and address decoders for shorted or open conditions. Also, during part of the cycle the ROMs will put data on the data bus, so an oscilloscope or signature analyzer can be used to detect data bus problems. A signature analyzer can also detect a bad ROM by checking its output signatures. Once all these circuits are functional, the MPU should be fully operational. It may still be unable to talk to the front panel or the GPIB if problems exist on the address and data buses outside the MPU Board.

To perform Forced-Instruction Freerun, proceed as follows:

1. Turn off power in the host oscilloscope.
2. Remove 7D20 from the host oscilloscope.
3. Remove the four screws that fasten the two ECB guide rails to the top rail and the Time Base Board.
4. Remove the two ECB guide rails.
5. Unplug the MPU Board and withdraw it carefully through the top of the 7D20.
6. Remove the following connectors:

   P215, P720, P810, P811, P812, P901, P902, P903, P904, P905, P906 — See Figure 3-33

7. Remove P900 and P907, then install them as shown in Figure 3-33.
8. Check that the connector installation matches that shown in Figure 3-33.
9. Install an Extender Board (670-4334-00) in the 7D20 socket (J310) for the MPU Board.

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10. Replace the front ECB guide rail between the top rail and the Time Base Board. The guide rail will support the Extender Board.

11. Install the MPU Board in the socket on the Extender Board.

12. Use three Flexible Plug-In Extenders (067-0616-00) to connect the 7D20 to the host oscilloscope.

13. Turn on the host oscilloscope.

14. Connect the Signature Analyzer pod as follows:

Start	TP 820
Stop	TP 820
Clock	TP 824
Ground	TP 800

15. Use the Signature Analyzer probe to check the following signatures:

+5 V	0003
Start	0001
Stop	0001
Clock	0000

16. Troubleshoot as necessary, referring to SA Table 1.0. Refer to the Theory of Operation for details of operation.

The second option is External Bus Exercise, which means external to the 7D20 kernel. When the 7D20 is first powered-up (provided that MPU Board is not set to Forced-Instruction Freerun option), the MPU will read the external-bus-exercise strap bit. If the external bus-exercise strap (P510) is removed, the MPU will:

1. Operate in an infinite loop that will shift alternate 1's and 0's through the address and data buses and reads each front-panel port.

2. Exercise the Display Interrupt Generator by alternately strobing the Start Display Cycle and the End Display Cycle lines.

This will help find any external bus faults and also verify that the front-panel ports are placing data on the bus when they are read. When these circuits are working, the instrument can be powered-up normally and all further tests can be called via the front-panel pushbuttons or the GPIB.

To use External Bus Exercise, proceed as follows:

1. Turn off power in the host oscilloscope.

2. Remove 7D20 from the host oscilloscope.

3. Remove the four screws that fasten the two ECB guide rails to the top rail and to the Timebase Board.

4. Remove the two ECB guide rails.

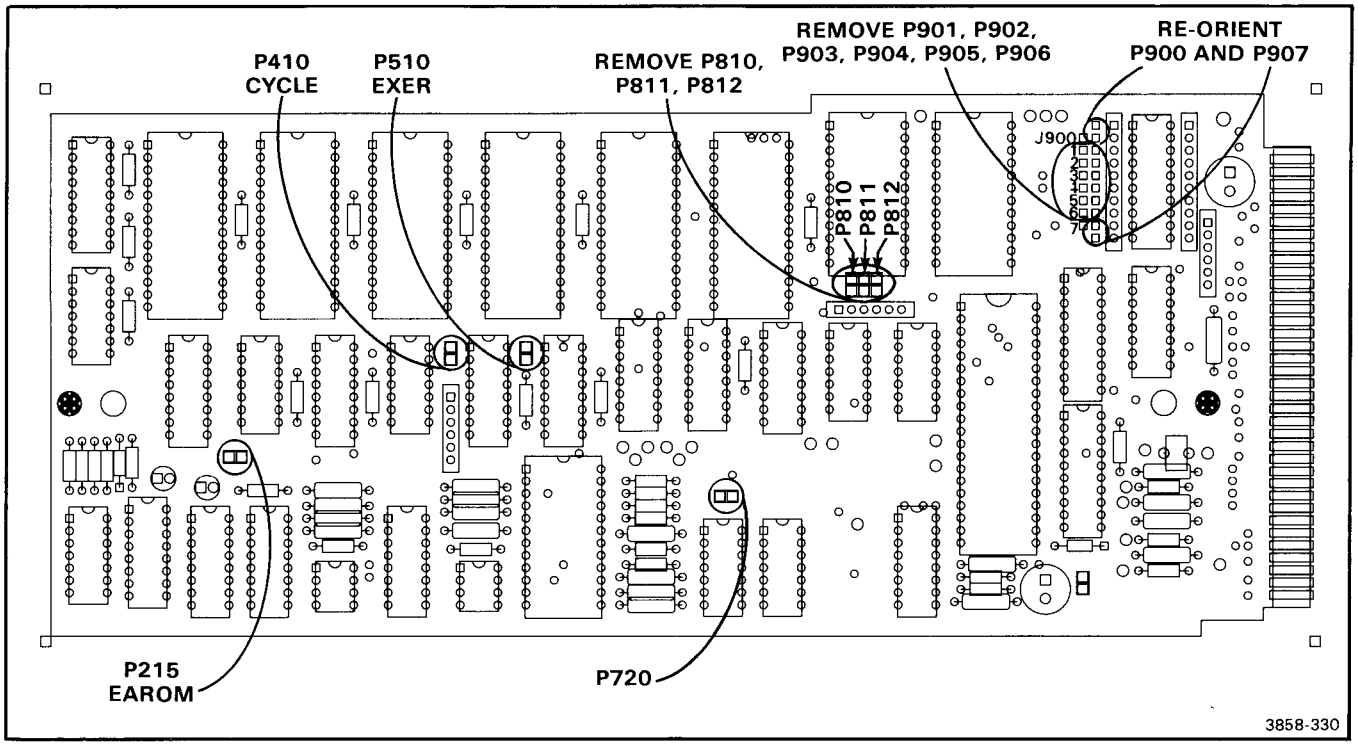

Figure 3-33. Configuration of jumper connectors on MPU Board for Forced Instruction Freerun.

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5. Unplug the MPU Board and withdraw it carefully through the top of the 7D20.

6. Remove connector P510, the external-bus-exercise plug. P510 is located between U510 and U515 on the MPU Board.

7. Install an Extender Board (670-7334-00) in the 7D20 socket (J310) for the MPU Board.

8. Replace the front ECB guide rail between the top rail and the Timebase Board. The guide rail will support the Extender Board.

9. Install the MPU Board in the socket on the Extender Board.

10. Use three Flexible Plug-In Extenders (067-0616-00) to connect the 7D20 to the host oscilloscope.

11. Turn on the host oscilloscope.

12. Connect the Signature analyzer pod as follows:

Start	TP 900
Stop	TP 901
Clock	TP 902
Ground	TP 800

13. Use the Signature Analyzer probe to check the following signatures:

+5 V	FU6C
Start	FU6C
Stop	FU6C
Clock	0000

14. Troubleshoot as necessary, referring to SA Table 2.0. Refer to Theory of Operation for details of operation.

HIERARCHY OF TEST MENUS

This part lists the Test Menu and its submenus. For specific details of the operation of each function, refer to the Operating Instructions section of the 7D20 Operators Manual.

The Test Menu will be displayed when the *f* and MENU TEST buttons are pressed in sequence. (If one of the Test Menu's submenus was in use when the Test Menu was last used, that submenu will be displayed. Item 6 in these submenus will be TEST MENU. To display the Test Menu, press the MEMORY DISPLAY 6 button.) The Test Menu follows:

```
TEST MENU
1 EXECUTE SELFTEST
2 *CALIBRATION*
3 *EXTENDED TEST*
4 *CIRCUIT EXERCISER*
*SERVICE ONLY*
```

To start the Self-Test, press MEMORY DISPLAY 1. If the instrument passes the Self-Test, the words SELFTEST PASS will be displayed in the prompt area of the crt in the host oscilloscope. If the 7D20 fails the Self-Test, the number of the test that fails will be displayed in the prompt area of the host oscilloscope crt, and the following submenu will be presented:

```
SELFTEST FAILURE
1 CONTINUE SELFTEST
2 EXIT SELFTEST
```

Pressing MEMORY DISPLAY 2 while the Test Menu is being displayed will select the Calibration submenu, which is as follows:

```
CALIBRATION
*SERVICE ONLY*
1 FAST RAMP GAIN/COUNT
2 VERTICAL DISPLAY DAC
3 POSITION OFFSET
4 POSITION GAIN
6 TEST MENU
```

Pressing MEMORY DISPLAY 1 will select the Fast Ramp Gain/Count test. Regardless of the result of this test, the 7D20 will present the following display on the crt of the host mainframe:

```
XXX.X          X
GAIN         COUNT
FAST RAMP TEST
*SERVICE ONLY*
6 TEST MENU
```

The Fast Ramp Gain/Count test is performed repetitively, and the Gain and Count results are updated after each test.

When the Calibration submenu is displayed, pressing the MEMORY DISPLAY 2 button will select the Vertical Display DAC test. The test waveform for use in adjusting the Vertical Display DAC and the following submenu will be presented on the crt:

```
VERTICAL DISPLAY DAC
*SERVICE ONLY*
6 TEST MENU
```

When the Test Menu is being displayed and the MEMORY DISPLAY 3 button is pressed, the Extended Test submenu will be displayed as follows:

```
EXTENDED TEST
*SERVICE ONLY*
1 GPIB TEST *REMOVE CABLE*
2 EAROM TEST
3 FRONT PANEL TEST
6 TEST MENU
```


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When the Extended Test submenu is being displayed and the MEMORY DISPLAY 3 button is pressed, the Front-Panel Test will commence. All the LEDs on the front panel will be lighted, except the MENU/TEST LED, which will blink. Pressing each pushbutton will change its state. To terminate the Front-Panel Test, press the MENU/TEST button. The 7D20 will then initialize to its status before the Front-Panel Test, and the Test Menu will not be displayed.

When the Test Menu is being displayed and the MEMORY DISPLAY 4 button is pressed the following information will be displayed:

CIRCUIT EXERCISER
SERVICE ONLY
REFER TO SERVICE MANUAL
PRESS 'ƒ TEST' TO EXIT

The Circuit Exercise function is described under "Troubleshooting Modules" in this section.

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GLOSSARY OF TERMS

AAG—Acquire Address Generator.

AAGINIT—Acquire Address Generator Initialize.

AAGSSE—Acquire Address Generator Single-Step Enable (turns off the AWCK to the AAG).

ABUS1—Analog Bus 1.

ABUS2—Analog Bus 2.

ACQ—ACQuire cycle on Memory Board.

ADC—Analog-to-Digital Converter.

AQRINIT—INITialize new Acquire (signal on Time Base Board).

AWCK—Acquire Write Clock.

AWCKE—AWCK Enable.

CE—Circuit Exercise.

CHBLNK—Character Blank.

CLRB—Clear Register B.

CM—Common Mode.

CRC—Cyclic Redundancy Check (method of checking ROMs).

DAC—Digital-to-Analog Converter.

DAG—Display Address Generator.

DAGSSE—Display Address Generator Single Step Enable (gates off normal clock to display length counter).

DISPBLKX—Display Block X.

DISPBLKY—Display Block Y.

DISPINTR—Display Interrupt.

DLC—Display Length Counter.

DSP—DiSPlay cycle on Memory Board (complement of ACQ).

EAROM—Electrically Alterable ROM (non-volatile memory).

EDR—End Down Ramp (end of time interval measured by fast ramp).

ENDACQ—End of Acquire.

EOA—End of Acquire.

ERD—Extended Real-Time Digitizing.

ETD—Equivalent-Time Digitizing.

FIRQ—Fast Interrupt Request.

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FISO—Fast In, Slow Out (any time/division setting where the CCD's clock is changed from supplying the samples to digitizing them; i.e., 200 μS/division and faster).

FRT—Fast Ramp Test; selects PCK as trigger for that test.

GC—Gain Change control to pre-amplifier IC.

GC820—820 Gain Compensation. Increases horizontal gain to display 80 points per division.

HFR—High Frequency Reject.

ICS—Input Current Source (injects current into the attenuators to produce a 100 mV signal).

INIT—Initialize.

INS—INput Strobe (signal on Time-Base Board indicating data points are currently being sampled for possible storage).

KERNEL—The central control devices, i.e., the MPU, the RAMs, and the ROMs.

LFR—Low-Frequency Reject.

MA—Memory Address.

MD—Memory Data.

MPU—Microprocessor Unit.

P820.1024—820-point display.

PCK—Phase Clock.

PRBS—Pseudo Random Byte Sequence.

PRWS—Processor Read/Write Select (high allows MPU to access waveform memory during ACQ time; low allows access during DSP time).

RMA—Read Memory Address. Also known as the Last Address Latch.

RMD—Read Memory Data. Also known as the Last Data Latch.

SA—Signature Analysis or Signature Analyzer.

SDS—Serial Data Strobe.

SO—Slow Out.

ST—Self Test.

STG—Synchronous Trigger Gate.

TRIGRST—Trigger Reset.

WD—Waveform Data.

WMS—Waveform Memory Select (MPU Select to access waveform memory).

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CHECKS AND ADJUSTMENT

This section provides procedures for checking and adjusting this instrument. These procedures are designed to compare the performance of this instrument with measurement instruments of known accuracy to detect, correlate, or eliminate by adjustment, any variation from the electrical specifications. Also, the functional check procedure verifies that the major functions of the instrument perform properly.

This section has three separate parts: Part I—Functional Check Procedure verifies that the major functions of the instrument perform properly. Part II—Performance Check Procedure verifies that this instrument meets the applicable electrical specifications in Section 1. Part III—Adjustment Procedure provides adjustment instructions to ensure that this instrument is performing at peak capabilities and meets or exceeds the listed electrical specifications at the time of adjustment under the conditions specified. These three parts provide for verification of the qualitative integrity of the product, its performance relating to specifications in Section 1, and the optimization of its performance respectively.

USING THESE PROCEDURES

NOTE

In these procedures, capital letters within the body of the text identify front-panel controls, indicators, connectors and readout information on the 7D20 (e.g., POSITION). Initial capitals identify all the associated test equipment and their controls, connectors and indicators (e.g., Triggering) used in the procedures. Initial capitals also identify adjustments internal to the 7D20 (e.g., Gain).

The Part I—Functional Check procedure should be followed in the sequence in which it is written, starting with step 1, and continuing through to its conclusion. Typically, the Functional Check Procedure is a front-panel check, but in some cases it may be necessary to open the instrument covers to change jumper positions, set switches, or make connections.

The Part II—Performance Check and Part III—Adjustment procedures are divided into subsections by major functional circuits (e.g., A. Acquisition and Display, B. Triggers, etc.). The order in which the subsections and procedures appear is the recommended sequence for a complete performance check or adjustment of the instrument.

The first step in each subsection (A1, B1, etc.) contains reference information and Setup Conditions that must be performed before proceeding.

The Setup Conditions provide equipment connection information and control settings for both this instrument and any associated test equipment. Also, the Setup Conditions are written so that if desired, each subsection (A, B, C, etc.) or step (A2, A3, B2, B3, etc.) can be performed independently.

When used as the first word of an instruction, the terms CHECK, EXAMINE, ADJUST, and INTERACTION are defined as follows:

1. **CHECK**—indicates that the instruction accomplishes an electrical specification check. Each electrical specification check is listed in Table 4-1, Performance Check and Adjustment Summary.
2. **EXAMINE**—usually precedes an ADJUST instruction and indicates that the instruction determines whether adjustment is necessary. If no ADJUST instruction appears in the same step, the EXAMINE instruction concerns measurement limits that do not have a related adjustment. Measurement limits following the word EXAMINE are not to be interpreted as electrical specifications. They are provided as indicators of a properly functioning instrument and to aid in the adjustment process.
3. **ADJUST**—describes which adjustment to make and the desired result. It is recommended that adjustments not be made if a previous EXAMINE instruction indicates that no adjustment is necessary.
4. **INTERACTION**—indicates that the adjustment described in the preceding instruction interacts with other circuits. The nature of the interaction is described and reference is made to the step(s) affected.

PERFORMANCE CHECK AND ADJUSTMENT SUMMARY

Table 4-1 lists the electrical specifications that are checked in Part II, and the related adjustment (when applicable) in Part III. Table 4-1 is intended to provide a convenient means of locating the steps that check the electrical specifications of the product.

TEST EQUIPMENT

The test equipment listed in Table 4-2 is required for completing Part II—Performance Check Procedure and Part III—Adjustment procedure.

If only a Performance Check is desired, not all equipment is necessary and is indicated by footnote 1. The remaining test equipment is common to both Parts II and III.

The Adjustment procedure is based on the first item of equipment given in Table 4-2. If other equipment is substituted, control settings or setups may need to be altered. If the exact item or equipment given as an

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example is not available, refer to the Minimum Specifications column to determine if other equipment may be substituted. Then check the Purpose column. If you determine that your measurement requirements will not be affected, the item and corresponding step(s) can be deleted.

TEST EQUIPMENT ALTERNATIVES

Completing both Part II and III may not always be necessary or desirable. You may desire to only check selected characteristics, and thereby substantially reduce the amount of test equipment required.

TABLE 4-1
Performance Check and Adjustment Summary

Characteristic	Performance Requirement	Part II Performance Check Procedure Title	Part III Adjustment Procedure Title
VERTICAL			
Deflection Factor (Volts/Div)		A3. CHECK—CH 1 and CH 2 Vertical Gain.	Not applicable.
Calibration Range	5 mV/Div to 5 V/Div in 1,2,5 sequence.		
Gain Ratio Accuracy	Within 2% with AQR GAIN adjusted 10 mV/Div.		
Uncalibrated (Variable)	Continuously variable; VARIABLE extends deflection factor to at least 12.5 V/Div.		
Vertical Linearity (1 kHz square wave)	0.12 Div or less expansion or compression of a center screen 2 Div signal positioned anywhere within the ±4 division graticule area.	A4. Check Vertical Linearity and Acquisition Window.	A6. Adjust Channel 1 Centering, Balance, Gain, and Reference Voltages. A7. Adjust Channel 2 Centering, Balance, Gain, and Reference Voltages.
Invert Deflection Factor Ratio	1:1 within 1%.	A3. Check—CH 1 and CH 2 Vertical Gain.	Not applicable.
Common Mode Rejection Ratio (using ADD, INVERT)	At least 10:1, DC to 50 MHz.	A5. Check Signal Isolation, and Common Mode Rejection Ratio.	Not applicable.
Bandwidth (1 μs to 50 ns/div)	DC to 70 MHz.	A6. Check Bandwidth.	Not applicable.
AC Coupled Low-Frequency Bandwidth	10 Hz or less.		
Overdrive Recovery	1 ms or less, to recover within 1 div. with the VOLTS/DIV set at 5 mV and an overdrive signal of ±1.5 V.	Customer verification normally not required. Satisfactory operation is substantiated at the factory.	Not applicable.
Maximum Input Voltage DC Coupled (DC+Peak AC) AC Coupled (DC+Peak AC)	250 V, 1 kHz or less.	Specification applicable under fault conditions; therefore this does not have a procedural check.	Not applicable.

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TABLE 4-1 (CONT)
Performance Check and Adjustment Summary

Characteristic	Performance Requirement	Part II Performance Check Procedure Title	Part III Adjustment Procedure Title
VERTICAL (Cont)			
Input R and C		Verified at the factory.	Not applicable.
Resistance	1 MΩ ±1%.		
Capacitance	Approximately 20 pF.		
Signal Isolation between Channels (8 Div Ref)	100:1 up to 20 MHz.	A5. Check Signal Isolation and Common Mode Rejection Ratio.	Not applicable.
Noise (Full scale = 10.24 divisions)	Mean value of 50 measurements taken at 0.02 Div increments.	Verified at the factory.	Not applicable.
10 mV/Div to 5 V/Div	55 dB Full Scale/RMS Noise.		
5 mV/Div	52 dB Full Scale/RMS Noise.		
Phase Match Between Channels	2 Degrees at 10 MHz.	A5. Check Signal Isolation and Common Mode Rejection Ratio.	Not applicable.

TRIGGER

Sensitivity	Triggering Frequency Range	Minimum Vertical Signal Required			A7. Check Triggering.	B. Trigger.
		Internal	Ext.	Ext ÷10		
AC Coupled	30 Hz to 30 MHz	0.4 Div	60 mV	0.6 V		
	30 MHz to 70 MHz	1.0 Div	150 mV	1.5 V		
AC LF REJ	50 kHz to 30 MHz	0.4 Div	60 mV	0.6 V		
	30 MHz to 70 MHz	1.0 Div	150 mV	1.5 V		
AC HF REJ	30 Hz to 30 kHz	0.4 Div	60 mV	0.6 V		
DC HF REJ	DC to 30 kHz	0.4 Div	60 mV	0.6 V		
DC	DC to 30 MHz	0.4 Div	60 mV	0.6 V		
	30 MHz to 70 MHz	1.0 Div	150 mV	1.5 V		
Max Signal		±6 Div	±1.0 V	±10 V		
P-P	30 Hz to 200 Hz	2.0 Div	300 mV	3.0 V		
	200 Hz to 30 MHz	0.6 Div	90 mV	0.9 V		
	30 MHz to 70 MHz	1.2 Div	200 mV	2.0 V		

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TABLE 4-1 (CONT)
Performance Check and Adjustment Summary

Characteristic	Performance Requirement			Part II Performance Check Procedure Title	Part III Adjustment Procedure Title
TRIGGER (Cont)					
Programmed Trigger Levels	Internal	Ext.	Ext ÷10	Verified at the factory.	Not applicable.
Resolution	0.05 Div	7.8 mV	78 mV		
Gain Accuracy	±5%	±8%	±12%		
Offset	±0.25 Div	±50 mV	±500 mV		
Range (Nominal)	±6.4 Div	±1.0 V ±10 V			
Position				Customer verification normally not necessary. Satisfactory operation is substantiated by other tests in the procedures.	Not applicable.
Normal	-1500 to +10 Div (+0, -1 sample interval).				
ROLL ENV, ROLL AVE	0 to 10 Div (+0, -1 sample interval).				
Ext Trigger Input				Customer verification normally not required. Input resistance and capacitance can be determined with appropriate testing bridge, if necessary.	Not applicable.
Resistance	1 MΩ, ±10%.				
Capacitance	Approximately 20 pF.				
Maximum Input Voltage (DC+Peak AC)	250 V.			Specification applicable under fault conditions; therefore this does not have a procedural check.	Not applicable.
DIGITIZER					
Acquisition Window	Nominally ±5 Div from center graticule line.			A4. Check Vertical Linearity and Acquisition Window.	Not applicable.
Resolution				Inherent to instrument architecture and does not require routine verification.	Not applicable.
Vertical	Nominally 0.04 Div.				
Horizontal	TIME/DIV	Points/Waveform	Resolution		
	EXT, 20s—500μs	1024	0.01 Div.		
	200μs—2μs	820	0.0125 Div.		
	1μs—50ns	1024	0.01 Div.		
Stored Timing Accuracy				A8. Check timing.	Not applicable.
1 Cursor	±0.1% of reading +0, -1 sample interval ±300 ps.				
2 Cursors	±0.1% of reading ±600 ps.				

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TABLE 4-1 (CONT)
Performance Check and Adjustment Summary

Characteristic	Performance Requirement	Part II Performance Check Procedure Title	Part III Adjustment Procedure Title
DIGITIZER (Cont)			
Digitizer Maximum Sample Rate	40 M Samples/sec.		
Digitizing Modes		A8. Check Timing.	Not applicable.
Equivalent Time	1 μs/div through 50 ns/div.		
Extended Real-Time	200 μs/div to 2 μs/div.		
Real-Time	50 ms/div to 500 μs/div.		
Roll	20 s/div to 100 ms/div and EXTernal CLOCK.*		

***EXTernal CLOCK does not normally require customer verification. Satisfactory operation can be substantiated by performing the Part I—Functional Check Procedure in this section.**

TABLE 4-2
Test Equipment

Description	Minimum Specification	Purpose	Example of Applicable Test Equipment
1. Oscilloscope Mainframe	Compatible with Tektronix 7000 series plug-ins.	Used throughout procedure.	a. TEKTRONIX 7603 Oscilloscope. b. Refer to Tektronix catalog for compatible oscilloscope.
2. Test Oscilloscope[1]	Bandwidth dc to 100 MHz; minimum deflection factor, 5 mV/div; accuracy within 3%. Dual-channel both with an inverting input and added mode.	Used to adjust CCD response.	a. TEKTRONIX 7603 Oscilloscope with 7A26 Dual Trace Amplifier, 7B80 Time Base, and two P6008 Probes. b. Refer to Tektronix catalog for comparible test oscilloscope.
3. Digital Multimeter[1]	0.05% dc voltage accuracy, 0-20 V dc range.	Used to adjust attenuator balance, CCD response and triggers.	a. TEKTRONIX DM 501A DM501A Option 02 Digital Multimeter with power module.
4. Calibration Generator	Square-wave output, 10 Hz to 1 MHz; output amplitude range, 20 mV to 20 V in a 1-2-5 sequence; amplitude accuracy, within 0.25%.	Provides calibrated signal for setting gain.	a. TEKTRONIX PG 506 Calibration Generator, with power module.
5. Time Mark Generator	Markers output; 5 s to 50 ns in 1-2-5 sequence; accuracy within 0.01%.	Used to check Timing accuracy.	a. TEKTRONIX TG 501 Time Mark Generator, with power module.
6. Function Generator	Sinewave output frequency, 20 Hz to 11 MHz; accuracy within 10%; variable output from 0 V to 20 V.	Provides low frequency sine wave signal for bandwidth and triggering checks and adjustments.	a. TEKTRONIX FG 502 Function Generator, with power module

[1]**Used for Adjustment only; not used for Performance Check.**

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TABLE 4-2 (CONT)
Test Equipment

Description	Minimum Specification	Purpose	Example of Applicable Test Equipment
7. Leveled Sine Wave Generator	Leveled, Variable Output, 250 kHz to 100 MHz; 0 to 1 V output into 1 megohm.	Used for bandwidth and CMRR checks.	a. TEKTRONIX SG 503 Leveled Sine Wave Generator with Power Module
8. Dual BNC Connector	Two lengths of RG58 are matched to less than 0.1 inch.	Used for CMRR check.	a. Tektronix part 067-0525-02
9. Cable	Connectors tip plugs on one end, and male bnc on other end.	Used to adjust CCD response.	a. Tektronix part 175-1178-00.
10. Flexible Plug-In Extender (three required)[1]	For use with 7000-series plug-in units.	Used throughout adjustment procedure.	a. Tektronix part 067-0616-00.
11. Coaxial Cable (two of each required)	50 Ω; 42 inch, bnc end connectors.	Used throughout Performance Check and Adjustment procedures to provide signal connection.	a. Tektronix part 012-0057-01.
12. 50-Ohm Terminator (two required)	Impedance, 50 ohms; accuracy, within 2%, connectors, bnc.	Output termination for signal generators.	a. Tektronix part 011-0049-01.
13. 2X Attenuator	Impedance, 50 ohms; accuracy, within 2%, connectors, bnc.	Used to check triggering.	a. Tektronix part 011-0069-02.
14. 10X Attenuator	Impedance, 50 ohms; accuracy, within 2%, connectors, bnc.	Used to check triggering.	a. Tektronix part 011-0059-02.
15. Screwdriver	Three-inch shaft, 3/32 inch bit.	Used to set front panel adjustments.	a. Xcelite R3323.
16. Alignment Tool[1]	Low capacitance adjustment tool.	Used throughout adjustment procedure.	a. Tektronix part 003-0675-00.

[1] **Used for Adjustment only; not used for Performance Check.**

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PART I—FUNCTIONAL CHECK PROCEDURE

The Part I—Functional Check Procedure verifies that the major functions of the instrument perform as described in the Operators Manual. The procedure exercises the main user interfaces of the device to verify their operation and checks the main internal features.

This procedure is not intended to fully check instrument specifications, but may serve as a brief instrument check of functional specifications, or nonquantified characteristics.

7D20 FUNCTIONAL CHECK

Performing this functional check procedure will ensure that your 7D20 is functionally operational but it will not determine if the instrument is properly adjusted for performance. Built-in self diagnostics greatly simplifies the functional check of the 7D20. You will, however, need a host mainframe and (if you wish to completely check the GPIB transfer capability) a controller such as the TEKTRONIX 4051 Desktop Computer. The following steps will take you through the Functional Check of the 7D20.

1. SELF TEST

a. Install the 7D20 into a Tektronix 7000-series host mainframe, and turn the power on. The Self-Test will run automatically at power up.

b. When the Self Test is successfully completed, the message "SELFTEST PASS" will appear in the display. If the message "FAIL n" (where n is the circuit number that failed) appears, a fault has been detected in the 7D20 circuitry; refer to Section 3, Maintenance, for troubleshooting information.

2. EXTENDED SELF TEST

a. Select the "TEST MENU" by pressing f, TEST.

b. Select the EXTENDED TEST from the TEST MENU by pressing MEMORY DISPLAY key 3. The "EXTENDED TEST" menu will be displayed. Be sure the GPIB cable is not connected, then select the "GPIB TEST" from the EXTENDED TEST MENU by pressing MEMORY DISPLAY key 1. At the conclusion of this test, the message "GPIB PASSED" will appear in the display. If the message "GPIB FAILED" appears, a fault has been detected; refer to Section 3, Maintenance, for troubleshooting information.

   This test checks all functions of the GPIB except for the Output Drivers. A method for checking the GPIB Output Drivers appears later in this check procedure.

c. Select the EAROM TEST from the EXTENDED TEST MENU by pressing MEMORY DISPLAY key 2 (item 2 on the menu). The message "EAROM PASSED" will appear in the display at the successful conclusion of this test. If the message "EAROM FAILED" appears, a fault has been detected; refer to Section 3, Maintenance, for troubleshooting information.

d. Select the FRONT PANEL TEST from the EXTENDED TEST MENU by pressing MEMORY DISPLAY key 3 (item 3 on the menu). This test turns on all the front panel leds and blinks the MENU led.

   Verify the leds and keys are operating properly by pressing each key and noting that the corresponding led extinguishes. The TRIGGERING ⇨TRIG POS key affects the TRIG'D led, and the ⇦TRIG POS key affects the REMOTE ONLY led.

   You can exit from the test by pressing the blinking MENU key.

3. CHECK 7D20 INPUT CONNECTORS

a. Connect the 4 volt, 1-kHz calibrator signal from the host mainframe to the CH 1 input connector of the 7D20. Select the BOTH AQR MODE.

b. Observe that the calibrator signal is displayed. Adjust the CH 1 POSITION control and observe that the waveform can be vertically repositioned.

c. Turn the VARIABLE VOLTS/DIV control out of its calibrated (detent) position. Observe that the CH 1 VOLTS/DIV readout includes a ">" sign indicating that the vertical attenuation is greater than the displayed setting. Return the control to its calibrated (detent) position and note that the ">" sign is no longer displayed.

d. Connect the calibrator signal in step a to the CH 2 input connector and repeat steps b and c for channel 2.

e. Connect the calibrator signal in step a to the EXT CLOCK connector on the front panel of the 7D20. Turn the TIME/DIV control fully counterclockwise to select EXT CLocK mode. EXT⇧ or EXT⇩ will appear in the display. Observe that the display rolls across the crt. Disconnect the signal and observe that the display appears to hold.

f. Connect the calibrator signal in step a to the EXT TRIG connector. Change the TIME/DIV setting to 100 μs/div and observe that the TRIG'D indicator lights.

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Disconnect the signal and note that the TRIG'D indicator extinguishes.

4. CHECK GPIB OUTPUT DRIVERS

a. Turn the power off and connect the 7D20 GPIB to a TEKTRONIX 4051 Desktop Computer. Turn the power on.

b. Connect the mainframe 4 V, 1-kHz calibrator signal to the CH 1 input connector.

c. Press the ID key to change the numeric MEMORY DISPLAY keypad mode from "waveform selection" to "function selection". (Repeatedly pressing the ID key will alternate between Waveform Selection and Function Selection.)

d. Press MEMORY DISPLAY key 6 to select GPIB address 1. The message "ADDR= n ?" (where n is the current GPIB address) will be displayed, and both the "?" and key 6 will blink. (Repeatedly pressing key 6 will increment address numbers 0 through 30.)

e. Press MEMORY DISPLAY key 5 to select GPIB Terminator EOI. The message "TERM= term ?" (where term is the current GPIB terminator) will be displayed, and both the "?" and key 5 will blink. (Repeatedly pressing key 5 will alternate the terminator between EOI and LF/EOI.)

f. Press MEMORY DISPLAY key 4 to select GPIB Mode Talk/Listen. The message "MODE= mode ?" (where mode is the current GPIB mode) will be displayed, and both the "?" and key 4 will blink. (Repeatedly pressing key 4 will sequence the Mode selection through Off Bus (OFF), Talk only (T), Listen only (L), and Talk/Listen (T/L).)

g. After making the above selections turn off the ID selection process by pressing the lit ID key. The changes initiated above actually take place when the ID key is pressed.

h. Type the following program into the 4051 computer:

```
10 INIT
20 ON SRQ THEN 200
30 PRINT @1:"INIT"
40 A2=0
50 PRINT @1:"DATA ENCDG:ASCII;TRIGGER HOLDN:ON"
60 IF A2=0 THEN 60
70 DIM A$(7000)
80 PRINT @1:"CURVE?"
90 INPUT @1:A$
100 PRINT @1:"DATA MEMORY:2;DISP 2:ON"
110 PRINT @1:A$
120 END
200 POLL A1,A2;1
210 RETURN
```

i. Run the program. When finished, the calibrator signal will be in both memory 1 and memory 2. If the program will not run, refer to Section 3, Maintenance, for troubleshooting information.

This concludes the Functional Check Procedure.

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PART II—PERFORMANCE CHECK PROCEDURE

The Part II—Performance Check Procedure verifies electrical specifications without removing instrument covers or changing internal adjustments. The steps in this procedure check the Performance Requirement statements in Table 4-1, Performance Check and Adjustment Summary. Performance Check Procedure step numbers listed in Table 4-1 reference each Performance Requirement to a specific check in this procedure, and cross-reference to the proper adjustment step in Part III—Adjustment Procedure.

INDEX TO PART II— PERFORMANCE CHECK PROCEDURE

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2. Initialization Procedure 4-10
3. Check CH 1 and CH 2 Vertical Gain 4-11
4. Check Vertical Linearity and Acquisition Window 4-13
5. Check Signal Isolation, Common Mode Rejection Ratio 4-14
6. Check Bandwidth 4-15
7. Check Triggering 4-16
8. Check Timing 4-17

PERFORMANCE CHECK INITIAL SETUP PROCEDURE

NOTE

The specifications are valid at an ambient temperature of 0° to +40° C when used in a 7400/7600 Series mainframe without a fan, or at an ambient temperature of 0° to +45° C when used in any other 7000 Series mainframe, unless otherwise stated.

CAUTION

To avoid instrument damage, it is recommended that the POWER switch be turned off before removing or replacing the 7D20.

1. Install the 7D20 in the Oscilloscope Mainframe.
2. Connect the Oscilloscope Mainframe to a suitable power source and turn power on. Allow at least 20 minutes warmup before beginning the procedure.

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A. SIGNAL ACQUISITION AND DISPLAY

Equipment Required (Numbers correspond to those listed in Table 4-2, Test Equipment).

1. Oscilloscope Mainframe
4. Calibration Generator
5. Time Mark Generator
6. Function Generator
7. Leveled Sine-Wave Generator
8. Dual BNC Connector
9. Cable
11. Coaxial Cable (two required)
12. 50-ohm Terminator
13. 2X Attenuator
14. 10X Attenuator
15. Screwdriver (Xcelite R3323)

A1. PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and the change Information at the rear of the manual for any modifications which may affect this procedure.

c. Set the Oscilloscope Mainframe controls:
Power ..... On
Vertical Mode ..... Left
Intensity ..... Visible Display
Focus ..... Well defined display

d. Set the 7D20 controls:
HORIZ POSITION .. Fully clockwise (In detent)
CH 1 VARIABLE ..... CAL (In detent)
CH 1 POSITION ..... Midrange
CH 2 VARIABLE ..... CAL (In detent)
CH 2 POSITION ..... Midrange

e. Press MENU (pushbutton will light). If MASTER MENU is not displayed, press MEMORY DISPLAY pushbutton number 6. From the MASTER MENU list displayed on the oscilloscope mainframe crt, select DISPLAY ADJ PATTERN by pressing MEMORY DISPLAY pushbutton number 3.

f. While observing the adjustment pattern displayed on the oscilloscope mainframe crt, set VERT GAIN, VERT CTR, HORIZ GAIN and HORIZ CTR adjustments to place the corner markers of the displayed adjustment pattern on the center 6 × 8 divisions of graticule, as shown in Figure 4-1.

g. Set VECT LIN adjustment for minimum trace separation of the diagonal lines on the displayed adjustment pattern as shown in Figure 4-1.

h. Press MEMORY DISPLAY pushbutton number 6 to return to MASTER MENU. Press MENU pushbutton to turn off MASTER MENU display.

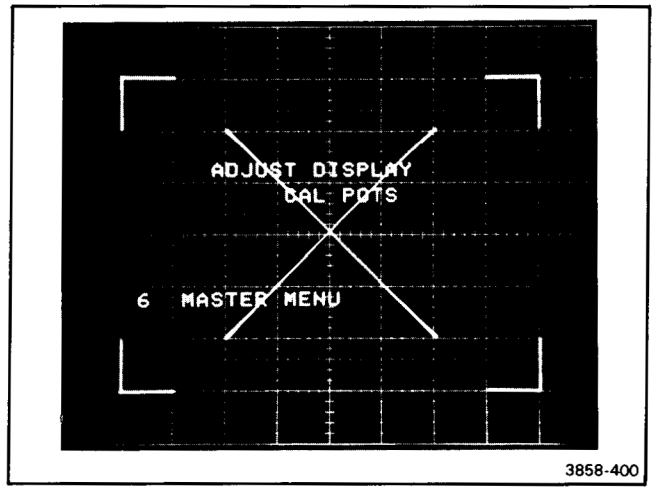

Figure 4-1. Display adjust pattern.

A2. INITIALIZATION PROCEDURE

a. Press MENU (pushbutton will light).

b. If MASTER MENU is not displayed press MEMORY DISPLAY pushbutton number 6.

c. From displayed MASTER MENU list select UTILITIES by pressing MEMORY DISPLAY pushbutton number 4.

d. From displayed UTILITIES list select INIT FRONT PANEL by pressing MEMORY DISPLAY pushbutton number 5.

e. To return to MASTER MENU, press MEMORY DISPLAY pushbutton number 6. To turn off MASTER MENU display, press MENU.

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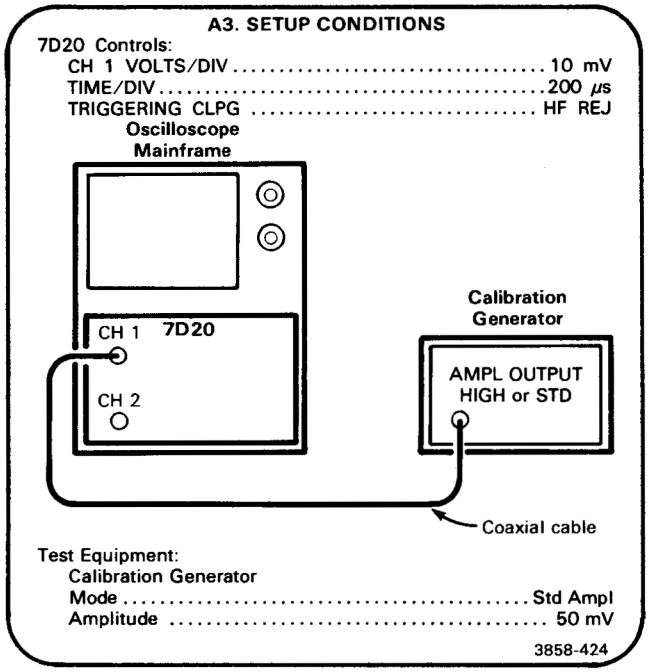
A3. CHECK CH 1 AND CH 2 VERTICAL GAIN

NOTE

First perform steps A1 and A2, then proceed.



NOTE

It is essential that the oscilloscope mainframe sensitivity be properly adjusted prior to performing this step. Refer to the oscilloscope mainframe instruction manual for adjustment procedure.

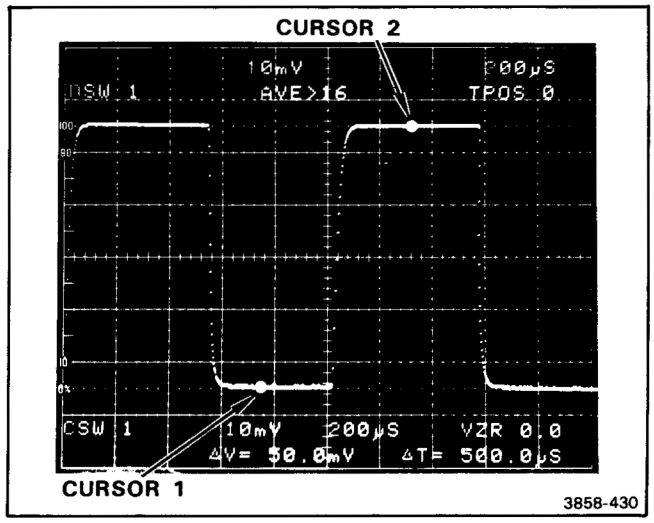


Figure 4-2. CURSORS 1 and 2 used to measure p-p voltage.

a. Set CURSORS to ΔON and position CURSORS 1 and 2 as shown in Figure 4-2.

b. Set CH 1 AQR GAIN for CURSORS readout of ΔV=50mV.

c. **CHECK**—Using Table 4-3, check vertical deflection, error, and ΔV readout, for each position of the CH 1 VOLTS/DIV switch.

d. Set CH 1 VOLTS/DIV to 5V and calibration generator for a 20 volt output.

e. Rotate CH 1 VARIABLE [VOLTS/DIV] control fully counterclockwise.

TABLE 4-3
Vertical Deflection Accuracy

Volts/Div Switch Setting	Calibration Generator Output	Vertical Deflection in Divisions	Maximum Error in Divisions	ΔV Readout
5mV	20 mV	4	0.1	19.6 to 20.4mV
10mV	50 mV	5	Gain Adjusted to 0.0	49.6 to 50.4mV
20mV	0.1 V	5	0.1	98.4 to 101.6mV
50mV	0.2 V	4	0.1	196 to 204mV
100mV	0.5 V	5	0.1	492 to 508mV
200mV	1.0 V	5	0.1	0.984 to 1.016V
500mV	2.0 V	4	0.1	1.96 to 2.04V
1V	5.0 V	5	0.1	4.92 to 5.08V
2V	10 V	5	0.1	0.984 to 1.016V
5V	20 V	4	0.1	19.6 to 20.4V

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f. **CHECK**—Displayed waveform is no more than 1.6 divisions in amplitude, ΔV readout is less than 8.0V and that the ">" symbol is displayed.

g. Connect the calibration generator output to CH 2 input and set CH 2 VOLTS/DIV to 10 mV.

h. Set AQR MODE to CH 2 and Calibration Generator Amplitude to 50 millivolts.

i. Set CH 2 AQR GAIN for CURSORS readout of ΔV=50mV.

j. **CHECK**—Using Table 4-3, check vertical deflection, error, and ΔV readout, for each position of the CH 2 VOLTS/DIV switch.

k. Set CH 2 VOLTS/DIV to 5V and calibration generator for a 20 volt output.

l. Rotate CH 2 VARIABLE (VOLTS/DIV) control fully counterclockwise.

m. **CHECK**—Displayed waveform is no more than 1.6 divisions in amplitude, ΔV readout is less than 8.0V and that the ">" symbol is displayed.

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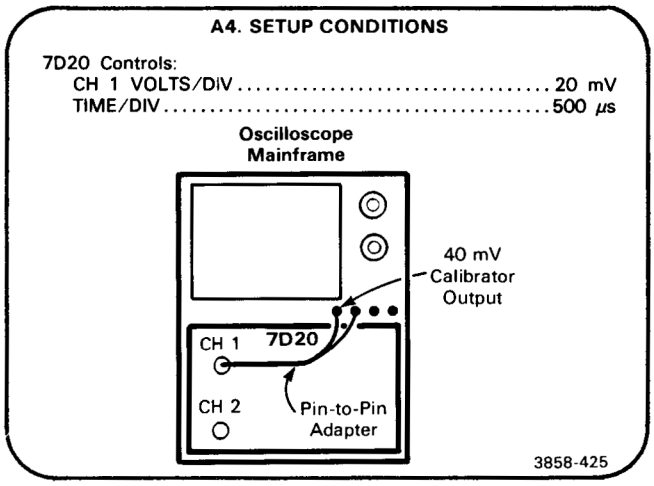
A4. CHECK VERTICAL LINEARITY AND ACQUISITION WINDOW

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

a. Perform step A2 Initialization Procedure, then proceed.



b. Set CURSORS to ΔON by pressing *f* pushbutton, then press CURSORS ΔON (pushbutton will light).

c. Set CURSORS 1 and 2 as shown in Figure 4-3.

d. **CHECK**—With the CH 1 POSITION control, move two division display over entire graticule area and observe that CURSORS readout does not vary more than 2.4mV (use AVE for each observation).

e. Connect calibrator output to CH 2 input connector.

f. Set AQR MODE to CH 2.

g. Set CH 2 VOLTS/DIV to 20mV.

h. **CHECK**—With CH 2 POSITION control, move two division display over entire graticule area and observe that CURSORS readout does not vary more than 2.4mV (use AVE for each observation).

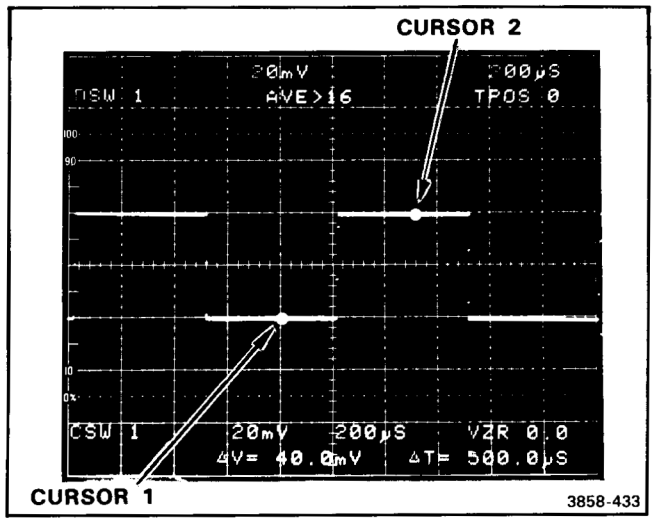


Figure 4-3. Check Vertical Linearity.

i. Set CH 1 and CH 2 input coupling to GND.

j. Rotate CH 2 POSITION control fully clockwise.

k. **CHECK**—For VZR reading of at least 5.0.

l. Rotate CH 2 POSITION control fully counterclockwise.

m. **CHECK**—For VZR reading of at least -5.0.

n. Set AQR MODE to CH 1.

o. Rotate CH 1 POSITION control fully clockwise.

p. **CHECK**—For VZR reading of at least 5.0.

q. Rotate CH 1 POSITION control fully counterclockwise.

r. **CHECK**—For VZR reading of at least -5.0.

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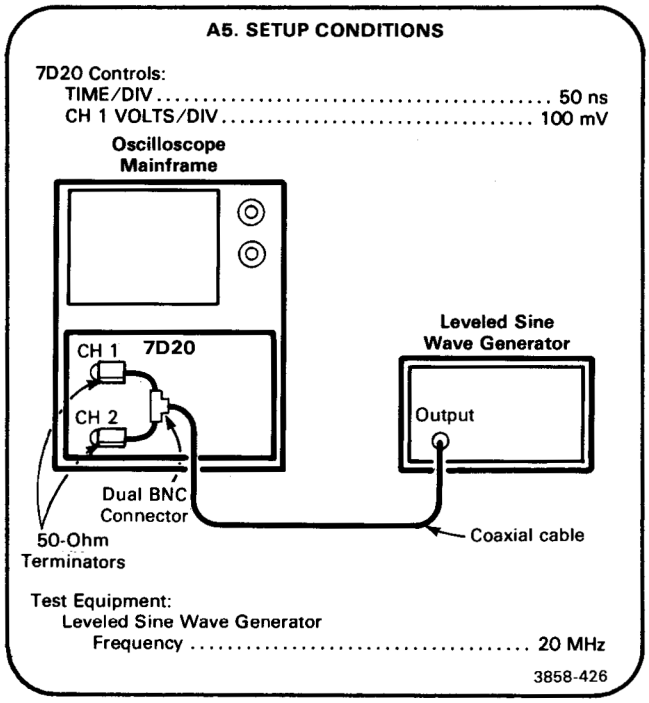
A5. CHECK SIGNAL ISOLATION, AND COMMON MODE REJECTION RATIO

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

a. Perform Step A2, Initialization procedure.



b. Set leveled sine-wave generator for eight divisions of 20 megahertz signal centered on the oscilloscope mainframe crt.

c. Set AQR MODE to BOTH and CH 2 VOLTS/DIV to 100mV.

d. Disconnect signal input to CH 2.

e. **CHECK**—CH 2 display for less than 0.08 division signal.

f. Connect signal input to CH 2 and disconnect signal input to CH 1. Set TRIGGERING SOURCE to CH 2.

g. **CHECK**—CH 1 display for less than 0.08 division signal.

h. Connect signal input to CH 1 and set leveled sine-wave generator for eight divisions of 25 megahertz signal centered on oscilloscope mainframe crt.

i. Set CH 2 INV switch on.

j. Set AQR MODE to ADD.

k. **CHECK**—Displayed signal is less than 0.8 divisions.

l. Set AQR MODE to BOTH.

m. Set CH 2 INV pushbutton to off.

n. Set leveled sine-wave generator to 10 megahertz, and Amplitude control for an eight-division display.

o. Press CURSORS WFM VS pushbutton.

p. Press MEMORY DISPLAY pushbutton number 2.

q. **CHECK**—Crt lissajous display for a separation of 0.28 division or less, See Figure 4-4, (indicates 2 degrees or less phase shift).

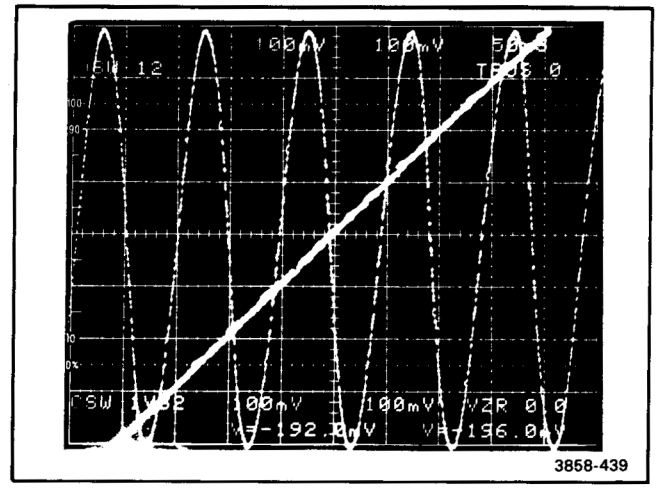


Figure 4-4. CH 1 vs CH 2.

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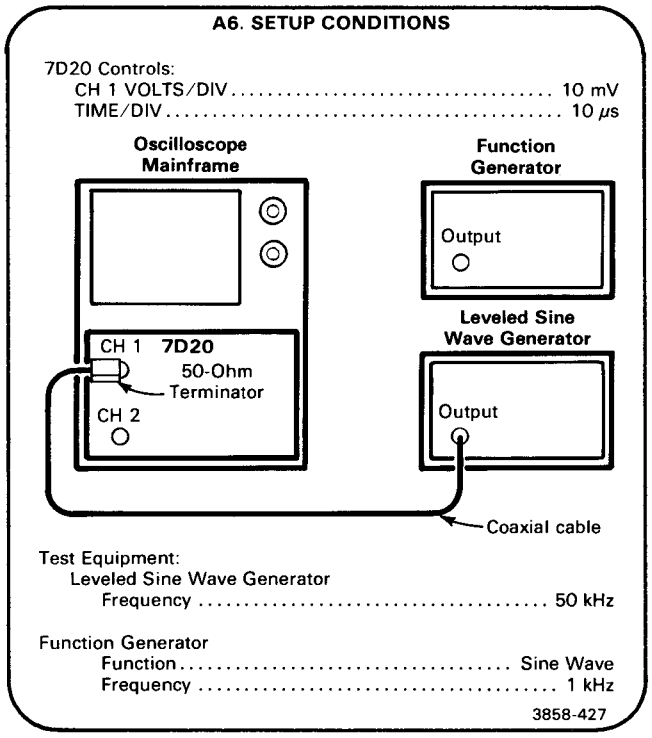
A6. CHECK BANDWIDTH

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

a. Perform step A2 Initialization Procedure.



b. Set CH 1 POSITION control and leveled sine-wave generator Amplitude controls for an eight-division 50 kilohertz signal centered on oscilloscope mainframe crt.

c. Set leveled sine-wave generator to 70 megahertz, and TIME/DIV to 50nS.

d. **CHECK**—For at least 5.7 divisions of displayed signal.

e. Set AQR MODE to CH 2.

f. Set CH 2 VOLTS/DIV to 10mV and TIME/DIV to 10μS.

g. Move coaxial cable and 50-ohm terminator from CH 1 input to CH 2 input.

h. Set leveled sine-wave generator to 50 kilohertz.

i. Set CH 2 POSITION control and leveled sine-wave generator Amplitude controls for an eight-division 50 kilohertz signal centered on oscilloscope mainframe crt.

j. Set leveled sine-wave generator to 70 megahertz, and TIME/DIV to 50nS.

k. **CHECK**—For at least 5.7 divisions of display signal.

l. Remove coaxial cable from leveled sine-wave generator and connect it to output of function generator.

m. Set TIME/DIV to 500μS.

n. Set function generator Amplitude control for an eight-division one kilohertz signal centered on oscilloscope mainframe crt.

o. Set TIME/DIV to 50mS.

p. Set function generator to 10 hertz.

q. **CHECK**—For at least 5.7 divisions of displayed signal on oscilloscope mainframe crt.

r. Set function generator to 1 kilohertz.

s. Set TIME/DIV to 500μS.

t. Move coaxial cable and 50-ohm terminator from CH 2 input to CH 1 input.

u. Set AQR MODE to CH 1.

v. Set function generator for an eight-division one kilohertz signal centered on oscilloscope mainframe.

w. Set TIME/DIV to 50mS.

x. Set function generator to 10 hertz.

y. **CHECK**—For at least 5.7 divisions displayed signal on oscilloscope mainframe crt.

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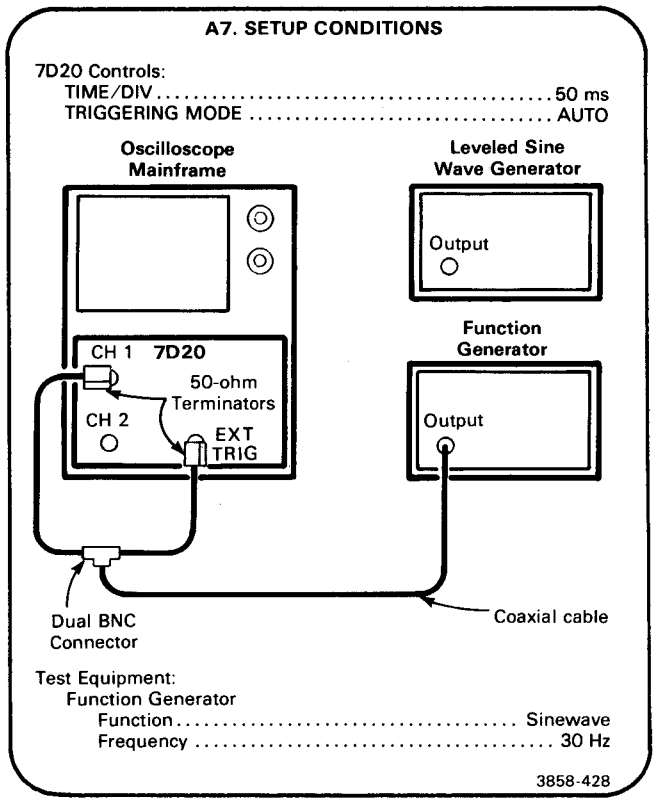
A7. CHECK TRIGGERING

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

a. Perform step A2 Initialization Procedure.



b. **CHECK**—Using settings listed in Table 4-4, check for stable triggering and a lighted TRIG'D lamp.

c. Set CH 1 VOLTS/DIV to 100mV and TIME/DIV to 50nS.

d. Move coaxial cable from function generator output to leveled sine-wave generator output.

e. Set leveled sine-wave generator frequency to 30 MHz and adjust amplitude for a 60 millivolt display on oscilloscope mainframe crt.

f. **CHECK**—Using settings listed in Table 4-5 check for stable triggering and lighted TRIG'D lamp.

TABLE 4-4
Low Frequency Triggering Checks

7D20 TRIGGERING		Function Generator		
COUPLING	SOURCE	Frequency	Displayed Signal/ External Amplitude	TIME/DIV
AC	CH1	30 Hz	0.4 Div	10mS
AC HF REJ	CH1	30 Hz	0.4 Div	10mS
DC	CH1	30 Hz	0.4 Div	10mS
DC HF REJ	CH1	30 Hz	0.4 Div	10mS
AC HF REJ	CH1	30 kHz	0.4 Div	20μS
DC HF REJ	CH1	30 kHz	0.4 Div	20μS
AC LF REJ	CH1	50 kHz	0.4 Div	20μS
AC	EXT	30 Hz	60 mV	10mS
AC HF REJ	EXT	30 Hz	60 mV	10mS
DC	EXT	30 Hz	60 mV	10mS
AC HF REJ	EXT	30 kHz	60 mV	20μS
AC LF REJ	EXT	50 kHz	60 mV	20μS

TABLE 4-5
High Frequency Triggering Checks

7D20 TRIGGERING		Leveled Sine-Wave Generator		
COUPLING	SOURCE	Frequency	Amplitude	TIME/DIV
DC	EXT	30 MHz	60 mV	50nS
AC	EXT	30 MHz	60 mV	50nS
AC LF REJ	EXT	30 MHz	60 mV	50nS
DC	CH1	30 MHz	0.4 div	50nS
AC	CH1	30 MHz	0.4 div	50nS
AC LF REJ	CH1	30 MHz	0.4 div	50nS
AC LF REJ	CH1	70 MHz	1.0 div	50nS, HMAG
DC	CH1	70 MHz	1.0 div	50nS, HMAG
AC	CH1	70 MHz	1.0 div	50nS, HMAG
AC	EXT	70 MHz	150 mV	50nS, HMAG
DC	EXT	70 MHz	150 mV	50nS, HMAG
AC LF REJ	EXT	70 MHz	150 mV	50nS, HMAG

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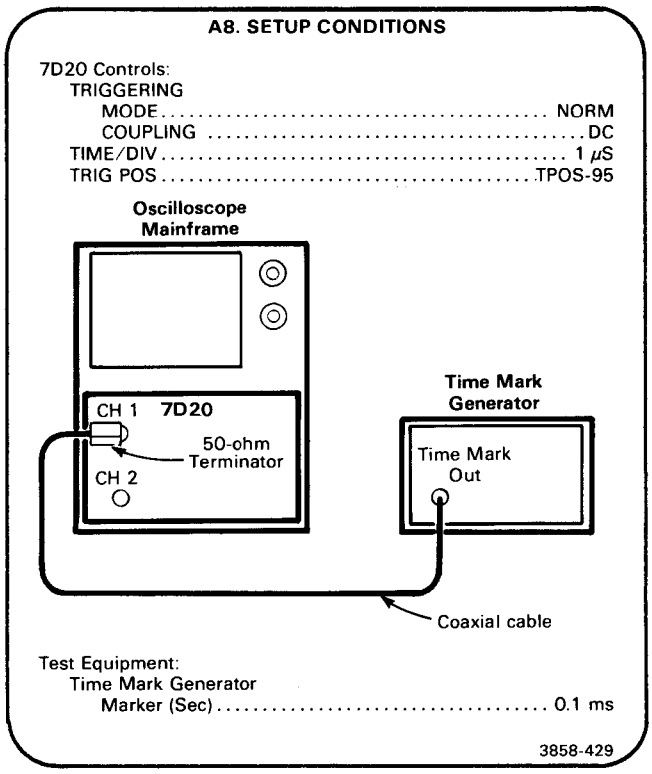
A8. CHECK TIMING

NOTE

If the preceding step was not performed, first perform step A1 then proceed.

a. Perform step A2 Initialization Procedure.



b. Set CH 1 VOLTS/DIV switch and VARIABLE control to display at least four divisions of time mark signal.

c. Set CURSORS "1" control so that cursor falls on rising edge of time mark as close to 50% point as possible, see Figure 4-5.

d. **CHECK**—Cursors readout is between T=99.9 and T=100.1μS.

e. **CHECK**—Using TIME/DIV, TRIG POS, and time mark settings listed in Table 4-6, check each TIME/DIV position for indicated readout reading.

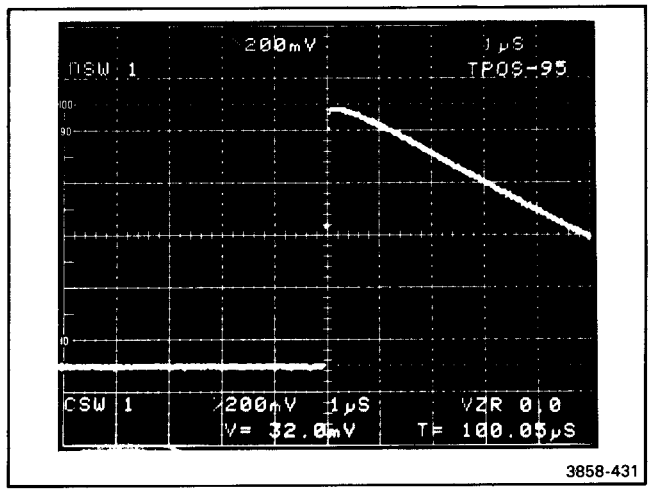


Figure 4-5. Measuring Timing to 0.1%.

TABLE 4-6
Timing Accuracy

TIME/DIV	TRIG POS	Time Mark	Cursor Readout
1μS	-95	0.1 ms	99.9-100.1μS
2μS	-95	0.2 ms	199.8-200.2μS
5μS	-95	0.5 ms	499.5-500.5μS
10μS	-95	1 ms	999μS-1.001mS
20μS	-95	2 ms	1.998-2.002mS
50μS	-95	5 ms	4.995-5.005mS
100μS	-95	10 ms	9.999-10.01mS
200μS	-95	20 ms	19.99-20.02mS
500μS	-95	50 ms	49.95-50.05mS
1mS	-95	0.1 s	99.9-100.1mS
2mS	-95	0.2 s	199.8-200.2mS
20mS[1]	-95	2 s	1.998-2.002S
500mS[1]	-35	2 s	19.98-20.02S
5S[1,2]	-35	5 s	199.8-200.2S

[1] **Press HOLD NEXT and wait for display to stop rolling before making cursor measurement.**
[2] **This test will take about 250 seconds.**

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PART III—ADJUSTMENT PROCEDURE

The Part III—Adjustment Procedure contains the information necessary to perform all internal adjustments. This procedure provides a logical sequence of adjustment steps, and is intended to return the instrument to specified operation following repair, or as a part of a routine maintenance program.

Most adjustment steps can be performed independently, except when it is specifically noted that the adjustment sequence is important, or interaction is involved. In all cases, perform the appropriate steps in the Performance Check Procedure or Functional Check Procedure following any repair or adjustment activity.

NOTE

Limits, tolerances, and waveform information in this section are not guaranteed specifications except when they agree with the Performance Requirements in the Specification tables.

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ADJUSTMENT INITIAL SETUP PROCEDURE

NOTE

The following Adjustment Procedure must be performed within the ambient temperature range of +20° and +30° C, to assure proper instrument adjustment.

CAUTION

To avoid instrument damage, it is recommended that the POWER switch be turned off before removing or replacing the 7D20.

1. Remove the 7D20 side covers.
2. Install the 7D20 in the oscilloscope mainframe.
3. Connect the oscilloscope mainframe to a suitable power source and turn power on. Allow at least 20 minutes warmup before beginning the procedure.

***Located on the A5—CCD board.**

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A. SIGNAL ACQUISITION AND DISPLAY

Equipment Required (Numbers correspond to those listed in Table 4-3, Test Equipment).

1. Oscilloscope Mainframe
2. Test Oscilloscope
3. Digital Multimeter (DMM)
4. Calibration Generator
9. Cable
10. Flexible Plug-In Extender (three required)
11. Coaxial Cable (two required)
12. 50-ohm Terminator
13. 2X Attenuator
14. 10X Attenuator
16. Alignment Tool

A1. PRELIMINARY SETUP

a. Perform the Adjustment Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and the change Information at the rear of the manual for any modifications which may affect this procedure.

c. Set the Oscilloscope Mainframe controls:
Power ..... On
Vertical Mode ..... Left
Intensity ..... Visible Display
Focus ..... Well defined display

d. Set the 7D20 controls:
HORIZ POSITION .. Fully clockwise (In detent)
CH 1 VARIABLE ..... CAL (In detent)
CH 1 POSITION ..... Midrange
CH 2 VARIABLE ..... CAL (In detent)
CH 2 POSITION ..... Midrange

e. Press MENU (pushbutton will light). If MASTER MENU is not displayed, press MEMORY DISPLAY pushbutton number 6. From the MASTER MENU list displayed on the oscilloscope mainframe crt, select DISPLAY CAL PATTERN by pressing MEMORY DISPLAY pushbutton number 3.

f. While observing the DISPLAY CAL PATTERN displayed on the oscilloscope mainframe crt, use screwdriver to set VERT GAIN, VERT CTR, HORIZ GAIN and HORIZ CTR controls to place corner markers of DISPLAY CAL PATTERN on center 6 × 8 divisions of graticule, as shown in Figure 4-6.

g. Set VECT LIN adjustment for minimum trace separation of the diagonal lines on DISPLAY CAL PATTERN as shown in Figure 4-6.

h. To return to MASTER MENU, press MEMORY DISPLAY pushbutton number 6. To turn off MASTER MENU display, press MENU.

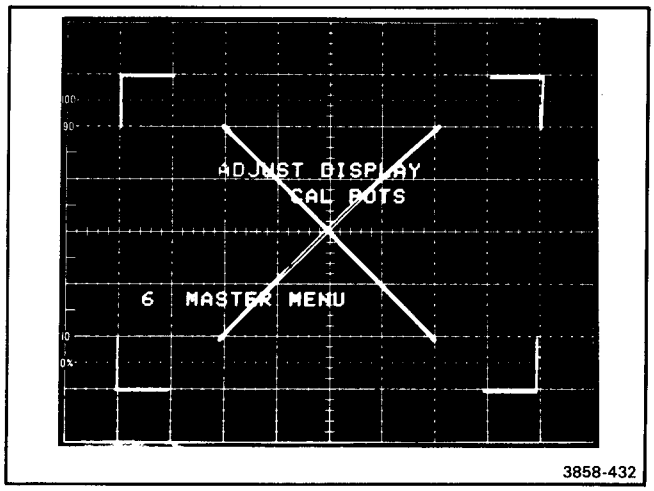

Figure 4-6. Display Adjust Pattern.

A2. INITIALIZATION PROCEDURE

a. Press MENU (pushbutton will light).

b. If MASTER MENU is not displayed press MEMORY DISPLAY pushbutton number 6.

c. From displayed MASTER MENU list, select UTILITIES by pressing MEMORY DISPLAY pushbutton number 4.

d. From displayed UTILITIES list select INIT FRONT PANEL by pressing MEMORY DISPLAY pushbutton number 5.

e. To return to MASTER MENU, press MEMORY DISPLAY pushbutton number 6. To turn off MASTER MENU display, press MENU.

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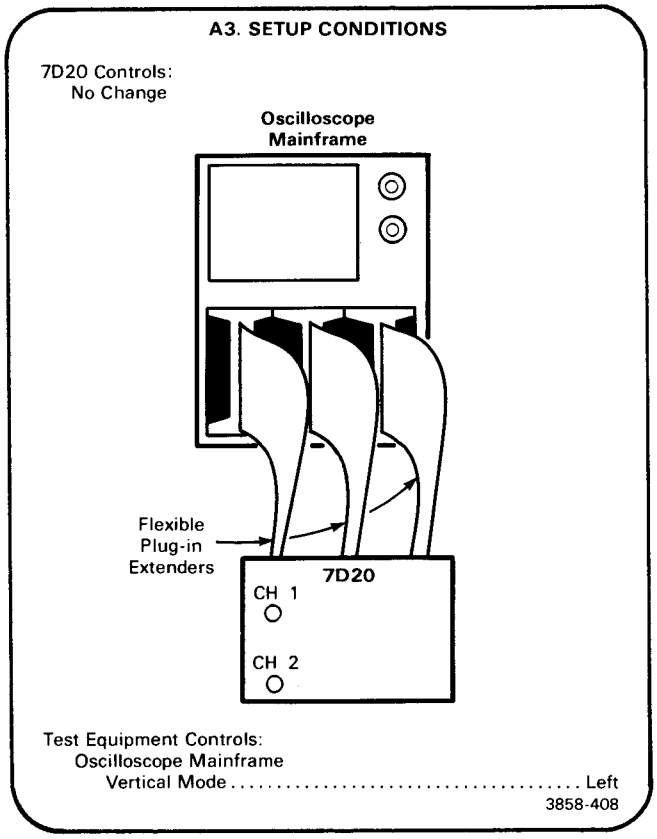
A3. ADJUST DISPLAY OFFSET AND DISPLAY BALANCE (R1000, R900)

NOTE

First perform steps A1 and A2 then proceed.



a. Press *f* (function), then press TEST. From the TEST MENU list displayed on the oscilloscope mainframe crt select CALIBRATION by pressing MEMORY DISPLAY pushbutton number 2.

b. From CALIBRATION list displayed on oscilloscope mainframe crt, select VERTICAL DISPLAY DAC by pressing MEMORY DISPLAY pushbutton number 2.

c. **EXAMINE**—Trace segmentation should not be visible (one continuous trace will appear if segments are properly aligned, see Figure 4-7A and B).

d. **ADJUST**—DAC Gain Balance adjustment R900, and DAC Offset adjustment, R1000, to vertically align the left two trace segments with the right trace segment.

e. Press MENU (pushbutton will light). If MASTER MENU is not displayed press MEMORY DISPLAY pushbutton number 6. From displayed MASTER MENU list, select DISPLAY CAL PATTERN by pressing MEMORY DISPLAY pushbutton number 3.

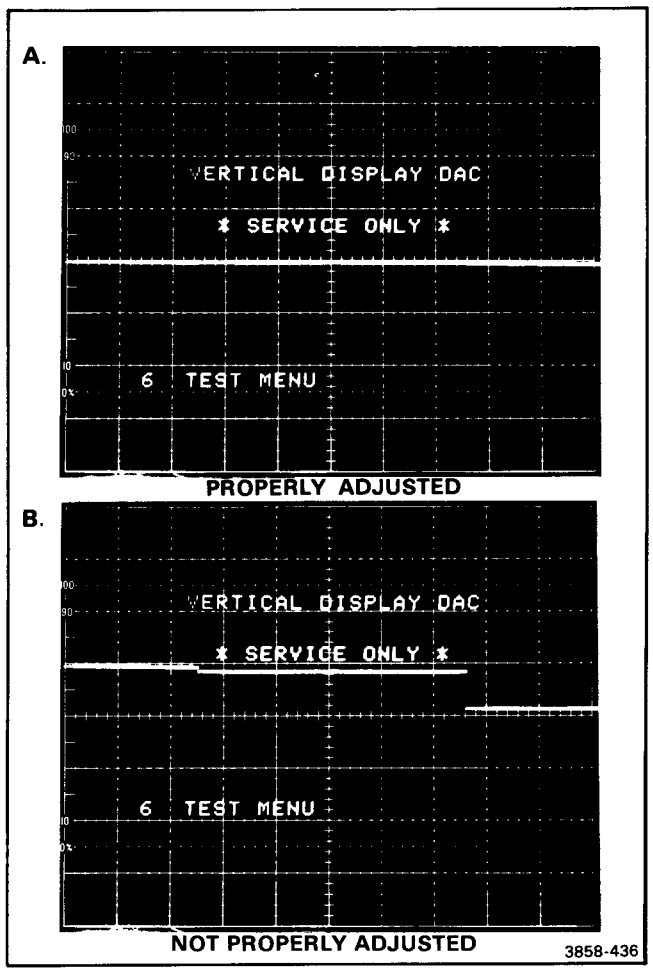


Figure 4-7. Display Offset adjustment.

f. While observing display cal pattern displayed on oscilloscope mainframe crt, set VERT GAIN, VERT CTR, HORIZ GAIN, and HORIZ CTR controls to place corner markers of displayed adjustment pattern on center 6 × 8 divisions of graticule, as shown in Figure 4-6.

g. Set VECT LIN control for minimum trace separation of diagonal lines on displayed adjustment pattern as shown in Figure 4-6.

h. To turn DISPLAY CAL PATTERN off press MENU.

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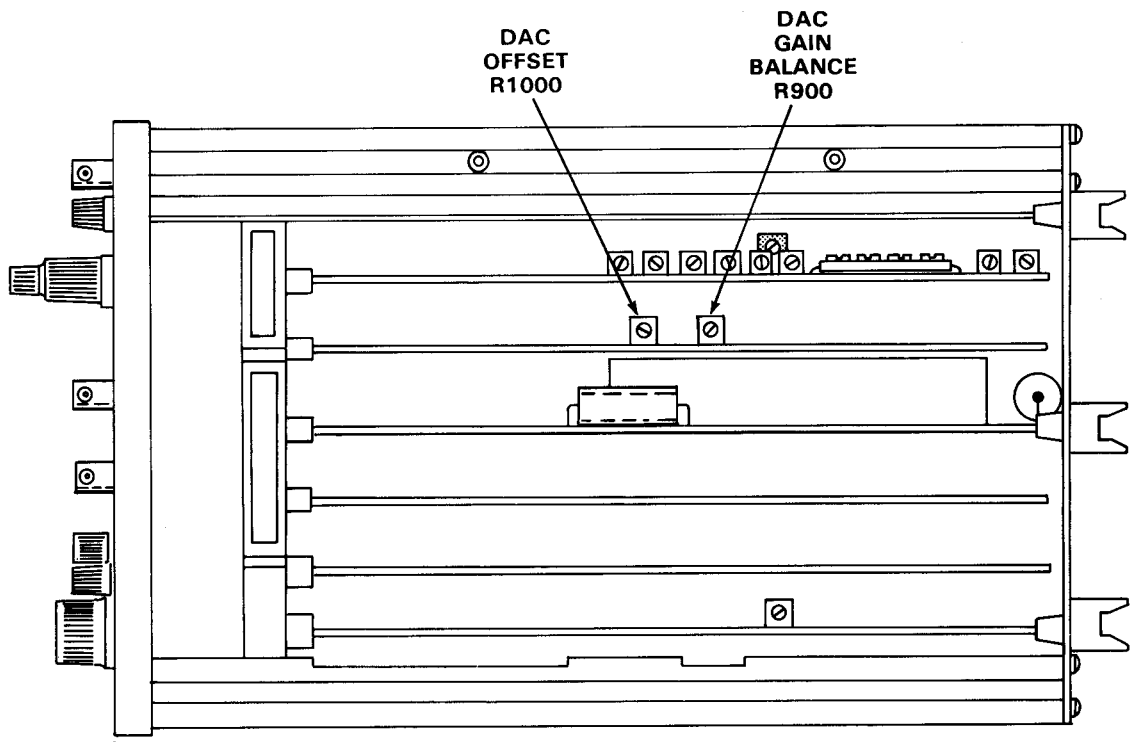
A3. ADJUSTMENT LOCATIONS



TOP VIEW OF 7D20

3858-405

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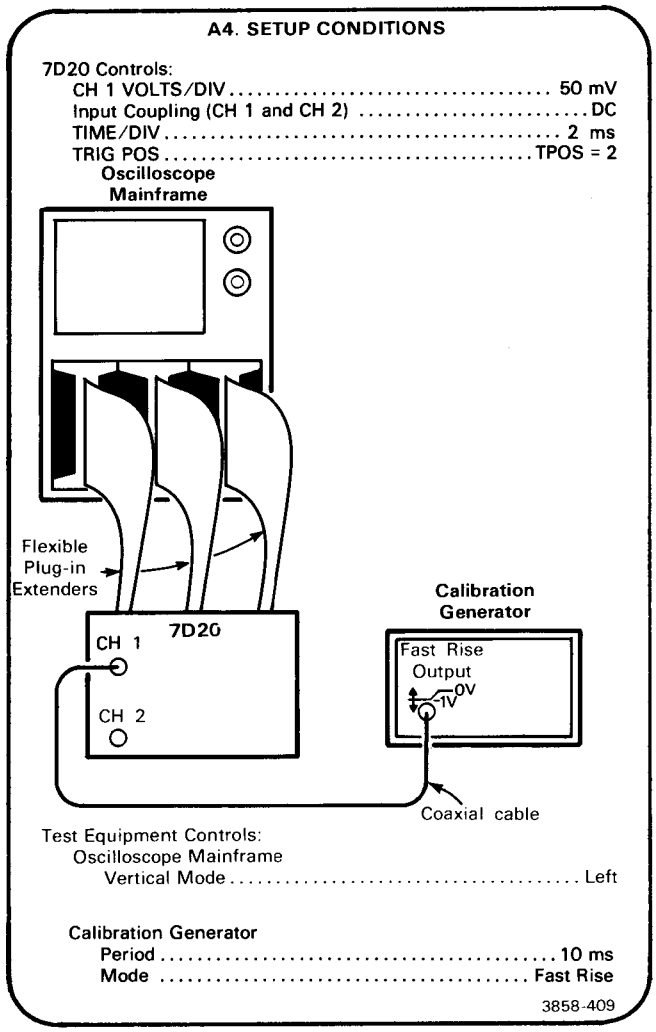
A4. ADJUST LOW FREQUENCY GAIN (R1003, R1033)

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

a. Perform step A2 Initialization Procedure.



b. Set CH 1 POSITION control and calibration generator Pulse Amplitude control for a six-division signal centered on the oscilloscope mainframe crt.

c. **EXAMINE**—Oscilloscope mainframe displayed waveform for flat top within 0.08 division.

d. **ADJUST**—CH 1 LF Gain adjustment, R1003, for optimum flat top on oscilloscope mainframe displayed waveform.

e. Connect Fast Rise output from calibration generator to CH 2 input.

f. Set AQR MODE to CH 2.

g. Set CH 2 VOLTS/DIV to 50mV.

h. Set calibration generator Pulse Amplitude control and CH 1 POSITION control for a six-division display centered on oscilloscope mainframe.

i. **EXAMINE**—Oscilloscope mainframe displayed waveform for flat top, within 0.08 division.

j. **ADJUST**—CH 2 LF Gain adjustment, R1033, for optimum flat top on oscilloscope mainframe displayed waveform.

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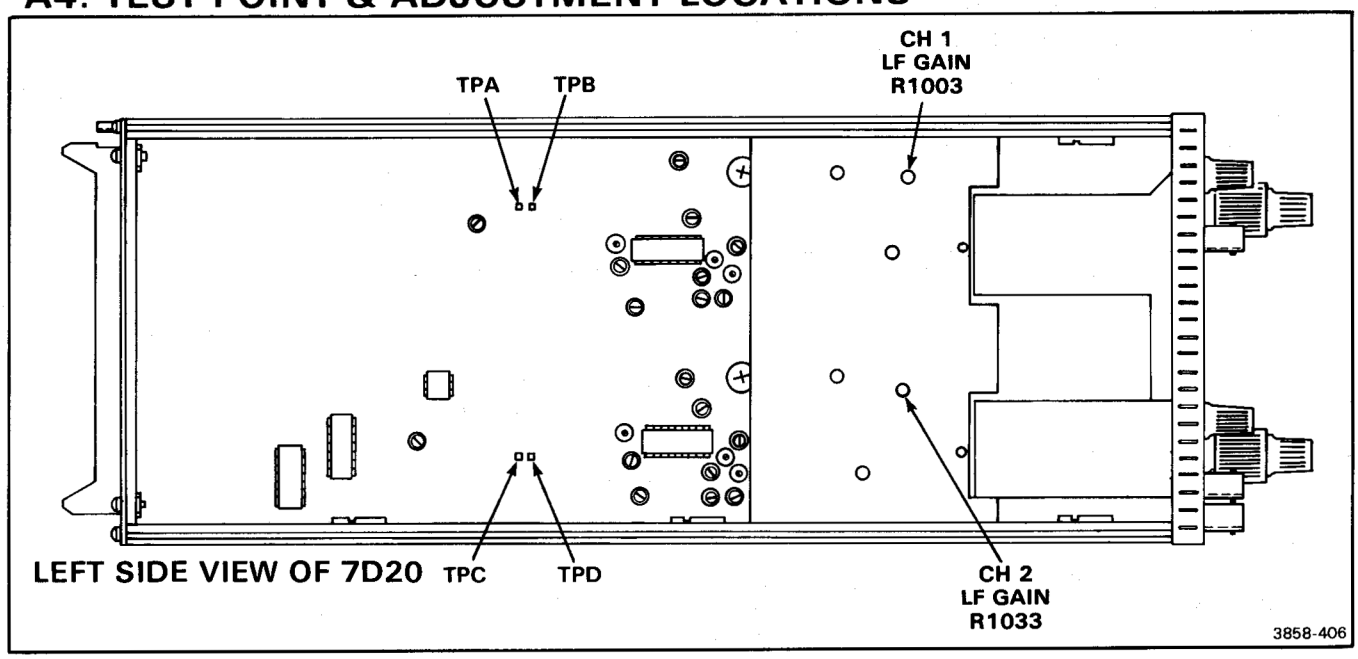
A4. TEST POINT & ADJUSTMENT LOCATIONS



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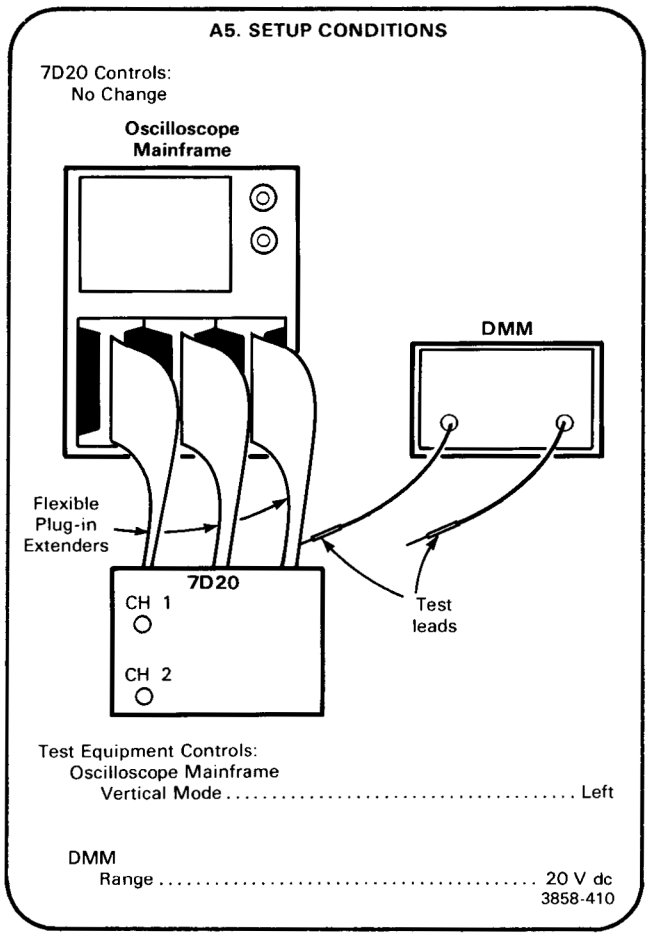
A5. ADJUST STEP ATTENUATOR BALANCE AND 5 mV OFFSET BALANCE (R902, R801, R934, R733, R751, R701, R518, R445)

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

a. Perform A2 Initialization Procedure, then proceed.



b. With CH 1 POSITION control, move displayed trace to center graticule line.

c. Set CH 1 and CH 2 input coupling to GND.

d. **EXAMINE**—For less than 0.24 division trace shift while switching CH 1 VOLTS/DIV switch between 5, 10, 20 and 50mV settings.

e. **ADJUST**—CH 1 Step Balance adjustment, R902, for minimum trace shift, while switching CH 1 VOLTS/DIV between 10, 20, and 50mV.

f. **ADJUST**—CH 1 Variable Balance adjustment, R701, for minimum trace shift, while rotating CH 1 VARIABLE (VOLTS/DIV) control throughout its range.

g. **ADJUST**—CH 1, 5mV Offset adjustment, R801, for minimum trace shift while switching CH 1 VOLTS/DIV between 10 mV and 5 mV.

h. Set AQR MODE to CH 2, and with CH 2 POSITION control, move displayed trace to center graticule line.

i. **EXAMINE**—For less than 0.24 division trace shift while switching CH 2 VOLTS DIV between 5, 10, 20, and 50mV.

j. **ADJUST**—CH 2 Step Balance adjustment, R934, for minimum trace shift, while switching CH 2 VOLTS/DIV between 10, 20, and 50mV.

k. **ADJUST**—CH 2 Invert Balance, R733, for minimum trace shift, while switching between INV (invert) and non-invert.

l. **ADJUST**—CH 2, 5 mV Offset adjustment, R833, for minimum trace shift while switching CH 1 VOLTS/DIV between 10 mV and 5 mV.

m. Set AQR MODE to BOTH. Then set CH 1 and CH 2 VOLTS/DIV switches to 10mV.

n. Mechanically center CH 1 and CH 2 POSITION controls.

o. Connect shorting strap between GND and TP1230.

p. Connect DMM test leads between TPC and TPD.

q. **ADJUST**—CH 2 Position Offset adjustment, R751, for a DMM reading of zero volts, within one millivolt.

r. Connect shorting strap between GND and TP1220.

s. Connect DMM test leads between TPA and TPB.

t. **ADJUST**—CH 1 Position Offset, R720, for a DMM reading of zero volts, within one millivolt.

u. Connect DMM test leads between TP902 and J400.

v. **ADJUST**—CH 1 Trigger Offset, R518, for a DMM reading of zero volts, within one millivolt.

w. Connect DMM test leads between TP902 and J550. Then connect shorting strap between GND and TP1230.

x. **ADJUST**—CH 2 Trigger Offset adjustment, R445, for a DMM reading of zero volts, within one millivolt.

y. Remove DMM Test leads.

z. Remove shorting strap.

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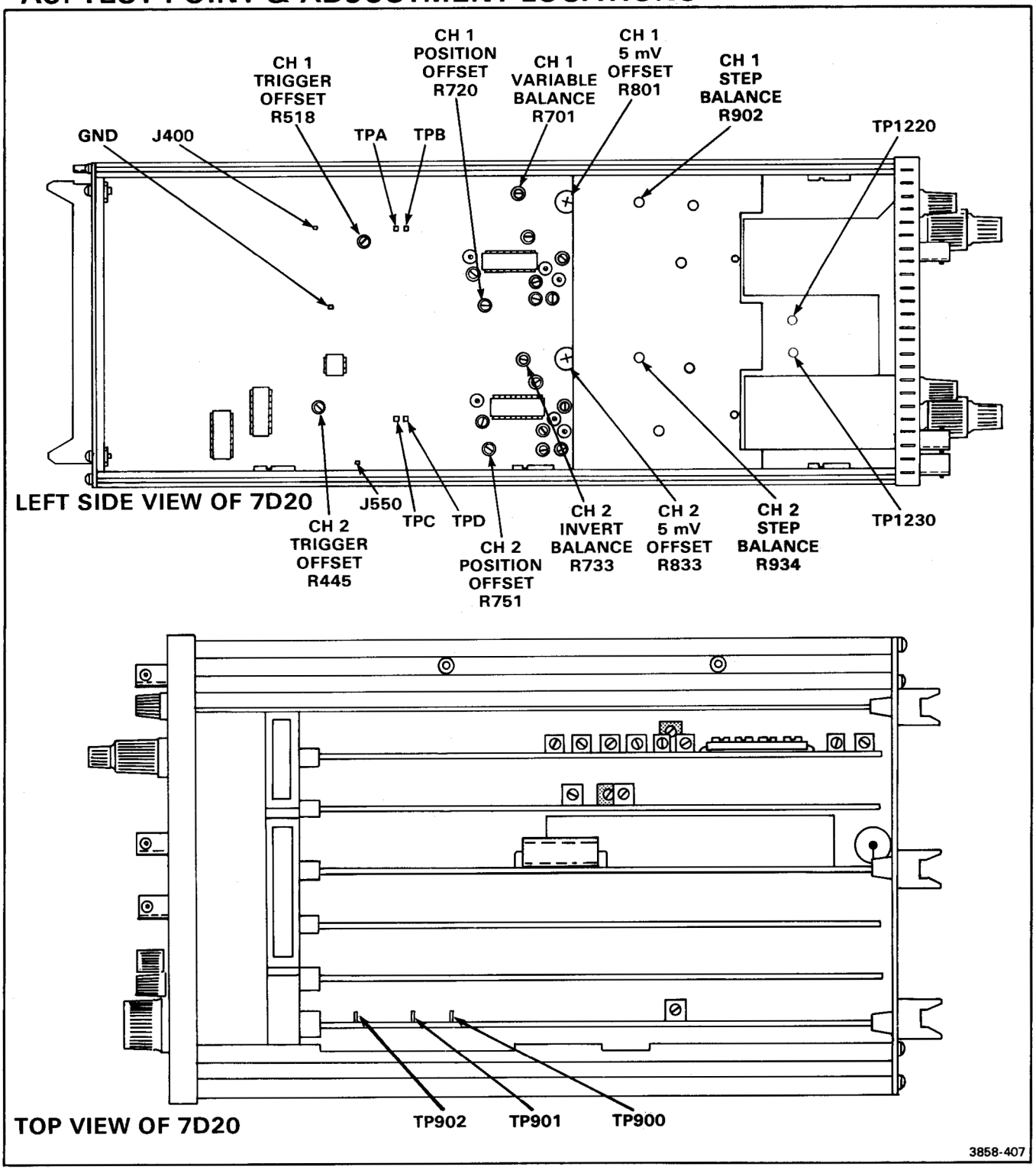
A5. TEST POINT & ADJUSTMENT LOCATIONS



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A6. ADJUST CHANNEL 1 CCD CENTERING, BALANCE, GAIN, AND REFERENCE VOLTAGES (R410, R411, R344, R311, R310)

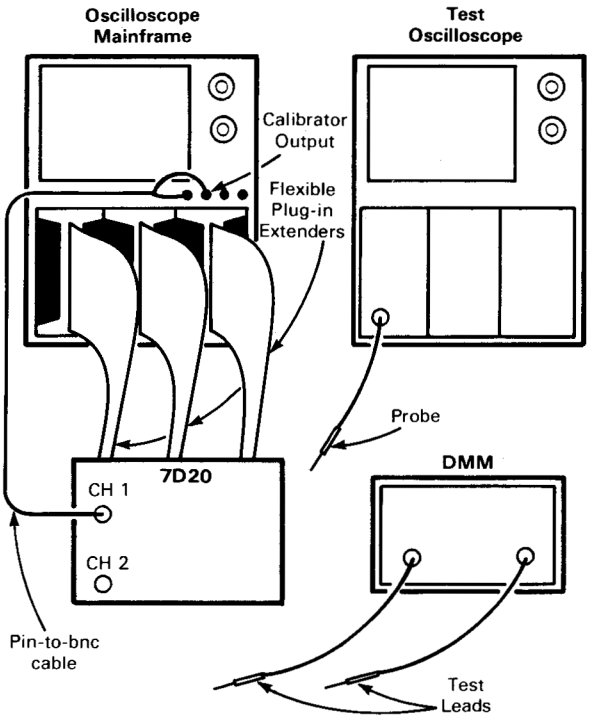
NOTE

If the preceding step was not performed, first perform step A1; further, steps A3, A4, and A5 must be performed before performing this step.

a. Perform step A2 Initialization Procedure, then proceed.

A6. SETUP CONDITIONS

7D20 Controls:
- CH 1 VOLTS/DIV ..... 10 mV
- CH 1 Input Coupling ..... GND
- TIME/DIV ..... 500 μS



Test Equipment Controls:
- Oscilloscope Mainframe
  - Calibrator ..... 40 mV
- DMM
  - Range ..... 20 V dc
- Test Oscilloscope
  - Vertical Deflection ..... 50 mV/div
  - Input Coupling ..... AC
  - Sweep Rate ..... 500 μs/div
  - Triggering ..... HF REJ

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b. Mechanically center CH 1 POSITION control.

c. Connect shorting strap between GND and TP1220.

d. **EXAMINE**—VZR readout reads between −0.2 and +0.2.

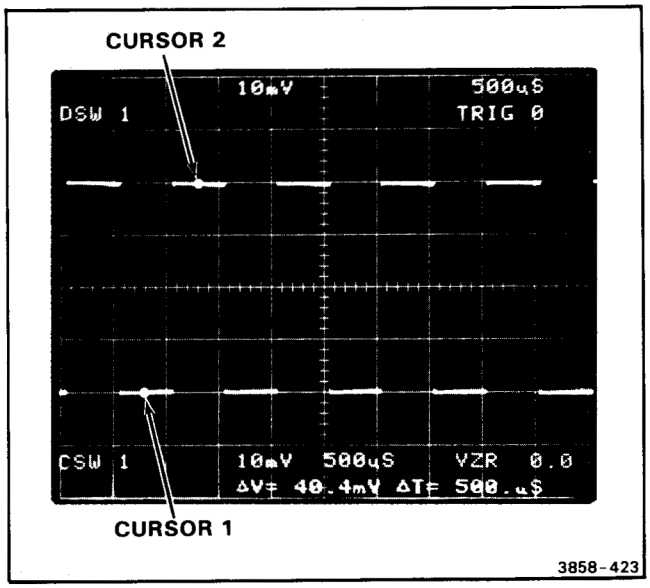

Figure 4-8. Typical CURSORS△ Display.

e. **ADJUST**—CH 1 Centering adjustment, R410, to align trace with center graticule line; VZR readout should read between −0.2 and +0.2.

f. Remove grounding strap from TP1220.

g. Set CH 1 input coupling to AC.

h. Connect test oscilloscope probe to J700-2.

i. **ADJUST**—CH 1 Balance adjustment, R411, for minimum signal.

j. Disconnect test oscilloscope probe and mechanically center CH 1 AQR GAIN adjustment.

k. Set CURSORS to △ON by pressing *f* pushbutton; then press CURSORS △ON (pushbutton will light).

l. Set CURSORS 1 and 2 as shown in Figure 4-8.

m. Press AVE (pushbutton will light).

n. **EXAMINE**—CURSORS readout reads V=40mV within 0.4 millivolts.

o. **ADJUST**—Ch 1 Gain adjustment, R344, so that CURSORS readout reads △V=40.0.

p. Set CH 1 VOLTS/DIV to 20mV.

q. Press AVE to turn off lighted pushbutton.

r. With CH 1 POSITION control, move display to center screen.

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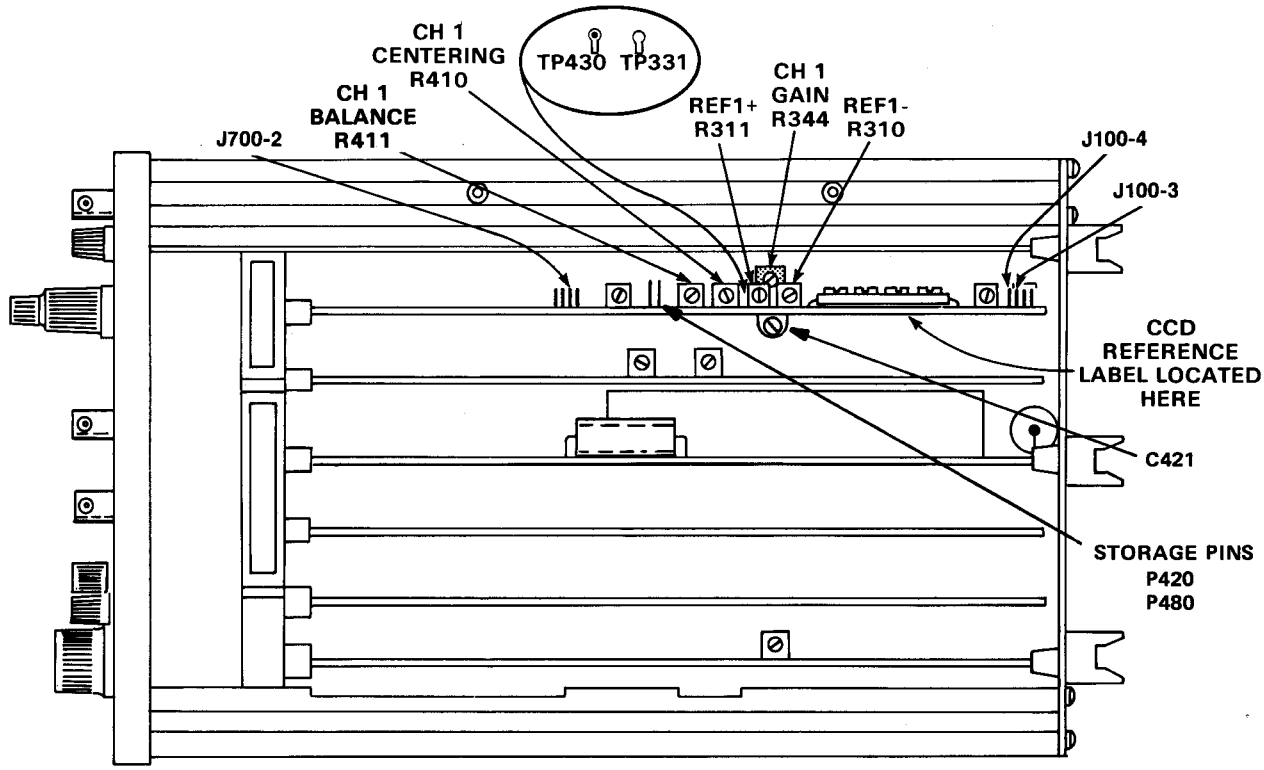
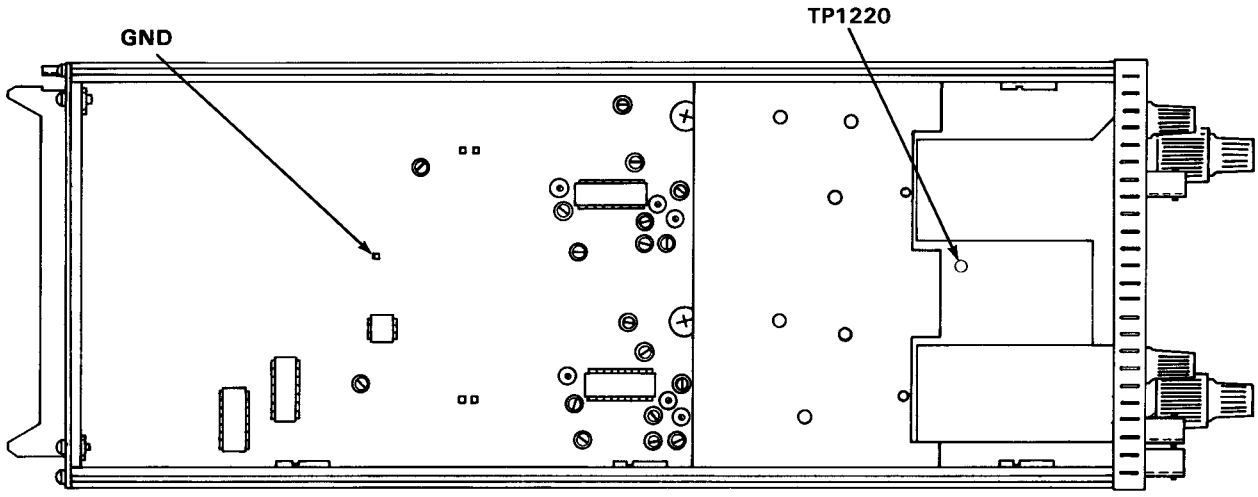
A6. TEST POINT & ADJUSTMENT LOCATIONS



TOP VIEW OF 7D20



LEFT SIDE VIEW OF 7D20

3858-403B

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s. **EXAMINE**—With the CH 1 POSITION control, move the two division display over the entire graticule area and observe that the CURSORS readout does not vary more than 2.4 mV. If CURSORS readout does not vary more than 2.4 mV ignore steps t through ss.

NOTE

The CCD Reference Voltage Label referred to in this procedure can be found attached to the shield mounted on the CCD board; see Test Point and Adjustment Locator. If the CCD Reference Voltage Label cannot be found, ignore parts t thru x of this step, and go to part y.

t. Connect DMM test leads between GND and test point P100-4.

u. **ADJUST**—REF1+ adjustment, R311, to match DMM reading to REF1+ voltage marked on the CCD Reference label.

v. Connect DMM test leads between GND and test point P100-3.

w. **ADJUST**—REF1- adjustment, R310, to match DMM reading with REF1- voltage marked on CCD Reference label.

x. **EXAMINE**—With the CH 1 POSITION control, move the two-division display over the entire graticule area, and observe that CURSORS readout does not vary more than 2.4 mV. If CURSORS readout does not vary more than 2.4 mV, ignore remainder of this step and perform parts a through o, then continue with step A7.

NOTE

The remainder of this procedure is intended for instruments which do not have a CCD Reference Label and for instruments with a label which cannot be adjusted to meet specifications in step x, using voltages listed on label.

y. Mechanically midrange CH 1 POSITION control.

z. Mechanically center adjustment R411 (Ch 1 Balance), R410 (Ch 1 Centering) R311 (REF1+), and R310 (REF1-).

aa. **ADJUST**—Set CH 1 input coupling to AC and position two-division display to center screen with Ch 1 Centering adjustment, R410.

bb. **ADJUST**—CH 1 Gain adjustment, R344, to set CURSORS readout to read ΔV=40mV, within one millivolt.

cc. Connect the test oscilloscope probe to test point TP430.

dd. Note exact amplitude display on test oscilloscope.

ee. **ADJUST**—With CH 1 POSITION control, move two-division display up three divisions and note exact amplitude on test oscilloscope. Then with CH 1 POSITION control, move display six divisions down and note exact amplitude on test oscilloscope; if test oscilloscope amplitude varies less than 5 millivolts when display is positioned between the top and bottom of the graticule, proceed to part kk. If test oscilloscope amplitude varies more than five millivolts, continue with the following; from the two amplitudes previously noted, determine whether lowest amplitude was at top or bottom of graticule, then position 7D20 display to that position. Adjust REF1+ adjustment, R311, to move 7D20 display one minor division for every 5 millivolts difference in amplitude toward center of graticule.

ff. Set CH 1 input coupling to GND.

gg. Mechanically center CH 1 POSITION control; and connect shorting strap between ground and TP1220.

hh. **ADJUST**—Ch 1 Centering adjustment, R410, for VZR=0, then remove shorting strap from TP1220.

ii. Set CH 1 input coupling to AC.

jj. **INTERACTION**—Repeat step ee.

kk. Connect the test oscilloscope probe to test point TP331.

ll. With CH 1 POSITION, move two-division display to center screen. Note exact amplitude of test oscilloscope display.

mm. **ADJUST**—With CH 1 POSITION control, move two-division display up three divisions, and note exact amplitude on test oscilloscope. Then move 7D20 display six divisions down, and note exact amplitude on test oscilloscope; if test oscilloscope amplitude varies less than five millivolts when display is positioned between top and bottom of graticule proceed to part ss. If test oscilloscope amplitude varies more than five millivolts continue with following. From the two amplitudes previously noted, determine whether lowest amplitude was at top or bottom of graticule, then position 7D20 display to that position. Adjust REF1- adjustment, R310, to move 7D20 display one minor division for every 5 millivolts difference in amplitude, toward the center of the graticule.

nn. Set CH 1 input coupling to GND.

oo. Mechanically midrange CH 1 POSITION control.

pp. **ADJUST**—Ch 1 Centering adjustment, R410, for VZR=0.

qq. Set CH 1 input coupling to AC.

rr. **INTERACTION**—Repeat part mm.

ss. If criteria of part mm has been met, perform parts a through s, and ignore remainder of this step.

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A7. ADJUST CHANNEL 2 CCD CENTERING, BALANCE, GAIN, AND REFERENCE VOLTAGES (R510, R511, R377, R111, R110)

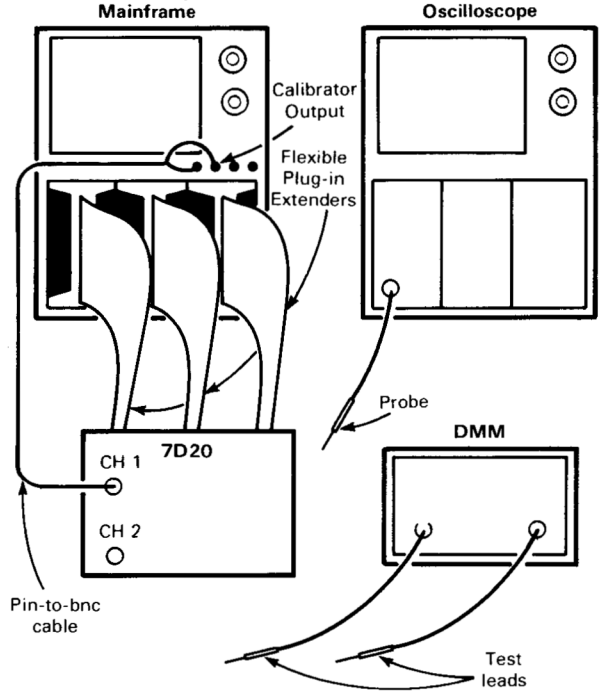
NOTE

If the preceding step was not performed, first perform step A1; further, steps A3, A4, and A5 must be performed before performing this step.

a. Perform step A2 Initialization Procedure, then proceed.

A7. SETUP CONDITIONS

7D20 Controls:
- AQR MODE ..... CH 2
- CH 2 VOLTS/DIV ..... 10 mV
- CH 2 Input Coupling ..... GND
- TIME/DIV ..... 500 μs



Test Equipment Controls:

Oscilloscope Mainframe
- Calibrator ..... 40 mV

DMM
- Range ..... 20 V dc

Test Oscilloscope
- Vertical Deflection ..... AC
- Input Coupling ..... AC
- Sweep Rate ..... 500 μs/div
- Triggering ..... HF REJ

3858-402

b. Mechanically center CH 2 POSITION control.

c. Connect shorting strap between GND and TP1230.

d. **EXAMINE**—VZR readout reads between -0.2 and +0.2.

e. **ADJUST**—CH 2 Center adjustment, R510, to align trace with center graticule line.

f. Remove grounding strap from TP1230.

g. Set CH 2 input coupling to AC.

h. Connect test oscilloscope probe to J700-1.

i. **ADJUST**—CH 2 Balance adjustment, R511, for minimum signal.

j. Mechanically midrange CH 2 ARQ GAIN adjustment.

k. Set CURSORS to ΔON by pressing *f* pushbutton, then press CURSORS ΔON (pushbutton will light).

l. Set CURSORS 1 and 2 as shown in Figure 4-8.

m. Press AVE.

n. **EXAMINE**—CURSORS readout reads V=40mV, within 0.4 millivolts.

o. **ADJUST**—Ch 2 Gain adjustment, R377, so that CURSORS readout reads ΔV=40.0.

p. Set CH 2 VOLTS/DIV to 20mV.

q. Press AVE to turn off lighted pushbutton.

r. With CH 2 POSITION control, move display to center screen.

s. **EXAMINE**—With the CH 2 POSITION control, move the two-division display over the entire graticule area and observe that the CURSORS readout does not vary more than 2.4 mV. If CURSORS readout does not vary more than 2.4 mV, ignore steps t through ss.

NOTE

The CCD Reference Voltage Label referred to in this procedure can be found attached to the shield mounted on the CCD board; see Test Point and Adjustment Locator. If the CCD Reference Voltage Label cannot be found, ignore parts t through x of this step, and go to part y.

t. Connect DMM test leads between GND and test point J100-2.

u. **ADJUST**—REF2+ adjustment, R111, to match DMM reading with REF2+ voltage marked on the CCD Reference label.

v. Connect DMM test leads between GND and test point J100-1.

w. **ADJUST**—REF2- adjustment, R110, to match DMM reading with REF2- voltage marked on CCD Reference label.

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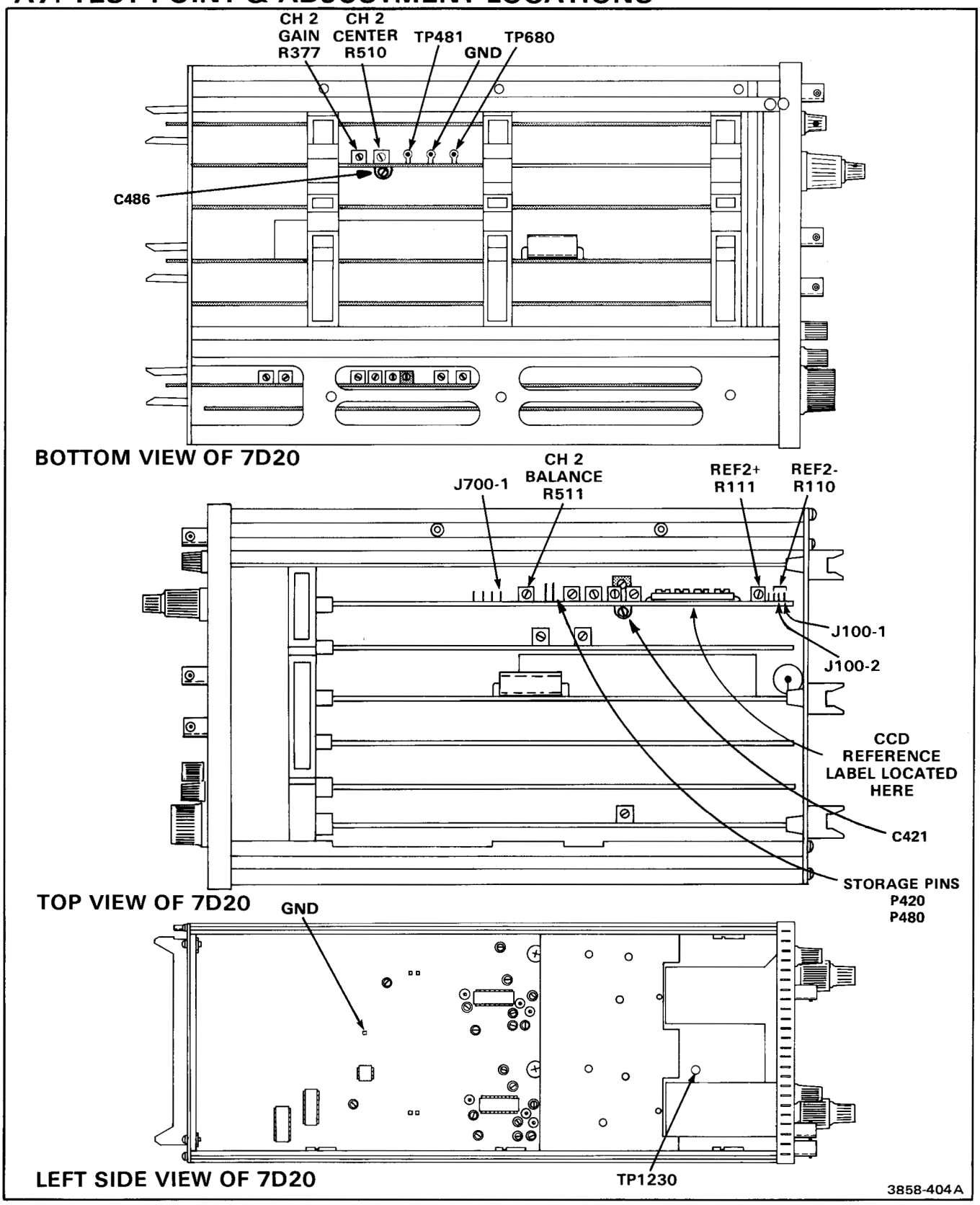
A7. TEST POINT & ADJUSTMENT LOCATIONS



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x. **EXAMINE**—With the CH 1 POSITION control, move the two-division display over the entire graticule area, and observe that CURSORS readout does not vary more than 2.4 mV. If CURSORS readout does not vary more than 2.4 mV, ignore remainder of this step and perform parts a through o, then continue with step A8.

NOTE

The remainder of this procedure is intended for instruments which do not have a CCD Reference Label and for instruments with a label which cannot be adjusted to meet specifications in step x, using voltages listed on label.

y. Mechanically midrange CH 2 POSITION control.

z. Mechanically center adjustment R511 (Ch 2 Balance), R510 (Ch 2 Center) R111 (REF2+), and R110 (REF2–).

aa. **ADJUST**—Set CH 2 input coupling to AC and position two-division display to center screen with Ch 2 Center adjustment, R510.

bb. **ADJUST**—CH 2 Gain adjustment, R377, to set CURSORS readout to read ΔV=40mV, within one millivolt.

cc. Connect the test oscilloscope probe to test point TP680.

dd. Note exact amplitude display on test oscilloscope.

ee. **ADJUST**—With CH 2 POSITION control, move two-division display up three divisions and note exact amplitude on test oscilloscope. Then with CH 2 POSITION control, move display six divisions down and note exact amplitude on test oscilloscope; if test oscilloscope amplitude varies less than 5 millivolts when display is positioned between the top and bottom of the graticule, proceed to part kk. If test oscilloscope amplitude varies more than five millivolts, continue with the following; from two amplitudes previously noted, determine whether lowest amplitude was at top or bottom of graticule, then position 7D20 display to that position. Adjust REF2+ adjustment, R111, to move 7D20 display one minor division, for every 5 millivolts difference in amplitude, toward center of graticule.

ff. Set CH 2 input coupling to GND.

gg. Mechanically center CH 2 POSITION control, and connect shorting strap between ground and TP1230.

hh. **ADJUST**—Ch 2 Center adjustment, R510, for VZR=0, then remove shorting strap from TP1230.

ii. Set CH 2 Input coupling to AC.

jj. **INTERACTION**—Repeat step ee.

kk. Connect the test oscilloscope probe to test point TP481 (REF2–).

ll. With CH 2 POSITION, move two-division display to center screen. Note exact amplitude of test oscilloscope display.

mm. **ADJUST**—With CH 2 POSITION control, move two division display up three divisions and note exact amplitude on test oscilloscope. Then move 7D20 display six divisions down and note exact amplitude on test oscilloscope; if test oscilloscope amplitude varies less than five millivolts when display is positioned between top and bottom of graticule, proceed to part ss. If test oscilloscope amplitude varies more than five millivolts continue with following.

From the two amplitudes previously noted, determine whether lowest amplitude was at top or bottom of graticule, then position 7D20 display to that position. Adjust REF2– adjustment, R110, to move 7D20 display one minor division, for every 5 millivolts difference in amplitude, toward the center of the graticule.

nn. Set CH 2 input coupling to GND.

oo. Mechanically midrange CH 2 POSITION control.

pp. **ADJUST**—CH 2 Center adjustment, R510, for VZR=0.

qq. Set CH 2 input coupling to AC.

rr. **INTERACTION**—Repeat step mm.

ss. If criteria of part mm has been met, perform parts a through s and ignore remainder of this step.

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A8. ADJUST 5 mV GAIN AND POSITION GAIN (R820, R850, R751, R821, R851)

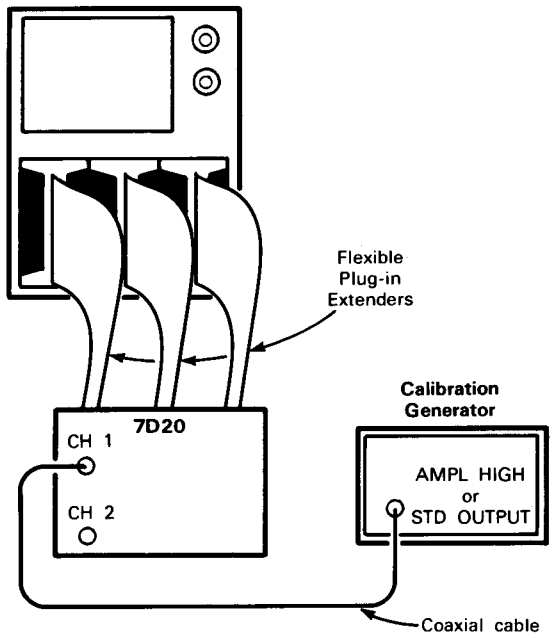
NOTE

If the preceding step was not performed, first perform step A1, then proceed.

a. Perform A2 Initialization Procedure, then proceed.

A8. SETUP CONDITIONS

7D20 Controls:
CH 1 VOLTS/DIV ..... 10 mV
TIME/DIV ..... 200 μs
CURSORS ΔON ..... ON (pushbuttons illuminated)
TRIGGERING COUPLING ..... HF REJ



Test Equipment Controls:
Calibration Generator
Mode ..... STD AMPL
Amplitude ..... 50 mV

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b. With CH 1 POSITION control, move display to center screen, and set CURSORS one 1 and 2 as shown in Figure 4-8 (except for TIME/DIV, should remain at 200 microseconds).

c. Press SET N pushbutton and observe readout; release SET N pushbutton when readout reads SET N=16, then press AVE pushbutton.

d. Set CH 1 AQR GAIN for ΔV=50.0mV.

e. Set CH 1 VOLTS/DIV to 5mV.

f. Set calibration generator to 20 millivolts.

g. **EXAMINE**—CURSORS readout reads ΔV=20mV, within 0.2 millivolt.

h. **ADJUST**—Ch 1 5 mV Gain adjustment, R820, so that CURSORS readout reads ΔV=20.0mV.

i. Set AQR MODE to CH 2.

j. Move coaxial cable from CH 1 input to CH 2 input.

k. Set calibration generation Amplitude to 50 millivolts and CH 2 VOLTS/DIV to 10mV.

l. Set CH 2 AQR GAIN for ΔV=50.0mV.

m. Set CH 2 VOLTS/DIV to 5mV and calibration generator Amplitude to 20 millivolts.

n. **EXAMINE**—CURSORS readout reads ΔV=20mV, within 0.2 millivolt.

o. **ADJUST**—CH 2, 5 mV Gain adjustment, R850, so that CURSORS readout reads ΔV=20mV.

p. Press *f* (function) pushbutton, then press MENU/TEST pushbutton. Set AQR MODE to CH 1.

q. From TEST MENU list displayed on oscilloscope mainframe, select CALIBRATION by pressing MEMORY DISPLAY pushbutton number 2.

r. From CALIBRATION list displayed on oscilloscope mainframe crt, select POSITION OFFSET by pressing MEMORY DISPLAY pushbutton number 3.

s. **EXAMINE**—Displayed trace is within 0.08 division of center graticule line.

t. **ADJUST**—CH 1, Centering adjustment, R410, to align displayed trace with center graticule line.

u. Set AQR MODE to CH 2.

v. **EXAMINE**—Displayed trace is within 0.08 divisions of center graticule line.

w. **ADJUST**—CH 2, Centering adjustment, R510, to align displayed trace with center graticule line.

x. From CALIBRATION list displayed on oscilloscope mainframe crt, select POSITION GAIN by pressing MEMORY DISPLAY pushbutton number 4.

y. **EXAMINE**—Displayed trace is three divisions above center graticule line, within 0.12 divisions.

z. **ADJUST**—CH 1, Position Gain adjustment, R821, to align displayed trace with third graticule line above center graticule line.

aa. Set AQR MODE to CH 2.

bb. **EXAMINE**—Displayed trace is three divisions above center graticule line, within 0.12 division.

cc. **ADJUST**—CH 2, Position Gain adjustment, R851, to align displayed trace with third graticule line above center graticule line.

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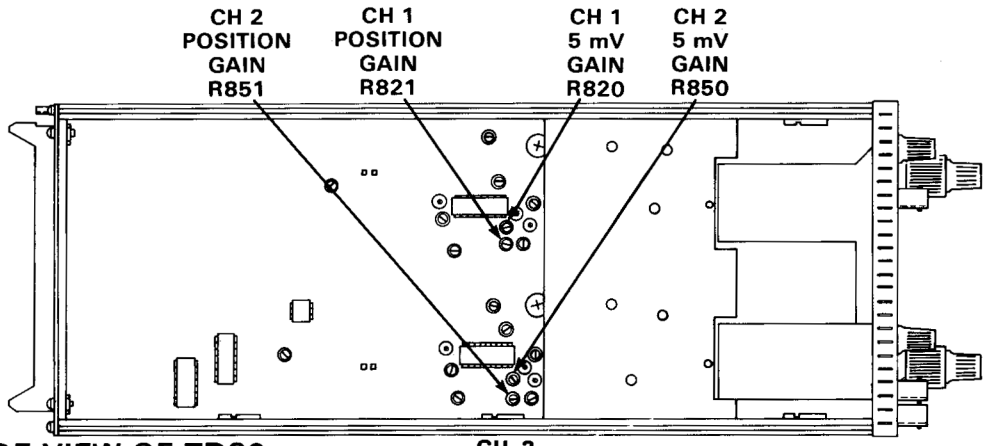
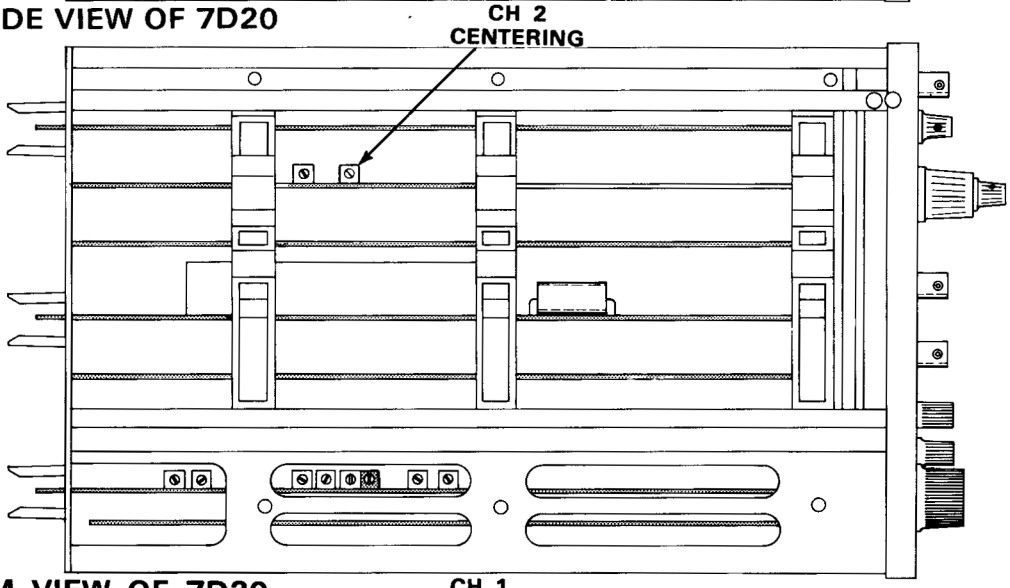
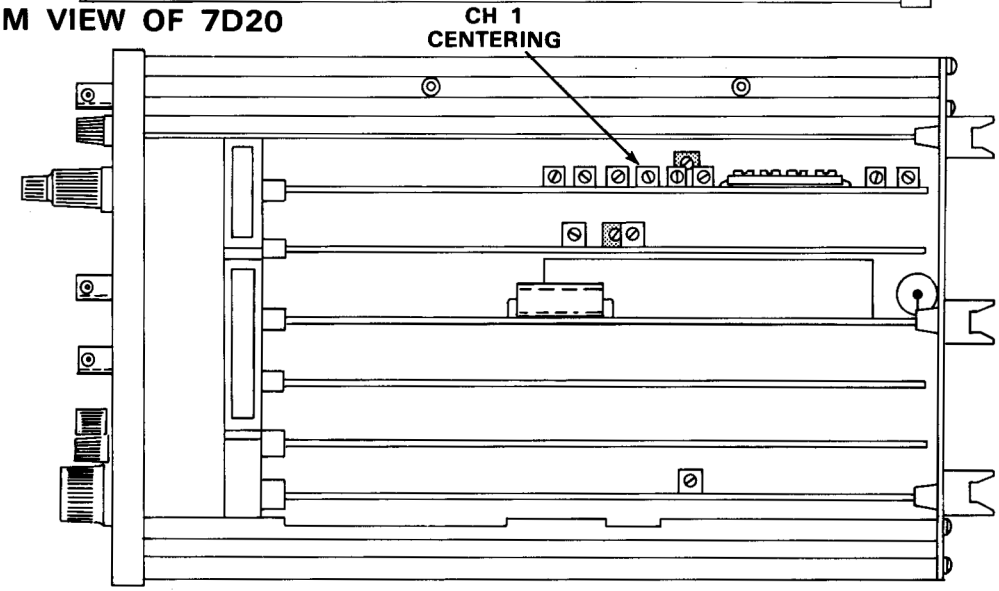
A8. ADJUSTMENT LOCATIONS



LEFT SIDE VIEW OF 7D20



BOTTOM VIEW OF 7D20



TOP VIEW OF 7D20

3858-413

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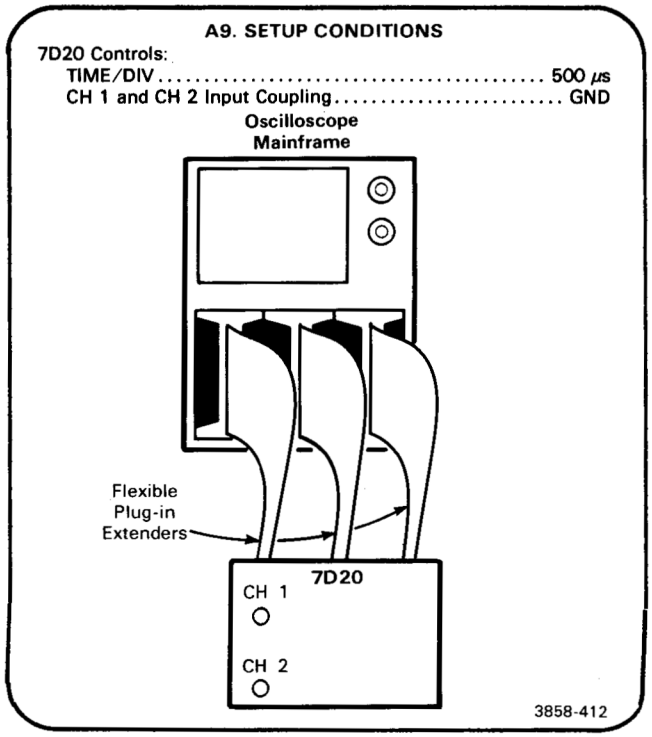
A9. ADJUST BASELINE SHIFT (R210D, R210C, R210B, R210A)

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

a. Perform A2 Initialization Procedure, then proceed.



b. With CH 1 POSITION control, set VZR=0.0.

c. **EXAMINE**—For less than 0.2 division trace shift while switching TIME/DIV from 500μS to 200μS.

d. **ADJUST**—Ch 1, ERD adjustment, R210D, for no trace shift when TIME/DIV switch is changed from 500μS to 200μs.

e. **EXAMINE**—For less than 0.2 division trace shift when switching TIME/DIV switch from 2μS to 1μS.

f. **ADJUST**—Ch 1, ETD adjustment, R210C, for no trace shift when switching TIME/DIV switch from 2μS to 1μS.

g. Set AQR MODE to CH 2.

h. With CH 2 POSITION control, set VZR=0.0.

i. Set TIME/DIV to 500μS.

j. **EXAMINE**—For less than 0.2 division trace shift while switching TIME/DIV switch from 500μS to 200μS.

k. **ADJUST**—Ch 2, ERD adjustment, R210B, for no trace shift when switching TIME/DIV from 500μS to 200μS.

l. **EXAMINE**—For less than 0.2 division trace shift when switching TIME/DIV switch from 2μS to 1μS.

m. **ADJUST**—Ch 2, ETD adjustment, R210A, for no trace shift when switching TIME/DIV switch from 2μS to 1μS.

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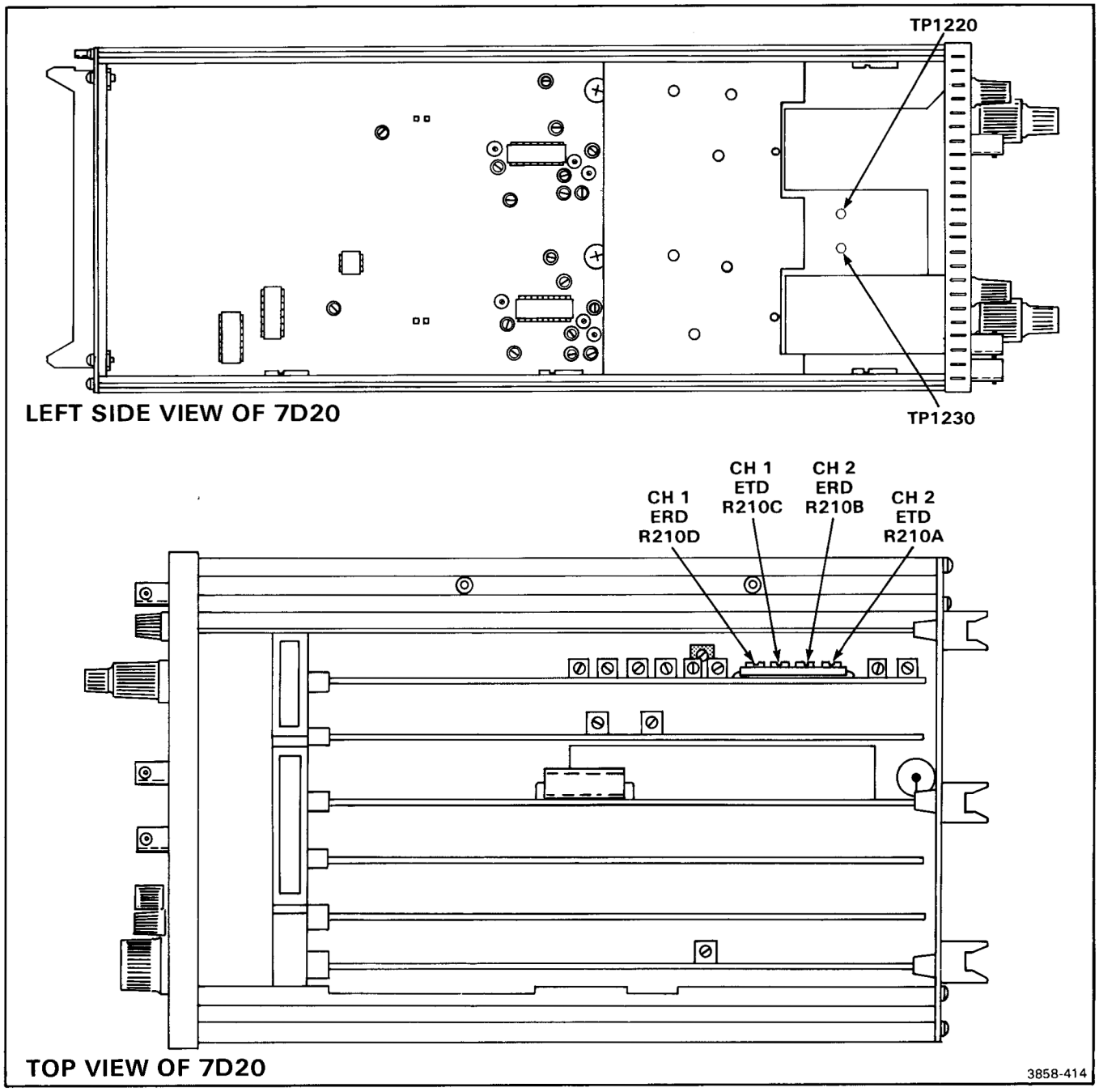
A9. TEST POINT & ADJUSTMENT LOCATIONS



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B. TRIGGER

Equipment Required (Numbers correspond to those listed in Table 4-3, Test Equipment).

1. Oscilloscope Mainframe
3. Digital Multimeter (DMM)
4. Calibration Generator
6. Function Generator
10. Flexible Plug-In Extender (three required)
11. Coaxial Cable (two required)
12. 50-ohm Terminator
16. Alignment Tool

B1. PRELIMINARY SETUP

a. Perform the Adjustment Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and the change Information at the rear of the manual for any modifications which may affect this procedure.

c. Set the 7D20 controls:
HORIZ POSITION .. Fully clockwise (In detent)
CH 1 VARIABLE ..... CAL (In detent)
CH 1 POSITION ..... Midrange
CH 2 VARIABLE ..... CAL (In detent)
CH 2 POSITION ..... Midrange

d. Set the Oscilloscope Mainframe controls:
Power ..... On
Vertical Mode..... Left
Intensity ..... Visible Display
Focus..... Well defined display
Trigger Source..... Left

e. Press MENU (pushbutton will light). If MASTER MENU is not displayed, press MEMORY DISPLAY number 6. From MASTER MENU list displayed on oscilloscope mainframe crt, select DISPLAY CAL PATTERN by pressing MEMORY DISPLAY pushbutton number 3.

f. While observing the DISPLAY CAL PATTERN displayed on the oscilloscope mainframe crt, set VERT GAIN, VERT CTR, HORIZ GAIN and HORIZ CTR adjustments to place corner markers of displayed adjustment pattern on center 6 × 8 divisions of graticule, as shown in Figure 4-9.

g. Set front-panel VECT LIN adjustment for minimum trace separation of diagonal lines on DISPLAY CAL PATTERN as shown in Figure 4-9.

h. To turn off DISPLAY CAL PATTERN, press MENU.

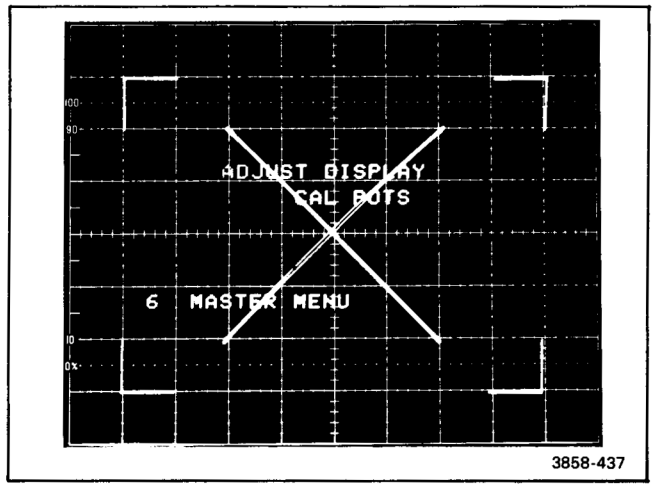

Figure 4-9. Display Adjust Pattern.

B2. INITIALIZATION PROCEDURE

a. Press MENU (pushbutton will light).

b. If MASTER MENU is not displayed, press MEMORY DISPLAY pushbutton number 6.

c. From MASTER MENU list, select UTILITIES by pressing MEMORY DISPLAY pushbutton number 4.

d. From displayed UTILITIES list select INIT FRONT PANEL by pressing MEMORY DISPLAY pushbutton number 5.

e. To return to MASTER MENU display, press MEMORY DISPLAY pushbutton number 6. To turn off MASTER MENU display, press MENU pushbutton.

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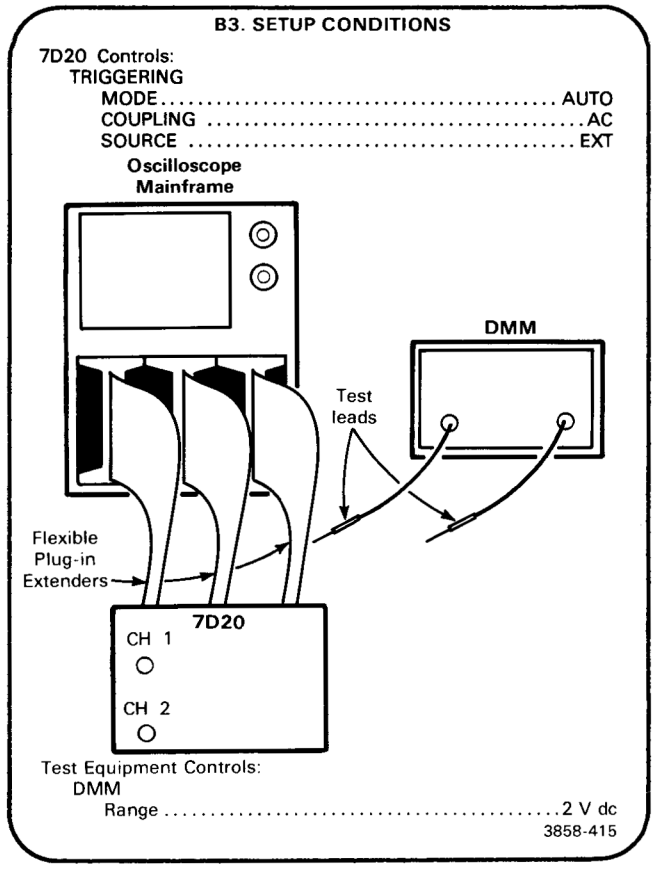
B3. ADJUST TRIGGER OFFSET, DC BALANCE, AND AC ZERO (R518, R445, R240 AND R241)

NOTE

First perform step B1, then proceed.

a. Perform step B2. Initialization Procedure.



b. Connect DMM test leads between TP902 and TP810.

c. **EXAMINE**—DMM should read zero volts, within 2 millivolts.

d. **ADJUST**—AC Zero adjustment, R241, for a DMM reading of zero volts, within 2 millivolts.

e. Set TRIGGERING COUPLING to DC.

f. **EXAMINE**—DMM should read zero volts, within 2 millivolts.

g. **ADJUST**—DC Balance adjustment, R240, for a DMM reading of zero volts, within 2 millivolts.

h. Mechanically center CH 1 and CH 2 POSITION controls.

i. Connect a shorting strap between TP1220 and GND.

j. Connect DMM test leads between TP902 and J400.

k. **EXAMINE**—DMM should read zero volts, within 2 millivolts.

l. **ADJUST**—CH 1 TRIGGER OFFSET adjustment, R518, for DMM reading of zero volts, within 2 millivolts.

m. Connect shorting strap between TP1230 and GND.

n. Connect DMM test leads between TP902 and J550.

o. **EXAMINE**—DMM should read zero volts, within 2 millivolts.

p. **ADJUST**—CH 2 TRIGGER OFFSET adjustment, R445, for a DMM reading of zero volts, within 2 millivolts.

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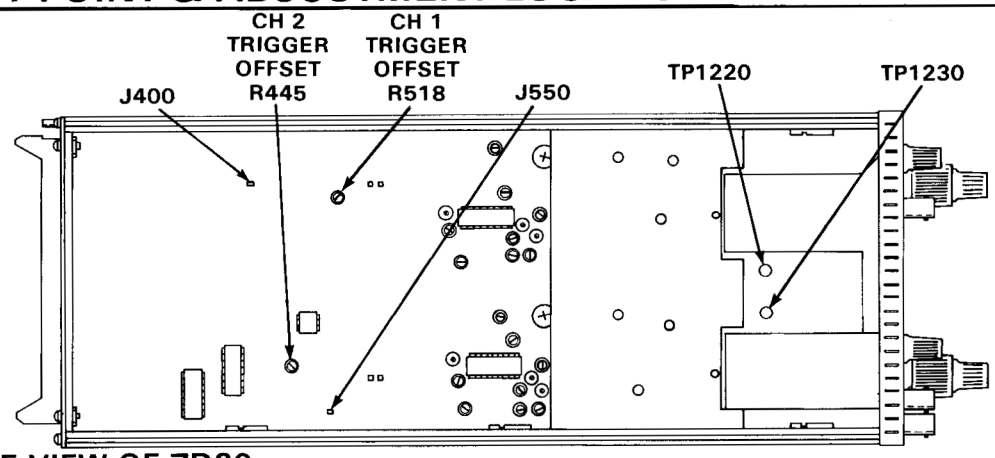
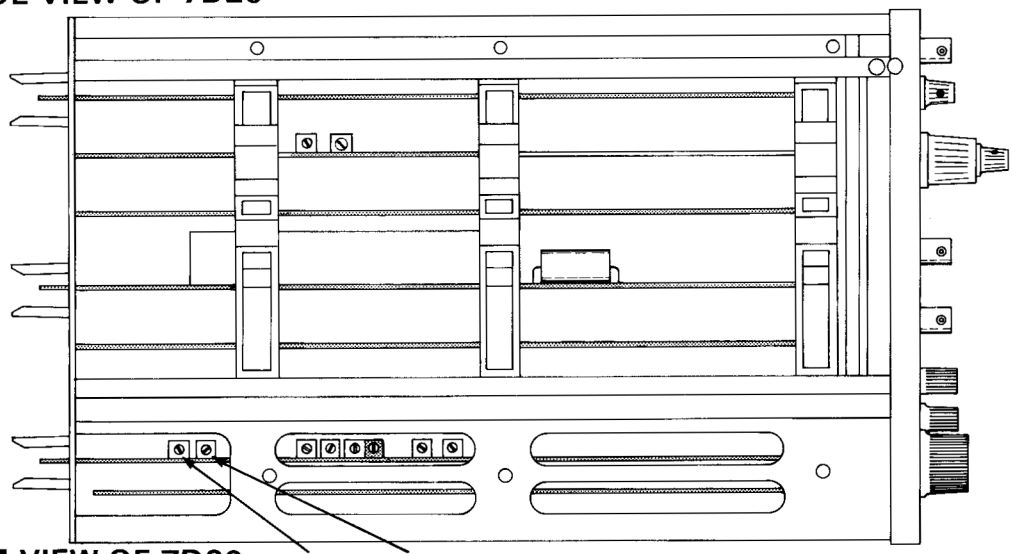
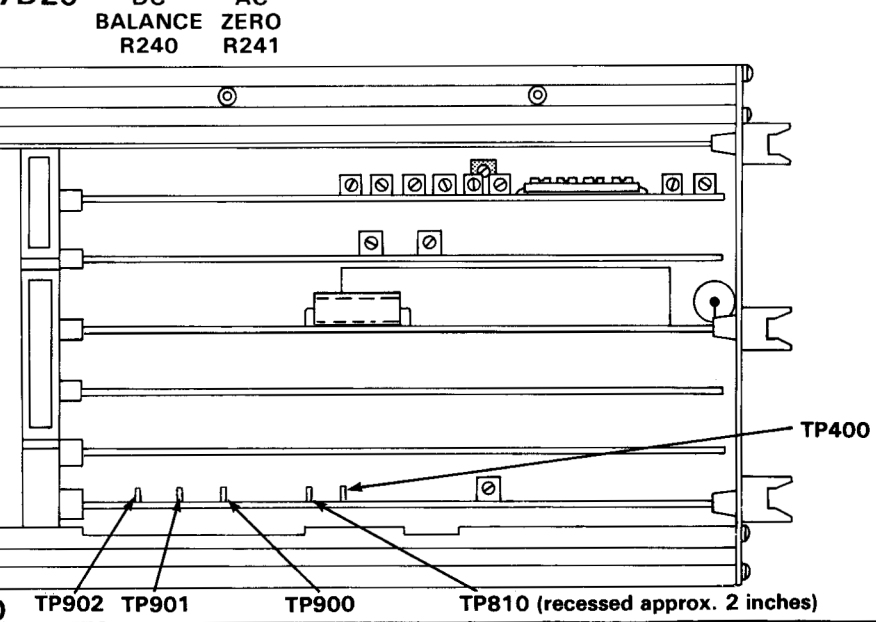
B3. TEST POINT & ADJUSTMENT LOCATIONS



LEFT SIDE VIEW OF 7D20



BOTTOM VIEW OF 7D20



TOP VIEW OF 7D20

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B4. ADJUST HYSTERESIS, SLOPE CENTER AND LEVEL CENTER (R444, R440, R543)

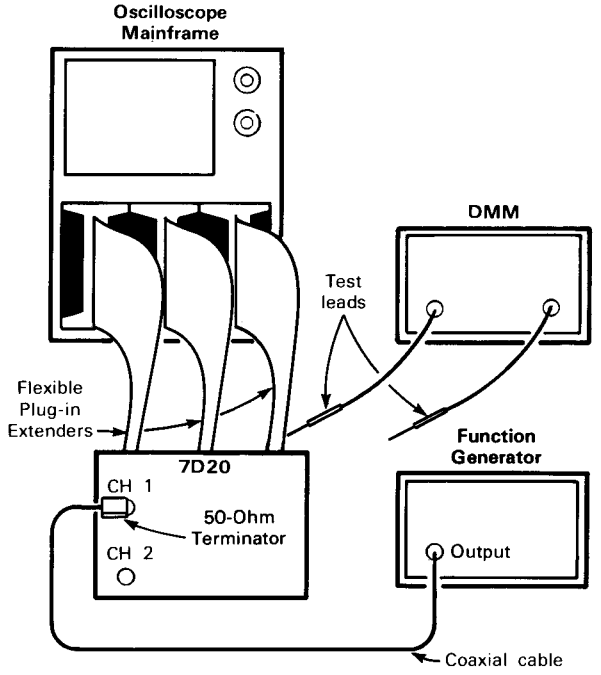
NOTE

If the preceding step was not performed, first perform step B1, then proceed.

a. Perform step B2. Initialization Procedure.

B4. SETUP CONDITIONS

7D20 Controls:
- CH 1 VOLTS/DIV ..... 100 mV
- CH 1 Input Coupling ..... DC
- TIME/DIV ..... 20 µs
- TRIGGERING
  - MODE ..... AUTO
  - COUPLING ..... AC HF REJ



Test Equipment Controls:
- Function Generator
  - Frequency ..... 30 KHz
  - Function ..... Sine Wave
- DMM
  - Range ..... 2 V dc

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b. Set function generator Amplitude control to display seven divisions of 30 kilohertz sine-wave signal.

c. Set CH I VOLTS/DIV to 2V.

d. **EXAMINE**—Stable triggering can be obtained with TRIGGERING LEVEL control.

e. **ADJUST**—Hysteresis adjustment, R444, so that stable triggering can be obtained with TRIGGERING LEVEL control.

f. Set CH 1 VOLTS/DIV to 5V.

g. **EXAMINE**—Displayed sine-wave signal should not be triggerable with TRIGGERING LEVEL control.

h. **ADJUST**—Hysteresis adjustment, R444, so that stable triggering can not be obtained with CH 1 VOLTS/DIV is set to 5V, and can be obtained with CH 1 VOLTS/DIV set to 2V.

i. Set TRIGGERING COUPLING to AC.

j. Set TIME/DIV control to 1mS.

k. Set CH 1 VOLTS/DIV to 500mV.

l. Set function generator frequency to one kilohertz.

m. Set TRIGGERING LEVEL control for stable triggering of displayed one-kilohertz signal.

n. Set CURSORS 1 for T=0.0S.

o. **EXAMINE**—While switching between + and - SLOPE observe that cursors dot does not move more than + or - 0.04 division vertically (-SLOPE is obtained when +SLOPE pushbutton is not lighted).

p. **ADJUST**—Slope Center adjustment, R440, so that while switching between + and - SLOPE cursors dot does not move vertically more than 0.04 divisions.

q. Set CH 1 input coupling to GND.

r. Connect DMM minus test lead to TP900 (GND) and plus test lead to TP400.

s. Set TRIGGERING LEVEL control for DMM reading of -1.28 volts, within 10 millivolts.

NOTE

Take care not to disturb TRIGGERING LEVEL setting throughout remainder of this step.

t. Set CH 1 VOLTS/DIV to 1V, and CH 1 input coupling to AC (out of HF REJ).

u. Set function generator Amplitude control to display two divisions of one kilohertz signal.

v. With CH 1 POSITION control, vertically center displayed two division signal exactly on oscilloscope mainframe crt.

w. **EXAMINE**—Displayed CURSORS dot is within 0.08 division of center graticule line.

x. **ADJUST**—Level Center adjustment, R543, so that trigger point (CURSORS 1 dot) is within 0.08 division of center graticule line.

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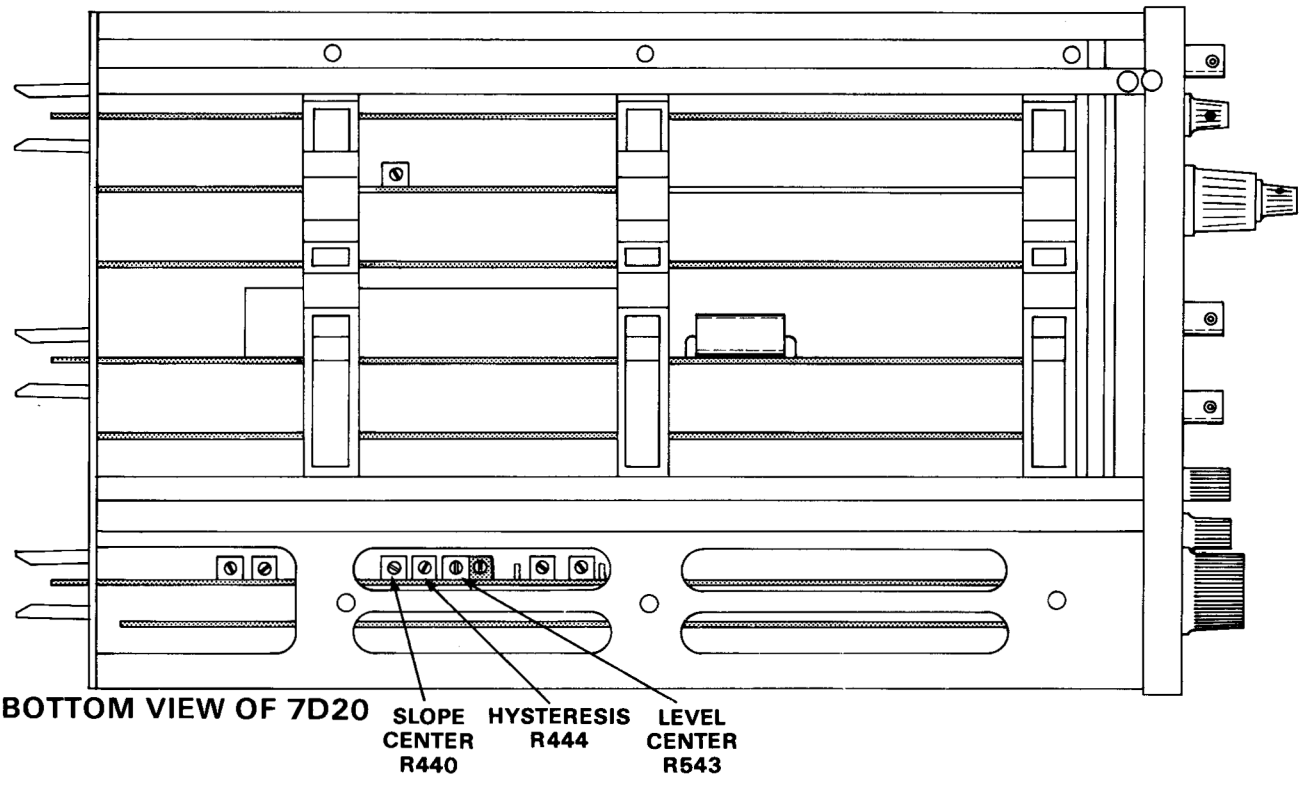
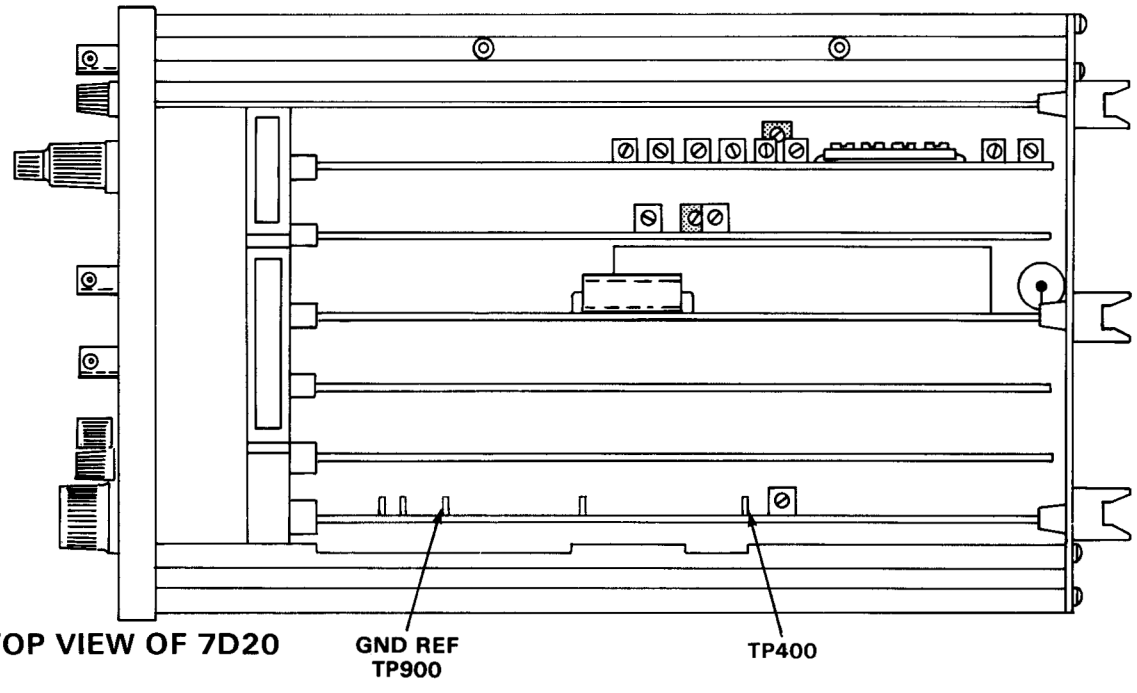
B4. TEST POINT & ADJUSTMENT LOCATIONS





J858-419

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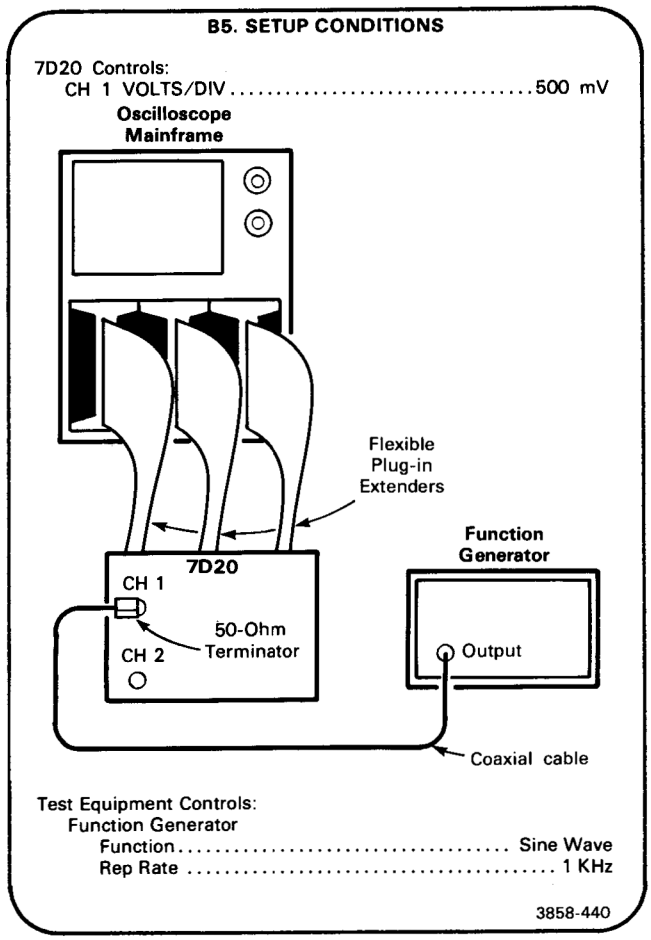
B5. ADJUST P-P RANGE, PLUS PEAK OFFSET, AND MINUS PEAK OFFSET (R541, R546, R645)

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

a. Perform B2 Initialization Procedure.



b. Set function generator to display six divisions of one kilohertz signal on oscilloscope mainframe crt.

c. Set TRIGGERING MODE to P-P and TRIGGERING LEVEL control fully clockwise.

d. Set CURSORS 1 to T=0.0S.

e. **EXAMINE**—Triggering point (displayed cursor dot) is between 0.8 and 1.2 divisions below positive sine-wave peak.

f. **ADJUST**—P-P RANGE adjustment, R541, so that triggered point falls between 0.8 and 1.2 divisions below sine-wave positive peak.

g. Rotate TRIGGERING LEVEL control fully counter clockwise and set +SLOPE to minus (+SLOPE pushbutton not lighted).

h. **EXAMINE**—Triggering point is between 0.8 and 1.2 divisions above negative sine-wave peak.

i. **ADJUST**—Compromise P-P RANGE adjustment, R541, to meet requirements of steps e and h.

j. Set TRIGGERING MODE to AUTO with +SLOPE.

k. Connect DMM negative test lead to GND REF and positive test lead to TP400.

l. Set TRIGGERING LEVEL control for a DMM reading of −1.28 volts, within 10 millivolts.

m. Set CH 1 VOLTS/DIV to 1 V. Set function generator Amplitude control to display 0.4 divisions of one kilohertz signal displayed on oscilloscope mainframe crt.

n. **EXAMINE**—Displayed one kilohertz sine wave remains triggered while switching between AUTO +SLOPE, and AUTO −SLOPE without readjusting TRIGGERING LEVEL, if sine wave does not remain triggered, perform step B4.

o. **EXAMINE**—Displayed one kilohertz sine wave remains triggered while switching between P-P +SLOPE and P-P −SLOPE without readjusting TRIGGERING LEVEL.

NOTE

If requirements of part p are met, ignore remainder of this step.

p. Set CH 1 input coupling to GND.

q. Set TRIGGERING MODE to AUTO AC with +SLOPE.

r. Connect DMM negative test lead to GND REF and positive test lead to TP400.

s. Set TRIGGERING LEVEL control for DMM reading of −1.28 volts, within 10 millivolts.

t. Move DMM positive test lead to TP540.

u. **ADJUST**—Plus Peak Offset adjustment, R546, for a DMM reading of +10 millivolts.

v. Move DMM positive test lead to TP640.

w. **ADJUST**—Minus Peak Offset adjustment, R645, for a DMM reading of 10 millivolts.

x. Set CH 1 input coupling to AC.

y. **EXAMINE**—Repeat part o; if requirements of part o cannot be met, perform following procedure. Observe direction trigger point moves when switching from AUTO +SLOPE to P-P +SLOPE; if triggering point moves up, subtract 10 millivolts from DMM reading called for in part v and add 10 millivolts to DMM reading called for in part x. If trigger point goes down, add 10 millivolts to DMM reading called for in part v and subtract 10 millivolts from DMM reading called for in part x. This procedure may be repeated again.

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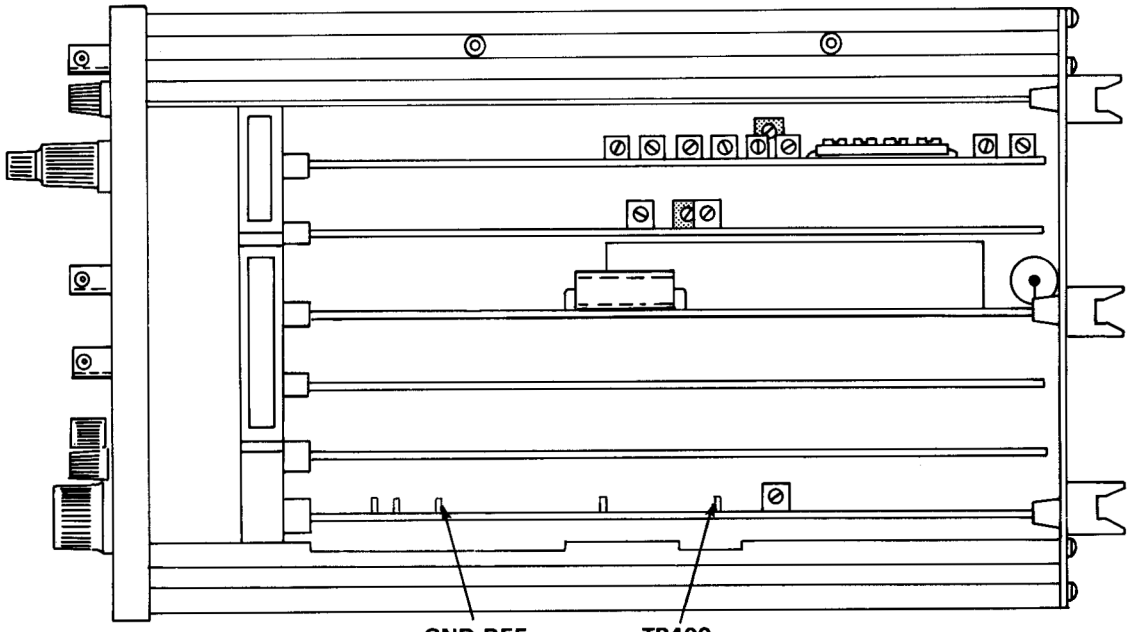
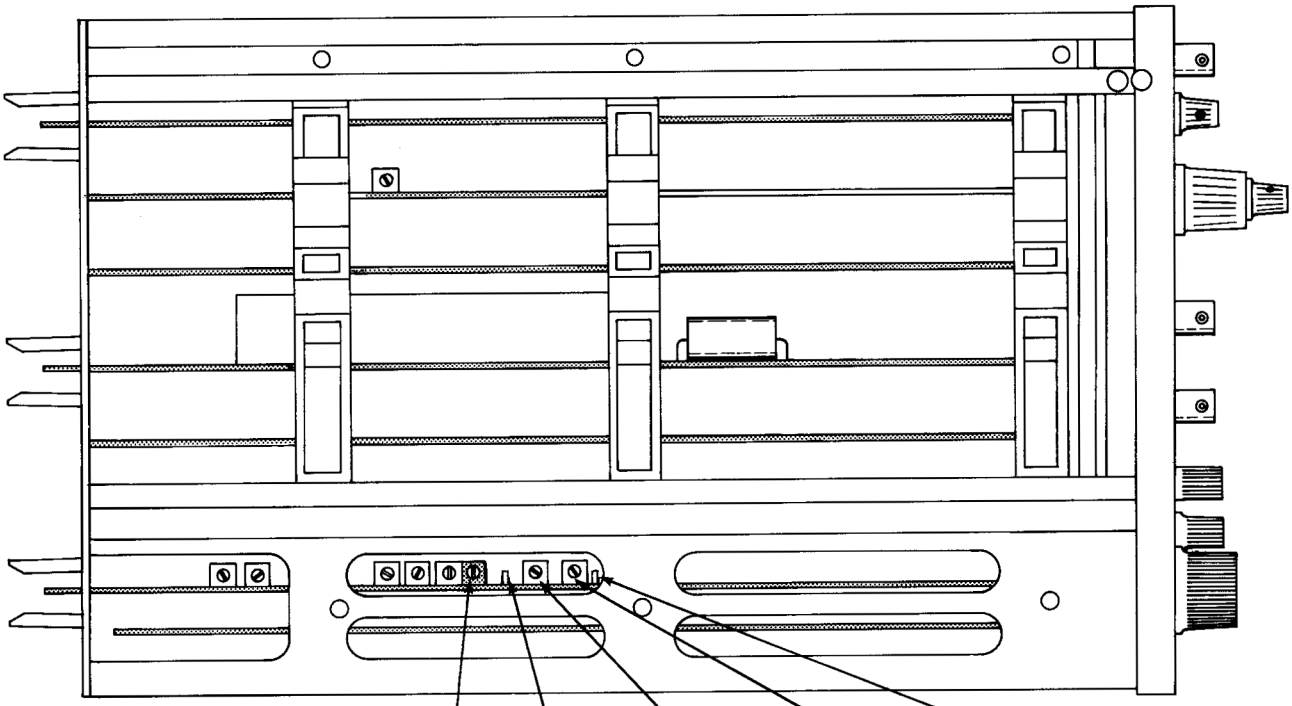
B5. TEST POINT AND ADJUSTMENT LOCATIONS



TOP VIEW OF 7D20



BOTTOM VIEW OF 7D20

3858-441

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C. TIMING AND STEP RESPONSE

Equipment Required (Numbers correspond to those listed in Table 4-3, Test Equipment).

1. Oscilloscope Mainframe
2. Test Oscilloscope
3. Digital Multimeter (DMM)
4. Calibration Generator
9. Cable
10. Flexible Plug-In Extender (three required)
11. Coaxial Cable (two required)
12. 50-ohm Terminator
13. 2X Attenuator
14. 10X Attenuator
16. Alignment Tool

C1. PRELIMINARY SETUP

a. Perform the Adjustment Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and the change information at the rear of the manual for any modifications which may affect this procedure.

c. Set the Oscilloscope Mainframe controls:
Power ..... On
Vertical Mode ..... Left
Intensity ..... Visible Display
Focus ..... Well defined display

d. Set the 7D20 controls:
HORIZ POSITION .. Fully clockwise (In detent)
CH 1 VARIABLE ..... CAL (In detent)
CH 1 POSITION ..... Midrange
CH 2 VARIABLE ..... CAL (In detent)
CH 2 POSITION ..... Midrange

e. Press MENU (pushbutton will light). If MASTER MENU is not displayed press MEMORY DISPLAY pushbutton number 6. From the MASTER MENU list displayed on the oscilloscope mainframe crt, select DISPLAY CAL PATTERN by pressing MEMORY DISPLAY pushbutton number 3.

f. While observing the DISPLAY CAL PATTERN displayed on the oscilloscope mainframe crt, use screwdriver to set VERT GAIN, VERT CTR, HORIZ GAIN and HORIZ CTR controls to place corner markers of DISPLAY CAL PATTERN on center 6 × 8 divisions of graticule, as shown in Figure 4-10.

g. Set VECT LIN adjustment for minimum trace separation of the diagonal lines on DISPLAY CAL PATTERN as shown in Figure 4-10.

h. To return to MASTER MENU, press MEMORY DISPLAY pushbutton number 6. To turn off MASTER MENU display press MENU.

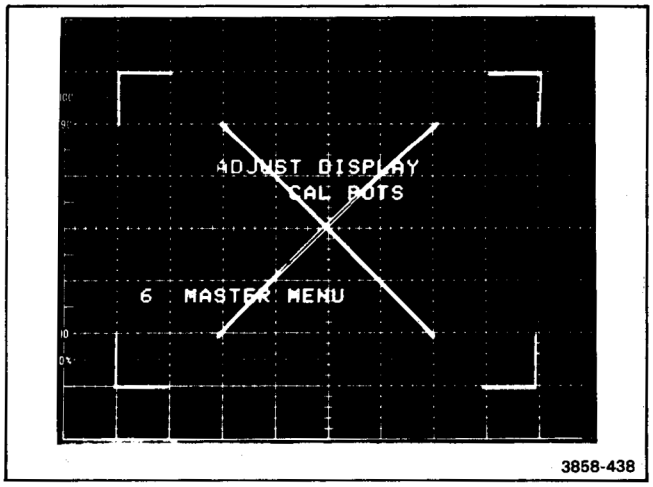

Figure 4-10. Display Adjust Pattern.

C2. INITIALIZATION PROCEDURE

a. Press MENU (pushbutton will light).

b. If MASTER MENU is not displayed, press MEMORY pushbutton number 6.

c. From displayed MASTER MENU list, select UTILITIES by pressing MEMORY DISPLAY pushbutton number 4.

d. From displayed UTILITIES list select INIT FRONT PANEL by pressing MEMORY DISPLAY pushbutton number 5.

e. To return to MASTER MENU, press MEMORY DISPLAY pushbutton number 6. To turn off MASTER MENU display press MENU.

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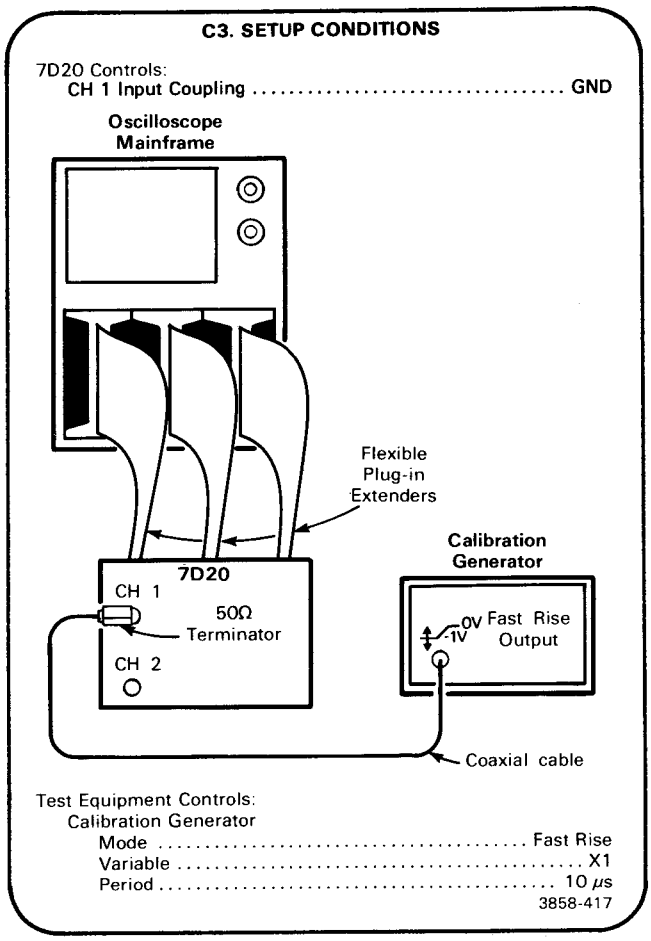
C3. ADJUST FAST RAMP GAIN AND OFFSET (R320, R732)

NOTE

The preceding step (B. TRIGGER) should be performed in its entirety prior to performing this step.

a. Perform step C2. Initialization Procedure.



b. Mechanically center TRIGGERING LEVEL knob.

NOTE

Do not disturb the setting of the TRIGGERING LEVEL knob throughout the remainder of this step.

c. Press *f* (function) then press MENU/TEST.

d. If TEST MENU is not displayed, press MEMORY DISPLAY pushbutton number 6.

e. From displayed TEST MENU, select CALIBRATION by pressing MEMORY DISPLAY number 2.

f. From displayed CALIBRATION menu select FAST RAMP GAIN/COUNT by pressing MEMORY DISPLAY number 1.

g. **EXAMINE**—Gain (see Fig. 4-11) is within limits of 99.7 to 100.3.

h. ADJUST—Ramp Gain adjustment, R320, so that GAIN reads 100.0.

i. Press MEMORY DISPLAY pushbutton number 6. Press *f* then TEST.

j. Set TIME/DIV to 2μS.

k. Set CH 1 VOLTS/DIV to 100 mV and Input Coupling to AC.

l. Set calibration generator Amplitude control and CH 1 POSITION control to display a six-division signal centered vertically and horizontally on the graticule.

m. Set TIME/DIV to 50 nS.

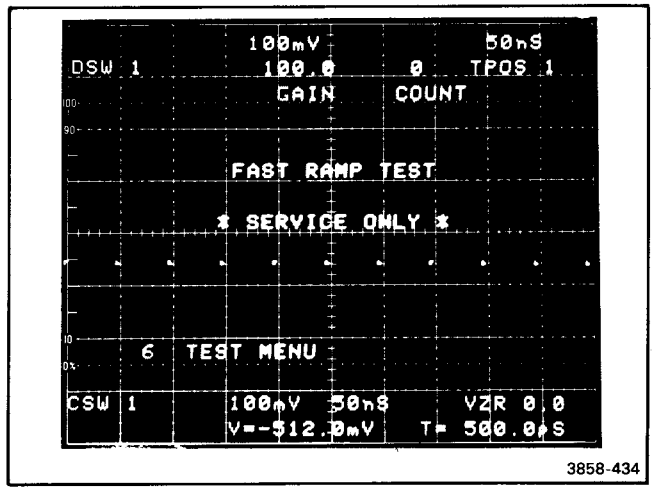


Figure 4-11. Gain Count readout.

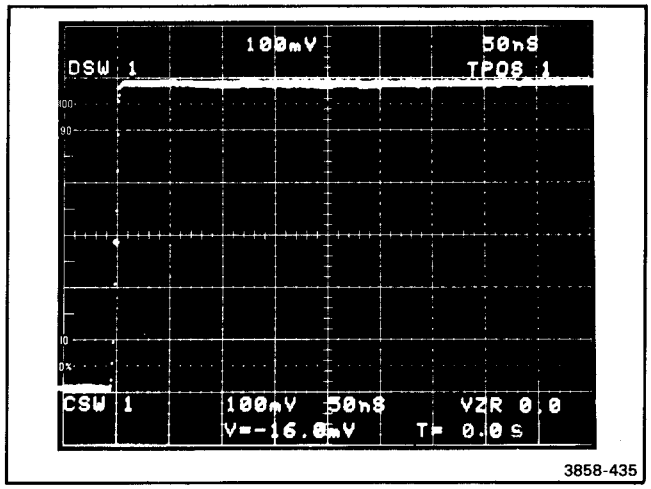


Figure 4-12. Fast Ramp Offset adjustment.

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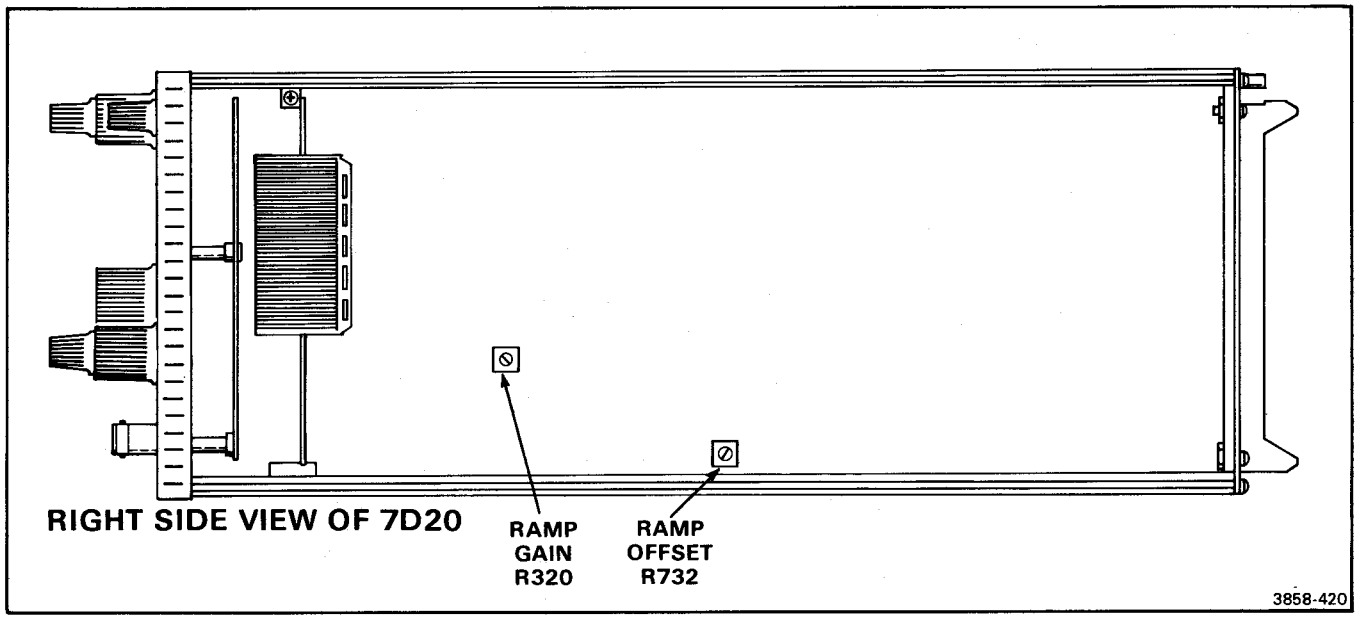
C3. ADJUSTMENT LOCATIONS



n. Set TRIG POS to read TPOS 1 (see Fig. 4-12).

o. Set CURSORS "1" to read T=0.0S (see Fig. 4-12).

p. Set TRIGGERING MODE to AUTO and COUPLING to DC.

q. **CHECK**—Displayed cursor dot is within two vertical divisions of center graticule line.

r. **ADJUST**—Ramp Offset adjustment, R732, so that displayed cursor dot is within one vertical division of center graticule line.

s. **INTERACTION**—Adjustment of Ramp Offset adjustment, R732, affects the setting of Ramp Gain adjustment, R320, repeat parts a through h.

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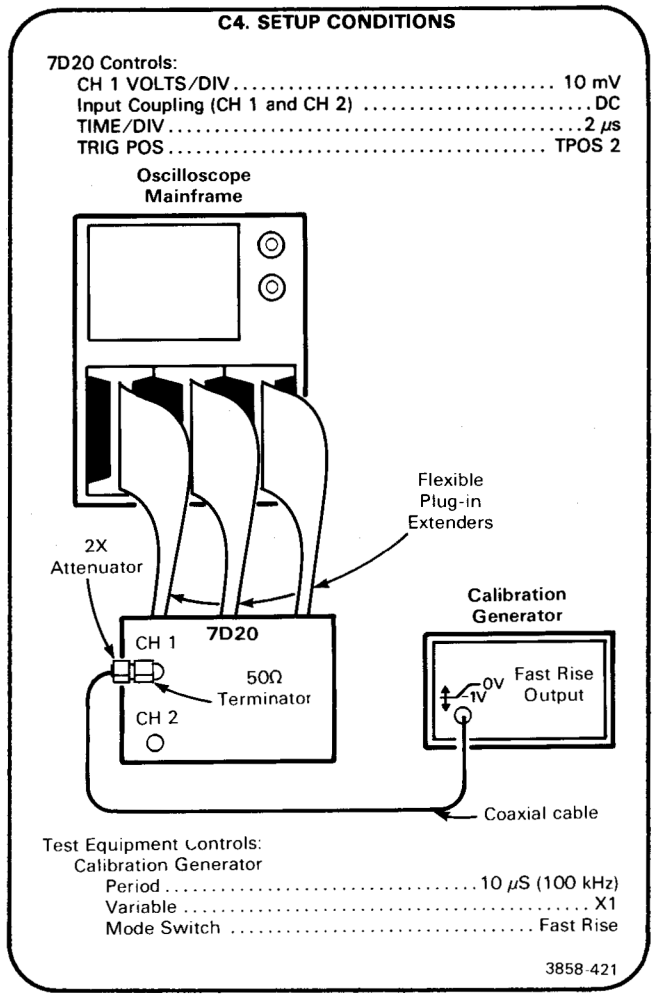
C4. ADJUST HIGH FREQUENCY STEP RESPONSE (R810, C813, R710, C710, C1020, C822, C820, C811, R840, C841, R750, C740, C913, C954, C1050, R852, C851, C850, *C421, *C486)

NOTE

The entire B. TRIGGER step and Step C3 should be performed before performing this step.

a. Perform step C2, Initialization Procedure, then proceed.



b. Set POSITION control and calibration generator Pulse Amplitude control for a six-division display centered on oscilloscope mainframe crt.

c. Set TIME/DIV control to 50nS.

d. **EXAMINE**—For optimum square corner and flat top on displayed pulse at 5, 10 and 100mV VOLTS/DIV settings within the following limits: Aberration in first 60 nanoseconds should not exceed 0.3 divisions peak-to-peak or 0.18 division above or below final step plateau. Aberrations after first 60 nanoseconds should not exceed 0.18 divisions peak-to-peak or 0.12 divisions above or below final step plateau.

***C421 and C486 are located on the A5—CCD board.**

e. **ADJUST**—CH 1 preamplifier compensations for optimum square corner and flat top, using VOLTS/DIV, TIME/DIV and Rep Rate settings, listed in Table 4-7. Set C421 on CCD Board for minimum step 50 ns after front corner.**

f. Set CH 1 VOLTS/DIV to 50mV and TIME/DIV to 10μS.

g. Set CH 1 VOLTS/DIV to 500mV and TIME/DIV to 10μS.

h. Connect High Ampl Output from calibration generator to CH 1 input through coaxial cable, and 50-ohm Terminator.

i. Set calibration generator mode switch to High Ampl, and Rep Rate to 10 kHz.

j. Set POSITION control and calibration generator Amplitude control for a six-division display centered on oscilloscope mainframe crt.

k. **EXAMINE**—Displayed waveform for flat top, within 0.08 division.

l. **ADJUST**—Comp 1 adjustment C1011 for optimum flat top on displayed waveform.

TABLE 4-7
CH 1 High Frequency Adjustments

VOLTS/DIV	TIME/DIV	REP RATE	ADJUSTMENT
10mV	200nS	100 kHz	Comp 9 (R810) Comp 8 (C813)
10mV	50nS, HMAG	1 MHz	Comp 10 (R710) Comp 11 (C710) Comp 2 (C1020)
5mV	50nS, HMAG	1 MHz	Comp 5 (R822) Comp 6 (C820) Comp 7 (C811)
20mV †50mV	50nS, HMAG	1 MHz	Comp 19 (C913)

m. Set AQR MODE to CH 2.

n. Connect Fast Rise output from calibration generator to CH 2 Input through coaxial cable, 2X Attenuator, and 50-ohm terminator.

o. Set calibration generator mode switch to Fast Rise.

p. Set CH 2 VOLTS/DIV to 10mV.

q. Set POSITION control and calibration generator Amplitude control for a six-division display centered on oscilloscope mainframe crt.

r. Set TIME/DIV control to 50nS.

****If P420 (CCD board) is in the storage position, do not adjust C421.**

†Preamp shield must be removed to make this adjustment.

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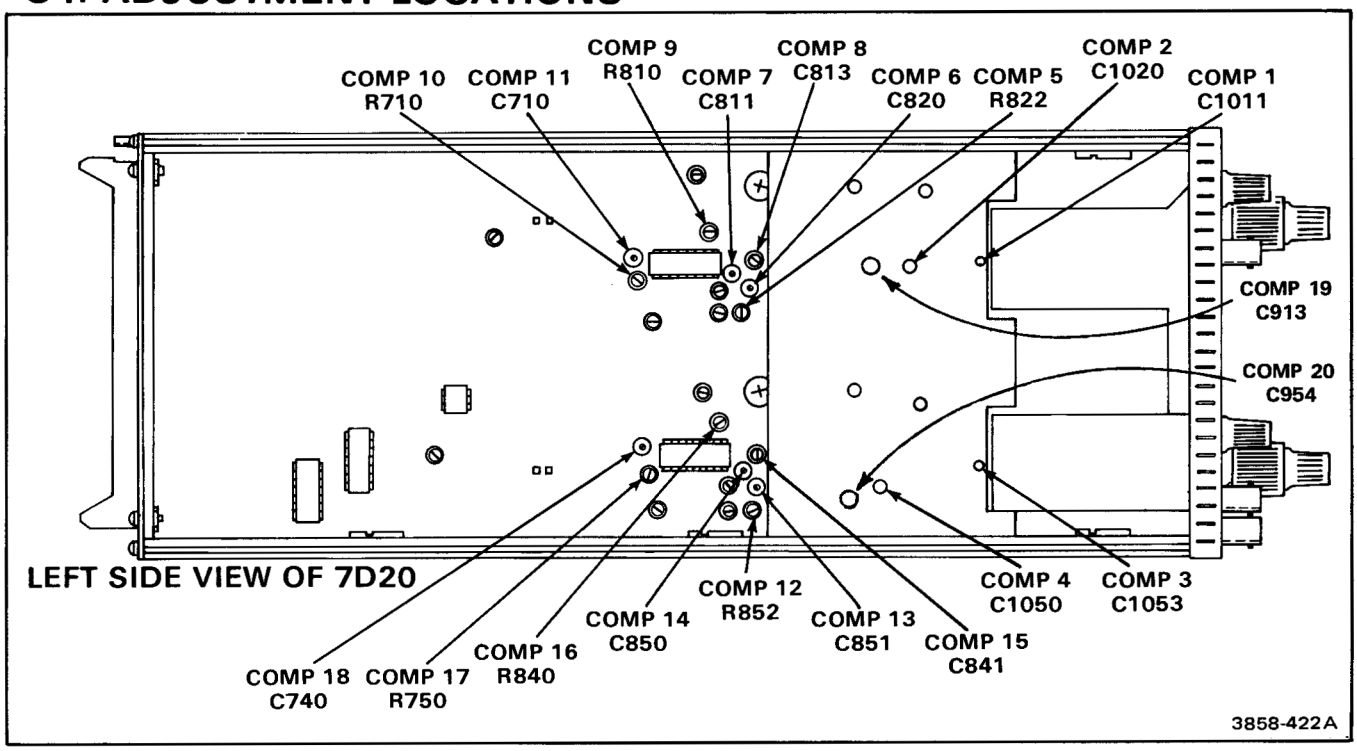
C4. ADJUSTMENT LOCATIONS



s. **EXAMINE**—For optimum square corner and flat top on displayed pulse at 5, 10 and 100mV VOLTS/DIV settings within the following limits: Aberration in first 60 nanoseconds should not exceed 0.3 divisions peak-to-peak or 0.18 division above or below final step plateau. Aberrations after first 60 nanoseconds should not exceed 0.18 divisions peak-to-peak or 0.12 divisions above or below final step plateau.

t. **ADJUST**—CH 2 preamplifier compensations for optimum square corner and flat top, using VOLTS/DIV, TIME/DIV and Rep Rate settings, listed in Table 4-8. Set C486 on CCD board for minimum step 50 ns after front corner.***

u. Set CH 2 VOLTS/DIV to 500mV and TIME/DIV to 10μS.

v. Connect High Ampl Output from calibration generator to CH 2 input through coaxial cable and 50-ohm Terminator.

w. Set calibration generator mode switch to High Amp and Rep Rate to 10 kHz.

x. Set CH 2 POSITION control and calibration generator amplitude control for a six-division display centered on oscilloscope mainframe crt.

TABLE 4-8
CH 2 High Frequency Adjustments

VOLTS/DIV	TIME/DIV	REP RATE	ADJUSTMENT
10mV	200nS	100 kHz	Comp 16 (R840) Comp 15 (C841)
10mV	50nS, HMAG	1 MHz	Comp 17 (R750) Comp 18 (C740) Comp 3 (C1050)
5mV	50nS, HMAG	1 MHz	Comp 12 (R852) Comp 13 (C851) Comp 14 (C850)
20mV †50mV	50nS, HMAG	1 MHz	Comp 20 (C954)

y. **EXAMINE**—Displayed waveform for flat top, within 0.08 division.

z. **ADJUST**—Comp 3 adjustment, C1053, for optimum flat top on displayed waveform.

***If P480 (CCD board) is in the storage position, do not adjust C486.

†Preamp shield must be removed to make this adjustment.

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INSTRUMENT OPTIONS

No options were available for the 7D20 at the time of this printing.

Information about any subsequent options will be included in the CHANGE INFORMATION section at the back of this manual.

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REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

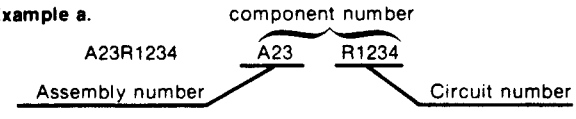
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

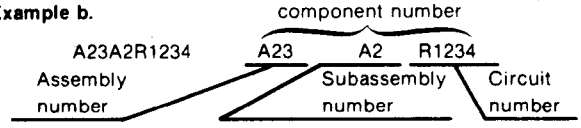
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

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CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P.O. BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01281	TRW ELECTRONIC COMPONENTS, SEMICONDUCTOR OPERATIONS	14520 AVIATION BLVD.	LAWNDALE,CA 90260
01295	TEXAS INSTRUMENTS, INC. SEMICONDUCTOR GROUP	P.O. BOX 5012	DALLAS, TX 75222
02735	RCA CORPORATION, SOLID STATE DIVISION	ROUTE 202	SOMERVILLE, NY 08876
03508	GENERAL ELECTRIC COMPANY, SEMI-CONDUCTOR PRODUCTS DEPARTMENT	ELECTRONICS PARK	SYRACUSE, NY 13201
03888	KDI PYROFILM CORPORATION	60 S JEFFERSON ROAD	WHIPPANY, NJ 07981
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
05828	GENERAL INSTRUMENT CORP ELECTRONIC SYSTEMS DIV.	600 W JOHN ST.	HICKSVILLE LI, NY 11802
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
07716	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, BURLINGTON DIV.	2850 MT. PLEASANT	BURLINGTON, IA 52601
11236	CTS OF BERNE, INC.	406 PARR RD.	BERNE, IN 46711
12697	CLAROSTAT MFG. CO., INC.	LOWER WASHINGTON STREET	DOVER, NH 03820
12969	UNITRODE CORPORATION	580 PLEASANT STREET	WATERTOWN, MA 02172
14193	CAL-R, INC.	1601 OLYMPIC BLVD.	SANTA MONICA, CA 90404
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
14552	MICRO SEMICONDUCTOR CORP.	2830 E FAIRVIEW ST.	SANTA ANA, CA 92704
15454	RODAN INDUSTRIES, INC.	2905 BLUE STAR ST.	ANAHEIM, CA 92806
15818	TELEDYNE SEMICONDUCTOR	1300 TERRA BELLA AVE.	MOUNTAIN VIEW, CA 94043
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
19701	ELECTRA-MIDLAND CORP., MEPCO ELECTRA INC.	P O BOX 760	MINERAL WELLS, TX 76067
20932	EMCON DIV OF ILLINOIS TOOL WORKS INC.	11620 SORRENTO VALLEY RD P O BOX 81542	SAN DIEGO, CA 92121
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
22929	DALE ELECTRONICS CORP FREQUENCY CONTROL GROUP	P.O. BOX 3164	TEMPE,AZ 85282
24546	CORNING GLASS WORKS, ELECTRONIC COMPONENTS DIVISION	550 HIGH STREET	BRADFORD, PA 16701
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
31433	UNION CARBIDE CORP ELECTRONICS DIV	PO BOX 5928	GREENVILLE, SC 29606
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
49956	RAYTHEON CO.	141 SPRING ST.	LEXINGTON, MA 02173
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
52763	STETTNER-TRUSH, INC.	67 ALBANY STREET	CAZENOVIA, NY 13035
53184	XCITON CORPORATION	5 HEMLOCK STREET	LATHAM, NY 12110
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
57668	R-OHM CORP.	16931 MILLIKEN AVE.	IRVINE, CA 92713
57924	BOURNS INC NETWORKS DIV 12155	MAGNOLIA AVE	RIVERSIDE, CA 92503
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
73899	JFD ELECTRONICS COMPONENTS CORP.	PINETREE ROAD	OXFORD, NC 27565
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
75378	CTS KNIGHTS, INC.	400 REIMANN AVE.	SANDWICH, IL 60548
76493	BELL INDUSTRIES, INC., MILLER, J. W., DIV.	19070 REYES AVE., P O BOX 5825	COMPTON, CA 90224
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
80031	ELECTRA-MIDLAND CORP., MEPCO DIV.	22 COLUMBIA ROAD	MORRISTOWN, NJ 07960
81483	INTERNATIONAL RECTIFIER CORP.	9220 SUNSET BLVD.	LOS ANGELES, CA 90069
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC.	3029 E. WASHINGTON STREET P. O. BOX 372	INDIANAPOLIS, IN 46206
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
93958	REPUBLIC ELECTRONICS CORPORATION	176 E 7TH STREET	PATERSON, NJ 07524
96733	SAN FERNANDO ELECTRIC MFG CO	1501 FIRST ST	SAN FERNANDO, CA 91341
T0679	DILECTRON, INC.	2669 S. MYRTLE AVE.	MONROVIA, CA 91016

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CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
T0987	SEMI PROCESSES INC	1971 N CAPITOL AVE	SAN JOSE CA 95132
T1015	MUSASHI WORKS OF HITACHI LTD	1450 JOSUIHON-CHO	KODAIRA-SHI TOKYO, JAPAN
T1282	XICOR,INC.	851 BUCKEYE COURT	MILPITAS, CA 95035

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-7315-00			CKT BOARD ASSY:SWITCH	80009	670-7315-00
A2	670-7316-00	B010100	B062059	CKT BOARD ASSY:LED	80009	670-7316-00
A2	670-7316-01	B062060		CKT BOARD ASSY:LED	80009	670-7316-01
A3	670-7317-00			CKT BOARD ASSY:INTERCONNECT	80009	670-7317-00
A4	670-7318-00	B010100	B040399	CKT BOARD ASSY:PREAMP	80009	670-7318-00
A4	670-7318-01	B040400	B062059	CKT BOARD ASSY:PREAMP	80009	670-7318-01
A4	670-7318-02	B062060		CKT BOARD ASSY:PREAMP	80009	670-7318-02
A5	670-7319-00	B010100	B050483	CKT BOARD ASSY:CCD	80009	670-7319-00
A5	670-7319-01	B050484	B050595	CKT BOARD ASSY:CCD	80009	670-7319-01
A5	670-7319-02	B050596		CKT BOARD ASSY:CCD	80009	670-7319-02
A6	670-7320-00	B010100	B040399	CKT BOARD ASSY:DISPLAY	80009	670-7320-00
A6	670-7320-01	B040400	B061194	CKT BVOARD ASSY:DISPLAY	80009	670-7320-01
A6	670-7320-02	B061195	B063249	CKT BOARD ASSY:DISPLAY	80009	670-7320-02
A6	670-7320-03	B063250		CKT BOARD ASSY:DISPLAY	80009	670-7320-03
A7	670-7321-00	B010100	B061194	CKT BOARD ASSY:POWER SUPPLY	80009	670-7321-00
A7	670-7321-01	B061195		CKT BOARD ASSY:POWER SUPPLY	80009	670-7321-01
A8	670-7322-00			CKT BOARD ASSY:MEMORY	80009	670-7322-00
A9	670-7323-00	B010100	B029999	CKT BOARD ASSY:MPU	80009	670-7323-00
A9	670-7323-01	B030000	B061869	CKT BOARD ASSY:MPU	80009	670-7323-01
A9	670-7323-03	B061369	B061869	CKT BOARD ASSY:MPU	80009	670-7323-03
A9	670-7323-04	B061870	B062199	CKT BOARD ASSY:MPU	80009	670-7323-04
A9	670-7323-05	B062200		CKT BOARD ASSY:MPU	80009	670-7323-05
A10	670-7324-00	B010100	B040399	CKT BOARD ASSY:TRIGGER	80009	670-7324-00
A10	670-7324-01	B040400	B062019	CKT BOARD ASSY:TRIGGER	80009	670-7324-01
A10	670-7324-02	B062020		CKT BOARD ASSY:TRIGGER	80009	670-7324-02
A11	670-7325-00	B010100	B050595	CKT BOARD ASSY:TIME BASE	80009	670-7325-00
A11	670-7325-02	B050596		CKT BOARD ASSY:TIME BASE	80009	670-7325-02
A12	119-1444-00			ATTENUATOR,VAR:CHANNEL 2	80009	119-1444-00
A13	119-1444-00			ATTENUATOR,VAR:CHANNEL 2	80009	119-1444-00
.						
.						
A1	670-7315-00			CKT BOARD ASSY:SWITCH	80009	670-7315-00
.						
A1C310	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A1C320	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A1C330	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A1C420	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A1DS240	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A1DS400	150-1029-00			LT EMITTING DIO:GREEN,565NM,35MA	53184	XC209G
A1R120	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9) RES	91637	MSP10A01-472M
A1R121	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9) RES	91637	MSP10A01-472M
A1R320	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9) RES	91637	MSP10A01-472M
A1S100	263-0087-00			SWITCH,ROTARY:CHANNEL 1 & 2	80009	263-0087-00
A1S120	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S121	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S122	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S130	263-0087-00			SWITCH,ROTARY:CHANNEL 1 & 2	80009	263-0087-00
A1S140	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S141	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S142	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S143	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S200	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S201	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S202	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1S203	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S204	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S205	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S210	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S211	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S220	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S221	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S222	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S223	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S224	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S225	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S230	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S231	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S232	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S233	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S240	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S241	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S300	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S301	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S302	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S303	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S304	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S310	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S311	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S320	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S321	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S322	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S323	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S330	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S340	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S400	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S401	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S402	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S403	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S404	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S405	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S410	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S411	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S412	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S413	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S414	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S415	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S420	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S421	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A1S430	263-0088-00			SWITCH,ROTARY:TIME/DIV	80009	263-0088-00
A1U310	156-1229-01			MICROCIRCUIT,DI:QUAD 2 TO 1 SEL/MUX	01295	SN74LS258NP3
A1U320	156-1432-00			MICROCIRCUIT,DI:DUAL 2/4 LINE DECODER/DEMUX	01295	SN74LS156
A1U330	156-0916-02			MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97A
A1U420	156-1229-01			MICROCIRCUIT,DI:QUAD 2 TO 1 SEL/MUX	01295	SN74LS258NP3

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2	670-7316-00	B010100	B062059	CKT BOARD ASSY:LED	80009	670-7316-00
A2	670-7316-01	B062060		CKT BOARD ASSY:LED	80009	670-7316-01
A2C100	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C110	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C115	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A2C116	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C130	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C140	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C227	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C241	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C310	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C335	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C430	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C500	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C730	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2DS120	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS121	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS122	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS140	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS141	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS142	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS201	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS203	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS220	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS221	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS230	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS231	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS240	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS301	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS303	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS305	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS307	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS310	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS311	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS320	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS321	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS322	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS323	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS330	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS331	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS332	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS340	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS341	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS342	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS400	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS401	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS410	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS420	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS421	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS500	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS501	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS502	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2DS510	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS520	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS700	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS701	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS702	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS710	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS800	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS801	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS802	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS803	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS804	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS805	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS810	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS811	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2DS812	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A2L221	120-0407-00			XFMR,TOROID:5 TURNS SINGLE	80009	120-0407-00
A2R100	311-2163-00			RES.,VAR,NONWIR:5K OHM,20%,0.5W	12697	CM43506
A2R125	307-0592-00			RES,NTWK,FXD FI:9,220 OHM,2%,2W	91637	MSP10A01-221G
A2R130	311-2163-00			RES.,VAR,NONWIR:5K OHM,20%,0.5W	12697	CM43506
A2R200	315-0202-00	B010100	B062059	RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A2R200	315-0102-00	B062060		RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A2R202	311-2171-00			RES.,VAR,NONWIR:20K OHM,10%,1W	01121	SPPG024S203U
A2R203	307-0717-00			RES NTWK,FXD FI:4,100 OHM,2%,0.3W	11236	750-83-R100
A2R223	311-2171-00			RES.,VAR,NONWIR:20K OHM,10%,1W	01121	SPPG024S203U
A2R235	307-0592-00			RES,NTWK,FXD FI:9,220 OHM,2%,2W	91637	MSP10A01-221G
A2R240	315-0202-00	B010100	B062059	RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A2R240	315-0102-00	B062060		RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A2R300	307-0592-00			RES,NTWK,FXD FI:9,220 OHM,2%,2W	91637	MSP10A01-221G
A2R301	307-0717-00			RES NTWK,FXD FI:4,100 OHM,2%,0.3W	11236	750-83-R100
A2R305	307-0592-00			RES,NTWK,FXD FI:9,220 OHM,2%,2W	91637	MSP10A01-221G
A2R310	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	57668	NTR25J-E220E
A2R320	307-0790-00			RES NTWK,FXD,FI:5,220 OHM,2%,0.15W	01121	206A221
A2R341	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	57668	NTR25J-E220E
A2R440	311-2167-00			RES.,VAR,NONWIR:5K OHM,10%,0.5W	12697	CM43512
A2R540	311-2167-00			RES.,VAR,NONWIR:5K OHM,10%,0.5W	12697	CM43512
A2R600	311-2164-00			RES.,VAR,NONWIR:5K OHM,20%,0.5W	12697	CM43492
A2R630	311-2190-00			RES.,VAR,NONWIR:5K OHM,10%,,0.5W	12697	MODEL 338
A2R640	311-2167-00			RES.,VAR,NONWIR:5K OHM,10%,0.5W	12697	CM43512
A2R700	307-0592-00			RES,NTWK,FXD FI:9,220 OHM,2%,2W	91637	MSP10A01-221G
A2R740	311-2167-00			RES.,VAR,NONWIR:5K OHM,10%,0.5W	12697	CM43512
A2R800	307-0592-00			RES,NTWK,FXD FI:9,220 OHM,2%,2W	91637	MSP10A01-221G
A2R840	311-2167-00			RES.,VAR,NONWIR:5K OHM,10%,0.5W	12697	CM43512
A2U100	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3 OR
A2U110	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3 OR
A2U120	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3 OR
A2U130	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3 OR
A2U140	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3 OR
A2U310	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3 OR
A2U335	156-0390-02			MICROCIRCUIT,DI:DUAL 4/2 LINE DCDR/DEMUX	01295	SN74LS155
A2U430	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245 N3ORJ4
A2U500	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3 OR
A2U720	156-1444-01			MICROCIRCUIT,DI:NMOS,GPIB ADAPTER	01295	TMS9914NL
A2U730	156-1414-02			MICROCIRCUIT,DI:OCTAL GPIB BUS XCVR	27014	DS75160A
A2U735	156-1415-01			MICROCIRCUIT,DI:OCTAL GPIB XCVR-MANAGEMENT	27014	DS75161A

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A3	670-7317-00			CKT BOARD ASSY:INTERCONNECT	80009	670-7317-00
A3C260	281-0755-00			CAP.,FXD,CER DI:1.8PF,0.1%,500V	96733	R2731
A3C360	281-0755-00			CAP.,FXD,CER DI:1.8PF,0.1%,500V	96733	R2731
A3C560	281-0755-00			CAP.,FXD,CER DI:1.8PF,0.1%,500V	96733	R2731
A3C650	281-0755-00			CAP.,FXD,CER DI:1.8PF,0.1%,500V	96733	R2731
A3C690	281-0755-00			CAP.,FXD,CER DI:1.8PF,0.1%,500V	96733	R2731
A3L680	108-0598-00			COIL,RF:200UH	80009	108-0598-00
A3L820	108-0598-00			COIL,RF:200UH	80009	108-0598-00
A3L825	108-0598-00			COIL,RF:200UH	80009	108-0598-00
A3L840	108-0598-00			COIL,RF:200UH	80009	108-0598-00
A3R310	307-0717-00			RES NTWK,FXD FI:4,100 OHM,2%,0.3W	11236	750-83-R100
A3R410	307-0717-00			RES NTWK,FXD FI:4,100 OHM,2%,0.3W	11236	750-83-R100
A3R760	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A3R810	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0

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A4	670-7318-00	B010100	B040399	CKT BOARD ASSY:PREAMP	80009	670-7318-00
A4	670-7318-01	B040400	B062059	CKT BOARD ASSY:PREAMP	80009	670-7318-01
A4	670-7318-02	B062060		CKT BOARD ASSY:PREAMP	80009	670-7318-02
A4C140	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C210	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C211	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C230	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C231	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C240	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C241	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A4C250	281-0864-00			CAP.,FXD,CER DI:430PF,5%,100V	12969	CGD431JEN
A4C300	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C350	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C400	281-0851-00			CAP.,FXD,CER DI:180PF,5%,100VDC	04222	MA101A181JAA
A4C410	281-0851-00			CAP.,FXD,CER DI:180PF,5%,100VDC	04222	MA101A181JAA
A4C420	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C421	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C430	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C431	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C450	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C500	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A4C510	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A4C511	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A4C520	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C524	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C530	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C540	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A4C541	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A4C550	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A4C600	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C610	281-0808-00			CAP.,FXD,CER DI:7PF,20%,100V	04222	MA101A7R04AA
A4C611	281-0808-00			CAP.,FXD,CER DI:7PF,20%,100V	04222	MA101A7R04AA
A4C620	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C621	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C630	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C631	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C640	281-0808-00			CAP.,FXD,CER DI:7PF,20%,100V	04222	MA101A7R04AA
A4C641	281-0808-00			CAP.,FXD,CER DI:7PF,20%,100V	04222	MA101A7R04AA
A4C700	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C710	281-0158-00			CAP.,VAR,CER D1:7-45PF,25V	73899	DVJ-5006
A4C720	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C721	283-0017-00	B010100	B061729	CAP.,FXD,CER DI:1UF,+80-20%,3V	T0679	RT31052-H
A4C721	283-0059-00	B061730		CAP.,FXD,CER DI:1UF,+80-20%,50V	96733	ADVIXE
A4C722	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C723	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C724	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C725	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C740	281-0158-00			CAP.,VAR,CER D1:7-45PF,25V	73899	DVJ-5006
A4C741	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C750	283-0017-00	B010100	B061729	CAP.,FXD,CER DI:1UF,+80-20%,3V	T0679	RT31052-H
A4C750	283-0059-00	B061730		CAP.,FXD,CER DI:1UF,+80-20%,50V	96733	ADVIXE
A4C751	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C752	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA

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A4C810	281-0823-00			CAP.,FXD,CER DI:470PF,10%,50V	04222	MA105A471KAA
A4C811	281-0158-00			CAP.,VAR,CER D1:7-45PF,25V	73899	DVJ-5006
A4C813	281-0158-00			CAP.,VAR,CER D1:7-45PF,25V	73899	DVJ-5006
A4C820	281-0158-00			CAP.,VAR,CER D1:7-45PF,25V	73899	DVJ-5006
A4C840	281-0823-00			CAP.,FXD,CER DI:470PF,10%,50V	04222	MA105A471KAA
A4C841	281-0158-00			CAP.,VAR,CER D1:7-45PF,25V	73899	DVJ-5006
A4C850	281-0158-00			CAP.,VAR,CER D1:7-45PF,25V	73899	DVJ-5006
A4C851	281-0158-00			CAP.,VAR,CER D1:7-45PF,25V	73899	DVJ-5006
A4C900	283-0348-00			CAP.,FXD,CER DI:0.5PF,+/-0.1PF,100V	51642	W150-100-NPO5088
A4C900	283-0158-00			CAP.,FXD,CER DI:1PF,10%,50V	51642	100-050-NP0-109B
A4C900	283-0160-00			CAP.,FXD,CER DI:1.5PF,10%,50V	93958	1C15RB
A4C900	283-0181-00			CAP.,FXD,CER DI:1.8PF,10%,100V	59660	8101B121COKO189B
A4C900	283-0185-00			CAP.,FXD,CER DI:2.5PF,5%,50V	96733	T-DG43BY2R5BP
A4C900	----- -----			(C900 SELECTED)		
A4C910	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A4C911	283-0348-00			CAP.,FXD,CER DI:0.5PF,+/-0.1PF,100V	51642	W150-100-NPO5088
A4C911	283-0158-00			CAP.,FXD,CER DI:1PF,10%,50V	51642	100-050-NP0-109B
A4C911	283-0160-00			CAP.,FXD,CER DI:1.5PF,10%,50V	93958	1C15RB
A4C911	283-0181-00			CAP.,FXD,CER DI:1.8PF,10%,100V	59660	8101B121COKO189B
A4C911	----- -----			(C911 SELECTED)		
A4C912	283-0183-00			CAP.,FXD,CER DI:0.045UF,20%,500V	56289	275C10
A4C912	283-0140-00			CAP.,FXD,CER DI:4.7PF,5%,50V	72982	8101E003A479C
A4C912	----- -----			(NOMINAL VALUE)		
A4C912	283-0260-00			CAP.,FXD,CER DI:5.6PF,5%,200V	51642	150 200NP0569C
A4C912	283-0157-00			CAP.,FXD,CER DI:7PF,5%,500V	59660	8111B065COHO709D
A4C912	283-0175-00			CAP.,FXD,CER DI:10PF,5%,200V	96733	TDR43BY100DP
A4C912	----- -----			(C912 SELECTED)		
A4C913	283-0140-00	B010100	B040399	CAP.,FXD,CER DI:4.7PF,5%,50V	72982	8101E003A479C
A4C913	283-0260-00	B010100	B040399	CAP.,FXD,CER DI:5.6PF,5%,200V	51642	150 200NP0569C
A4C913	283-0157-00	B010100	B040399	CAP.,FXD,CER DI:7PF,5%,500V	59660	8111B065COHO709D
A4C913	283-0175-00	B010100	B040399	CAP.,FXD,CER DI:10PF,5%,200V	96733	TDR43BY100DP
A4C913	283-0168-00	B010100	B040399	CAP.,FXD,CER DI:12PF,5%,100V	72982	8101B121C0G0120J
A4C913	----- -----			(C913 SELECTED)		
A4C913	281-0218-00	B040400		CAP.,VAR,CER DI:1-5PF,+2-2.5%,100V	59660	513-013A1-5
A4C920	281-0852-00			CAP.,FXD,CER DI:1800PF,10%,100VDC	04222	MA101C182KAA
A4C940	283-0348-00			CAP.,FXD,CER DI:0.5PF,+/-0.1PF,100V	51642	W150-100-NPO5088
A4C940	283-0158-00			CAP.,FXD,CER DI:1PF,10%,50V	51642	100-050-NP0-109B
A4C940	283-0160-00			CAP.,FXD,CER DI:1.5PF,10%,50V	93958	1C15RB
A4C940	283-0181-00			CAP.,FXD,CER DI:1.8PF,10%,100V	59660	8101B121COKO189B
A4C940	----- -----			(C940 SELECTED)		
A4C947	283-0348-00			CAP.,FXD,CER DI:0.5PF,+/-0.1PF,100V	51642	W150-100-NPO5088
A4C947	283-0158-00			CAP.,FXD,CER DI:1PF,10%,50V	51642	100-050-NP0-109B
A4C947	283-0160-00			CAP.,FXD,CER DI:1.5PF,10%,50V	93958	1C15RB
A4C947	283-0181-00			CAP.,FXD,CER DI:1.8PF,10%,100V	59660	8101B121COKO189B
A4C947	283-0185-00			CAP.,FXD,CER DI:2.5PF,5%,50V	96733	T-DG43BY2R5BP
A4C947	----- -----			(C947 SELECTED)		
A4C950	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A4C951	281-0852-00			CAP.,FXD,CER DI:1800PF,10%,100VDC	04222	MA101C182KAA
A4C952	283-0168-00			CAP.,FXD,CER DI:12PF,5%,100V	72982	8101B121C0G0120J
A4C953	283-0183-00			CAP.,FXD,CER DI:0.045UF,20%,500V	56289	275C10
A4C953	283-0140-00			CAP.,FXD,CER DI:4.7PF,5%,50V	72982	8101E003A479C
A4C953	----- -----			(NOMINAL VALUE)		
A4C953	283-0260-00			CAP.,FXD,CER DI:5.6PF,5%,200V	51642	150 200NP0569C
A4C953	283-0157-00			CAP.,FXD,CER DI:7PF,5%,500V	59660	8111B065COHO709D

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A4C953	283-0175-00			CAP.,FXD,CER DI:10PF,5%,200V	96733	TDR43BY100DP
A4C953	----- -----			(C953 SELECTED)		
A4C954	283-0140-00	B010100	B040399	CAP.,FXD,CER DI:4.7PF,5%,50V	72982	8101E003A479C
A4C954	283-0260-00	B010100	B040399	CAP.,FXD,CER DI:5.6PF,5%,200V	51642	150 200NP0569C
A4C954	283-0157-00	B010100	B040399	CAP.,FXD,CER DI:7PF,5%,500V	59660	8111B065COHO709D
A4C954	283-0175-00	B010100	B040399	CAP.,FXD,CER DI:10PF,5%,200V	96733	TDR43BY100DP
A4C954	283-0168-00	B010100	B040399	CAP.,FXD,CER DI:12PF,5%,100V	72982	8101B121C0G0120J
A4C954	----- -----			(C954 SELECTED)		
A4C954	281-0218-00	B040400		CAP.,VAR,CER DI:1-5PF,+2-2.5%,100V	59660	513-013A1-5
A4C1000	281-0812-00	B010100	B019999	CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A4C1000	281-0765-00	B020000		CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710-100NP0101J
A4C1010	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C1011	281-0214-00			CAP.,VAR,CER DI:0.5-3PF,400V	80031	2502A0R503VP02F0
A4C1020	281-0221-00			CAP.,VAR,CER DI:2-10PF,100V	59660	513-013A 2 0-10
A4C1021	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C1022	283-0168-00			CAP.,FXD,CER DI:12PF,5%,100V	72982	8101B121C0G0120J
A4C1023	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A4C1031	281-0812-00	B010100	B019999	CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A4C1031	281-0765-00	B020000		CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710-100NP0101J
A4C1040	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C1050	281-0221-00			CAP.,VAR,CER DI:2-10PF,100V	59660	513-013A 2 0-10
A4C1051	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C1052	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A4C1053	281-0214-00			CAP.,VAR,CER DI:0.5-3PF,400V	80031	2502A0R503VP02F0
A4C1100	281-0823-00			CAP.,FXD,CER DI:470PF,10%,50V	04222	MA105A471KAA
A4C1110	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C1130	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C1131	281-0823-00			CAP.,FXD,CER DI:470PF,10%,50V	04222	MA105A471KAA
A4C1132	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C1140	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A4C1141	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C1200	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A4C1220	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A4C1221	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A4C1240	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C1241	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C1242	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C1250	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A4C1251	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A4CR610	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR611	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR640	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR650	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1010	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1020	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1021	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1040	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1050	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1051	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1110	152-0246-00			SEMICOND DEVICE:SW,SI,40V,200MA	14433	WG1537TK
A4CR1111	152-0246-00			SEMICOND DEVICE:SW,SI,40V,200MA	14433	WG1537TK
A4CR1112	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1140	152-0246-00			SEMICOND DEVICE:SW,SI,40V,200MA	14433	WG1537TK
A4CR1141	152-0246-00			SEMICOND DEVICE:SW,SI,40V,200MA	14433	WG1537TK

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A4CR1142	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1143	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1200	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1201	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1210	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1211	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1212	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1213	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1214	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1215	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1216	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1220	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1230	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1240	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1241	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1242	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1243	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1244	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4CR1245	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A4L210	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A4L211	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A4L220	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A4L221	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L222	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L230	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L320	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L420	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L430	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L530	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L630	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L631	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L632	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L730	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L731	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L732	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L1020	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L1021	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L1022	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L1120	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L1121	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L1122	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4L1123	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A4Q300	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A4Q400	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A4Q410	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A4Q440	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A4Q500	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A4Q510	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A4Q540	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A4Q550	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A4Q610	151-0369-02			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0369-02
A4Q611	151-0212-00			TRANSISTOR:SILICON,NPN	04713	SRF 518
A4Q612	151-0369-02			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0369-02
A4Q613	151-0212-00			TRANSISTOR:SILICON,NPN	04713	SRF 518

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A4Q640	151-0369-02			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0369-02
A4Q641	151-0212-00			TRANSISTOR:SILICON,NPN	04713	SRF 518
A4Q642	151-0369-02			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0369-02
A4Q643	151-0212-00			TRANSISTOR:SILICON,NPN	04713	SRF 518
A4Q800	151-0711-00			TRANSISTOR:SILICON,NPN	04713	SPS8224
A4Q801	151-0711-00			TRANSISTOR:SILICON,NPN	04713	SPS8224
A4Q830	151-0711-00			TRANSISTOR:SILICON,NPN	04713	SPS8224
A4Q831	151-0711-00			TRANSISTOR:SILICON,NPN	04713	SPS8224
A4Q910	151-1103-00			TRANSISTOR:FE,N-CHANNEL,S1,TO-72	T0987	1S017
A4Q911	151-1103-00			TRANSISTOR:FE,N-CHANNEL,S1,TO-72	T0987	1S017
A4Q913	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A4Q920	151-1103-00			TRANSISTOR:FE,N-CHANNEL,S1,TO-72	T0987	1S017
A4Q921	151-1025-00			TRANSISTOR:SILICON,JFE,N-CHANNEL	01295	SFB8129
A4Q922	151-1103-00			TRANSISTOR:FE,N-CHANNEL,S1,TO-72	T0987	1S017
A4Q940	151-1103-00			TRANSISTOR:FE,N-CHANNEL,S1,TO-72	T0987	1S017
A4Q941	151-1103-00			TRANSISTOR:FE,N-CHANNEL,S1,TO-72	T0987	1S017
A4Q942	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A4Q950	151-1103-00			TRANSISTOR:FE,N-CHANNEL,S1,TO-72	T0987	1S017
A4Q951	151-1103-00			TRANSISTOR:FE,N-CHANNEL,S1,TO-72	T0987	1S017
A4Q952	151-1025-00			TRANSISTOR:SILICON,JFE,N-CHANNEL	01295	SFB8129
A4Q1010	151-0427-00			TRANSISTOR:SILICON,NPN	07263	S39287
A4Q1012	151-1103-00			TRANSISTOR:FE,N-CHANNEL,S1,TO-72	T0987	1S017
A4Q1020	151-0711-00			TRANSISTOR:SILICON,NPN	04713	SPS8224
A4Q1021	151-0369-02			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0369-02
A4Q1041	151-0427-00			TRANSISTOR:SILICON,NPN	07263	S39287
A4Q1042	151-1103-00			TRANSISTOR:FE,N-CHANNEL,S1,TO-72	T0987	1S017
A4Q1050	151-0369-02			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0369-02
A4Q1051	151-0711-00			TRANSISTOR:SILICON,NPN	04713	SPS8224
A4Q1230	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A4R140	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A4R200	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A4R201	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A4R220	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	57668	NTR25J-E 56K
A4R230	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A4R231	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	57668	NTR25J-E 56K
A4R232	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A4R240	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A4R241	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A4R242	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A4R243	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A4R244	321-0442-00			RES.,FXD,FILM:392K OHM,1%,0.125W	91637	MFF1816G39202F
A4R245	321-0442-00			RES.,FXD,FILM:392K OHM,1%,0.125W	91637	MFF1816G39202F
A4R246	321-0442-00			RES.,FXD,FILM:392K OHM,1%,0.125W	91637	MFF1816G39202F
A4R247	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A4R250	321-0138-00			RES.,FXD,FILM:267 OHM,1%,0.125W	91637	CMF55116G267R0F
A4R251	321-0184-00			RES.,FXD,FILM:806 OHM,1%,0.125W	91637	CMF55116G806R0F
A4R252	321-0442-00			RES.,FXD,FILM:392K OHM,1%,0.125W	91637	MFF1816G39202F
A4R253	321-0285-00			RES.,FXD,FILM:9.09K OHM,1%,0.125W	91637	MFF1816G90900F
A4R254	321-0285-00			RES.,FXD,FILM:9.09K OHM,1%,0.125W	91637	MFF1816G90900F
A4R255	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A4R300	322-0164-00			RES.,FXD,FILM:499 OHM,1%,0.25W	75042	CEBT0-4990F
A4R301	315-0163-00			RES.,FXD,CMPSN:16K OHM,5%,0.25W	57668	NTR25J-E16K0
A4R330	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A4R331	315-0334-00			RES.,FXD,CMPSN:330K OHM,5%,0.25W	01121	CB3345

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A4R332	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A4R333	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A4R334	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A4R335	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A4R340	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A4R341	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A4R342	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A4R400	321-0238-00			RES.,FXD,FILM:2.94K OHM,1%,0.125W	91637	MFF1816G29400F
A4R401	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	57668	NTR25J-E180E
A4R402	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	57668	NTR25J-E470E
A4R403	321-0094-00			RES.,FXD,FILM:93.1 OHM,1%,0.125W	91637	CMF55116G93R10F
A4R404	321-0098-00			RES.,FXD,FILM:102 OHM,1%,0.125W	91637	MFF1816G102R0F
A4R410	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	57668	NTR25J-E180E
A4R411	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	57668	NTR25J-E470E
A4R412	321-0094-00			RES.,FXD,FILM:93.1 OHM,1%,0.125W	91637	CMF55116G93R10F
A4R413	321-0098-00			RES.,FXD,FILM:102 OHM,1%,0.125W	91637	MFF1816G102R0F
A4R440	322-0164-00			RES.,FXD,FILM:499 OHM,1%,0.25W	75042	CEBT0-4990F
A4R441	321-0238-00			RES.,FXD,FILM:2.94K OHM,1%,0.125W	91637	MFF1816G29400F
A4R442	315-0163-00			RES.,FXD,CMPSN:16K OHM,5%,0.25W	57668	NTR25J-E16K0
A4R443	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A4R444	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A4R445	311-0622-00			RES.,VAR,NONWIR:100 OHM,10%,0.50W	32997	3329H-L58-101
A4R500	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	57668	NTR25J-E 430E
A4R501	321-0085-00			RES.,FXD,FILM:75 OHM,1%,0.125W	91637	CMF55116G75R00F
A4R502	321-0075-00			RES.,FXD,FILM:59 OHM,1%,0.125W	91637	CMF55116G59R00F
A4R510	321-0160-00			RES.,FXD,FILM:453 OHM,1%,0.125W	91637	CMF116G453R0F
A4R511	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A4R512	321-0160-00			RES.,FXD,FILM:453 OHM,1%,0.125W	91637	CMF116G453R0F
A4R513	321-0043-00			RES.,FXD,FILM:27.4 OHM,1%,0.125W	91637	CMF55116G27R40F
A4R514	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A4R515	321-0085-00			RES.,FXD,FILM:75 OHM,1%,0.125W	91637	CMF55116G75R00F
A4R516	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	57668	NTR25J-E 130E
A4R517	321-0062-00			RES.,FXD,FILM:43.2 OHM,1%,0.125W	91637	CMF55-116G43R20F
A4R518	311-0622-00			RES.,VAR,NONWIR:100 OHM,10%,0.50W	32997	3329H-L58-101
A4R520	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	57668	NTR25J-E 430E
A4R530	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A4R531	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A4R540	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A4R541	321-0160-00			RES.,FXD,FILM:453 OHM,1%,0.125W	91637	CMF116G453R0F
A4R542	321-0075-00			RES.,FXD,FILM:59 OHM,1%,0.125W	91637	CMF55116G59R00F
A4R543	321-0043-00			RES.,FXD,FILM:27.4 OHM,1%,0.125W	91637	CMF55116G27R40F
A4R544	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	57668	NTR25J-E 130E
A4R545	321-0062-00			RES.,FXD,FILM:43.2 OHM,1%,0.125W	91637	CMF55-116G43R20F
A4R546	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A4R550	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A4R551	321-0160-00			RES.,FXD,FILM:453 OHM,1%,0.125W	91637	CMF116G453R0F
A4R552	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A4R600	321-0157-00			RES.,FXD,FILM:422 OHM,1%,0.125W	91637	CMF55116G422R0F
A4R601	321-0132-00			RES.,FXD,FILM:232 OHM,1%,0.125W	91637	MFF1816G232R0F
A4R602	321-0205-00			RES.,FXD,FILM:1.33K OHM,1%,0.125W	91637	CMF55116G13300F
A4R603	321-0142-00			RES.,FXD,FILM:294 OHM,1%,0.125W	91637	CMF55116G294R0F
A4R604	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A4R605	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	57668	NTR25J-E 3K6
A4R610	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	57668	NTR25J-E 120E

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A4R611	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A4R612	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A4R613	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	57668	NTR25J-E 120E
A4R620	321-0157-00			RES.,FXD,FILM:422 OHM,1%,0.125W	91637	CMF55116G422R0F
A4R621	321-0125-00			RES.,FXD,FILM:196 OHM,1%,0.125W	91637	CMF55116G196R0F
A4R622	321-0142-00			RES.,FXD,FILM:294 OHM,1%,0.125W	91637	CMF55116G294R0F
A4R623	321-0205-00			RES.,FXD,FILM:1.33K OHM,1%,0.125W	91637	CMF55116G13300F
A4R624	321-0132-00			RES.,FXD,FILM:232 OHM,1%,0.125W	91637	MFF1816G232R0F
A4R630	321-0125-00			RES.,FXD,FILM:196 OHM,1%,0.125W	91637	CMF55116G196R0F
A4R631	321-0132-00			RES.,FXD,FILM:232 OHM,1%,0.125W	91637	MFF1816G232R0F
A4R640	321-0157-00			RES.,FXD,FILM:422 OHM,1%,0.125W	91637	CMF55116G422R0F
A4R641	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	57668	NTR25J-E 120E
A4R642	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A4R643	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A4R644	321-0205-00			RES.,FXD,FILM:1.33K OHM,1%,0.125W	91637	CMF55116G13300F
A4R645	321-0142-00			RES.,FXD,FILM:294 OHM,1%,0.125W	91637	CMF55116G294R0F
A4R650	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	57668	NTR25J-E 120E
A4R651	321-0157-00			RES.,FXD,FILM:422 OHM,1%,0.125W	91637	CMF55116G422R0F
A4R652	321-0142-00			RES.,FXD,FILM:294 OHM,1%,0.125W	91637	CMF55116G294R0F
A4R653	321-0205-00			RES.,FXD,FILM:1.33K OHM,1%,0.125W	91637	CMF55116G13300F
A4R654	321-0132-00			RES.,FXD,FILM:232 OHM,1%,0.125W	91637	MFF1816G232R0F
A4R700	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	57668	NTR25J-E07K5
A4R701	311-1035-00			RES.,VAR,NONWIR:50K OHM,10%,0.50W	73138	82-40-0
A4R702	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A4R703	321-0113-00			RES.,FXD,FILM:147 OHM,1%,0.125W	91637	CMF55116G147R0F
A4R704	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A4R705	321-0214-00			RES.,FXD,FILM:1.65K OHM,1%,0.125W	91637	MFF1816G16500F
A4R706	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A4R707	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A4R708	315-0683-00			RES.,FXD,CMPSN:68K OHM,5%,0.25W	57668	NTR25J-E68K0
A4R709	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	57668	NTR25J-E75K0
A4R710	311-0622-00			RES.,VAR,NONWIR:100 OHM,10%,0.50W	32997	3329H-L58-101
A4R720	311-0613-00			RES.,VAR,NONWIR:100K OHM,10%,0.50W	73138	82-27-2
A4R721	315-0304-00			RES.,FXD,CMPSN:300K OHM,5%,0.25W	57668	NTR25J-E300K
A4R722	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	57668	NTR25J-E12K0
A4R723	315-0113-00			RES.,FXD,CMPSN:11K OHM,5%,0.25W	57668	NTR25J-E 11K
A4R730	321-0113-00			RES.,FXD,FILM:147 OHM,1%,0.125W	91637	CMF55116G147R0F
A4R731	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	57668	NTR25J-E07K5
A4R732	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A4R733	311-1035-00			RES.,VAR,NONWIR:50K OHM,10%,0.50W	73138	82-40-0
A4R740	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A4R741	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A4R742	321-0214-00			RES.,FXD,FILM:1.65K OHM,1%,0.125W	91637	MFF1816G16500F
A4R743	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A4R744	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A4R745	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	57668	NTR25J-E75K0
A4R750	311-0622-00			RES.,VAR,NONWIR:100 OHM,10%,0.50W	32997	3329H-L58-101
A4R751	311-0613-00			RES.,VAR,NONWIR:100K OHM,10%,0.50W	73138	82-27-2
A4R752	315-0304-00			RES.,FXD,CMPSN:300K OHM,5%,0.25W	57668	NTR25J-E300K
A4R753	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	57668	NTR25J-E12K0
A4R754	315-0113-00			RES.,FXD,CMPSN:11K OHM,5%,0.25W	57668	NTR25J-E 11K
A4R800	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A4R801	311-1731-00			RES.,VAR,NONWIR:20 OHM,0.5W	73138	91AR20-94A
A4R802	321-0108-00			RES.,FXD,FILM:130 OHM,1%,0.125W	91637	CMF55116G13000F

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A4R803	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A4R810	311-0609-00			RES.,VAR,NONWIR:2K OHM,10%,0.50W	73138	82-26-1
A4R811	321-0109-00			RES.,FXD,FILM:133 OHM,1%,0.125W	91637	CMF55116G133R0F
A4R812	321-0108-00			RES.,FXD,FILM:130 OHM,1%,0.125W	91637	CMF55116G13000F
A4R813	321-0105-00			RES.,FXD,FILM:121 OHM,1%,0.125W	91637	CMF55116G121R0F
A4R820	311-1007-00			RES.,VAR,NONWIR:20 OHM,20%,0.50W	73138	82PR2038B
A4R821	311-0607-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	82-25-2
A4R822	311-0635-00			RES.,VAR,NONWW:TRMR,1K OHM,10%,0.5%,0.5W	73138	82PR1K-60
A4R823	321-0053-00			RES.,FXD,FILM:34.8 OHM,1%,0.125W	91637	MFF1816G34R80F
A4R825	321-0105-00			RES.,FXD,FILM:121 OHM,1%,0.125W	91637	CMF55116G121R0F
A4R830	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A4R831	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	57668	NTR25J-E 3K6
A4R832	315-0683-00			RES.,FXD,CMPSN:68K OHM,5%,0.25W	57668	NTR25J-E68K0
A4R833	311-1731-00			RES.,VAR,NONWIR:20 OHM,0.5W	73138	91AR20-94A
A4R834	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A4R840	311-0609-00			RES.,VAR,NONWIR:2K OHM,10%,0.50W	73138	82-26-1
A4R841	321-0109-00			RES.,FXD,FILM:133 OHM,1%,0.125W	91637	CMF55116G133R0F
A4R842	321-0108-00			RES.,FXD,FILM:130 OHM,1%,0.125W	91637	CMF55116G13000F
A4R843	321-0108-00			RES.,FXD,FILM:130 OHM,1%,0.125W	91637	CMF55116G13000F
A4R844	321-0105-00			RES.,FXD,FILM:121 OHM,1%,0.125W	91637	CMF55116G121R0F
A4R850	311-1007-00			RES.,VAR,NONWIR:20 OHM,20%,0.50W	73138	82PR2038B
A4R851	311-0607-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	82-25-2
A4R852	311-0635-00			RES.,VAR,NONWW:TRMR,1K OHM,10%,0.5%,0.5W	73138	82PR1K-60
A4R853	321-0053-00			RES.,FXD,FILM:34.8 OHM,1%,0.125W	91637	MFF1816G34R80F
A4R854	321-0105-00			RES.,FXD,FILM:121 OHM,1%,0.125W	91637	CMF55116G121R0F
A4R900	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A4R901	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A4R902	311-1551-00			RES.,VAR,NONWIR:TRMR,1M OHM,0.50W	73138	91-73-0
A4R910	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A4R911	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A4R912	317-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.125W	01121	BB2405
A4R913	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	CMF55116C50RR00C
A4R914	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A4R915	321-0085-07			RES.,FXD,FILM:75 OHM,1%,0.125W	07716	CEA75 OHM 0.1P
A4R916	321-0927-07			RES.,FXD,FILM:125 OHM,0.1%,0.125W	91637	CMF55-116C125R0B
A4R917	317-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.125W	01121	BB9115
A4R917	----- -----			(+/- 50% OF NOMINAL VALUE)		
A4R918	317-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.125W	01121	BB1125
A4R918	----- -----			(+/- 50% OF NOMINAL VALUE)		
A4R920	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A4R921	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	57668	NTR25J-E680E
A4R922	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A4R923	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A4R930	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A4R931	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A4R932	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A4R933	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A4R934	311-1551-00			RES.,VAR,NONWIR:TRMR,1M OHM,0.50W	73138	91-73-0
A4R940	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A4R941	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A4R942	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A4R943	317-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.125W	01121	BB2405
A4R944	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	CMF55116C50RR00C
A4R945	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0

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A4R946	317-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.125W	01121	BB1125
A4R946	----- -----			(+/- 50% OF NOMINAL VALUE)		
A4R947	317-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.125W	01121	BB9115
A4R947	----- -----			(+/- 50% OF NOMINAL VALUE)		
A4R950	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A4R951	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	57668	NTR25J-E680E
A4R952	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A4R953	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A4R954	321-0085-07			RES.,FXD,FILM:75 OHM,1%,0.125W	07716	CEA75 OHM 0.1P
A4R956	321-0927-07			RES.,FXD,FILM:125 OHM,0.1%,0.125W	91637	CMF55-116C125R0B
A4R1000	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	57668	NTR25J-E390E
A4R1001	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	57668	NTR25J-E 33E
A4R1002	321-0231-00			RES.,FXD,FILM:2.49K OHM,1%,0.125W	91637	MFF1816G24900F
A4R1003	311-1565-00			RES.,VAR,NONWIR:250 OHM,20%,0.50W	73138	91-87-0
A4R1004	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	57668	NTR25J-E 130E
A4R1010	321-0305-00			RES.,FXD,FILM:14.7K OHM,1%,0.125W	91637	MFF1816G14701F
A4R1011	321-0011-00			RES.,FXD,FILM:12.7 OHM,1%,0.125W	91637	MFF1816G12R70F
A4R1012	321-0011-00			RES.,FXD,FILM:12.7 OHM,1%,0.125W	91637	MFF1816G12R70F
A4R1013	321-0305-00			RES.,FXD,FILM:14.7K OHM,1%,0.125W	91637	MFF1816G14701F
A4R1014	321-0045-00			RES.,FXD,FILM:28.7 OHM,1%,0.125W	91637	MFF1816G28R70F
A4R1020	315-0240-00	B010100	B040399	RES.,FXD,CMPSN:24 OHM,5%,0.25W	57668	NTR25J-E24E0
A4R1020	315-0180-00	B040400		RES.,FXD,CMPSN:18 OHM,5%,0.25W	57668	NTR25J-E 18E
A4R1021	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A4R1021	----- -----			(NOMINAL VALUE)		
A4R1022	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	57668	NTR25J-E150E
A4R1030	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	57668	NTR25J-E390E
A4R1031	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	57668	NTR25J-E 33E
A4R1032	321-0231-00			RES.,FXD,FILM:2.49K OHM,1%,0.125W	91637	MFF1816G24900F
A4R1033	311-1565-00			RES.,VAR,NONWIR:250 OHM,20%,0.50W	73138	91-87-0
A4R1034	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	57668	NTR25J-E 130E
A4R1040	321-0305-00			RES.,FXD,FILM:14.7K OHM,1%,0.125W	91637	MFF1816G14701F
A4R1041	321-0011-00			RES.,FXD,FILM:12.7 OHM,1%,0.125W	91637	MFF1816G12R70F
A4R1042	321-0011-00			RES.,FXD,FILM:12.7 OHM,1%,0.125W	91637	MFF1816G12R70F
A4R1043	321-0305-00			RES.,FXD,FILM:14.7K OHM,1%,0.125W	91637	MFF1816G14701F
A4R1044	321-0045-00			RES.,FXD,FILM:28.7 OHM,1%,0.125W	91637	MFF1816G28R70F
A4R1050	315-0240-00	B010100	B040399	RES.,FXD,CMPSN:24 OHM,5%,0.25W	57668	NTR25J-E24E0
A4R1050	315-0180-00	B040400		RES.,FXD,CMPSN:18 OHM,5%,0.25W	57668	NTR25J-E 18E
A4R1051	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A4R1052	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	57668	NTR25J-E150E
A4R1100	315-0625-00			RES.,FXD,CMPSN:6.2M OHM,5%,0.25W	01121	CB6255
A4R1101	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A4R1102	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	57668	NTR25J-E 6K2
A4R1103	315-0107-00			RES.,FXD,CMPSN:100M OHM,5%,0.25W	01121	CB1075
A4R1110	315-0107-00			RES.,FXD,CMPSN:100M OHM,5%,0.25W	01121	CB1075
A4R1120	321-0189-00			RES.,FXD,FILM:909 OHM,1%,0.125W	91637	CMF55116G909R0F
A4R1130	315-0625-00			RES.,FXD,CMPSN:6.2M OHM,5%,0.25W	01121	CB6255
A4R1131	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A4R1132	315-0107-00			RES.,FXD,CMPSN:100M OHM,5%,0.25W	01121	CB1075
A4R1133	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	57668	NTR25J-E 6K2
A4R1140	315-0107-00			RES.,FXD,CMPSN:100M OHM,5%,0.25W	01121	CB1075
A4R1150	321-0189-00			RES.,FXD,FILM:909 OHM,1%,0.125W	91637	CMF55116G909R0F
A4R1200	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A4R1201	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A4R1202	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E

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A4R1203	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A4R1220	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	57668	NTR25J-E 62E
A4R1221	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A4R1222	321-0230-00			RES.,FXD,FILM:2.43K OHM,1%,0.125W	24546	CT552431F
A4R1230	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	57668	NTR25J-E 3K6
A4R1231	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A4R1232	321-0230-00			RES.,FXD,FILM:2.43K OHM,1%,0.125W	24546	CT552431F
A4T610	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A4T640	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A4U230	156-0514-01			MICROCIRCUIT,DI:DIFF 4-CHANNEL MUX,SEL	80009	156-0514-01
A4U231	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	LM358J
A4U240	156-1272-00			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	18324	NE5532 FE-B
A4U300	156-0796-01			MICROCIRCUIT,DI:8 STG SHF & STORE BUS RGTR	80009	156-0796-01
A4U330	156-1225-01			MICROCIRCUIT,LI:DUAL COMPARATOR,SCREENED	27014	LM393N/A+
A4U331	156-0067-13	B010100	B062299	MICROCIRCUIT,LI:OPNL AMPL,SELECTED	01295	UA741CJG4
A4U331	156-0067-01	B062300		MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER,CHK	04713	MC1741CP1DS
A4U340	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A4U350	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A4U530	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	LM358J
A4U710	155-0216-00			MICROCIRCUIT,LI:PLRT INV & TRIG PICK OFF	80009	155-0216-00
A4U740	155-0216-00			MICROCIRCUIT,LI:PLRT INV & TRIG PICK OFF	80009	155-0216-00
A4U910	156-0495-02			MICROCIRCUIT,LI:QUAD OPNL AMPL,SELECTED	01295	LM324J4
A4U930	156-0495-02			MICROCIRCUIT,LI:QUAD OPNL AMPL,SELECTED	01295	LM324J4
A4U1100	156-1551-00			MICROCIRCUIT,LI:OPNL AMPL	02735	90593
A4U1130	156-1551-00			MICROCIRCUIT,LI:OPNL AMPL	02735	90593
A4U1230	156-0796-01			MICROCIRCUIT,DI:8 STG SHF & STORE BUS RGTR	80009	156-0796-01
A4VR400	152-0175-00			SEMICOND DEVICE:ZENER,0.4W,5.6V,5%	04713	SZG35008
A4VR430	152-0175-00			SEMICOND DEVICE:ZENER,0.4W,5.6V,5%	04713	SZG35008
A4VR620	152-0395-00	B010100	B062059	SEMICOND DEVICE:ZENER,0.4W,4.3V,5%	14552	TD332317
A4VR620	152-0693-00	B062060		SEMICOND DEVICE:ZENER,0.4W,4V,5%	80009	152-0693-00
A4VR650	152-0395-00	B010100	B062059	SEMICOND DEVICE:ZENER,0.4W,4.3V,5%	14552	TD332317
A4VR650	152-0693-00	B062060		SEMICOND DEVICE:ZENER,0.4W,4V,5%	80009	152-0693-00
A4VR1000	152-0127-00			SEMICOND DEVICE:ZENER,0.4W,7.5V,5%	04713	SZG35009K2
A4VR1030	152-0127-00			SEMICOND DEVICE:ZENER,0.4W,7.5V,5%	04713	SZG35009K2

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A5	670-7319-00	B010100	B050483	CKT BOARD ASSY:CCD	80009	670-7319-00
A5	670-7319-01	B050484	B050595	CKT BOARD ASSY:CCD	80009	670-7319-01
A5	670-7319-02	B050596		CKT BOARD ASSY:CCD	80009	670-7319-02
A5C160	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A5C161	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A5C230	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A5C240	283-0186-00			CAP.,FXD,CER DI:27PF,5%,50V	59660	811A058C0G0270J
A5C270	283-0186-00			CAP.,FXD,CER DI:27PF,5%,50V	59660	811A058C0G0270J
A5C280	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A5C281	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A5C282	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	04222	MA101C271KAA
A5C310	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A5C323	281-0862-00			CAP.,FXD,CER DI:0.001UF,+80-20%,100V	96733	ADIVSE
A5C330	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A5C350	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A5C352	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	04222	SR302E105ZAA
A5C360	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A5C380	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	55680	ULA1A101TEA
A5C381	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	04222	MA101C271KAA
A5C382	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A5C421	283-0158-00	B010100	B050483	CAP.,FXD,CER DI:1PF,10%,50V	51642	100-050-NP0-109B
A5C421	283-0181-00	B010100	B050483	CAP.,FXD,CER DI:1.8PF,10%,100V	59660	8101B121COKO189B
A5C421	283-0185-00	B010100	B050483	CAP.,FXD,CER DI:2.5PF,5%,50V	96733	T-DG43BY2R5BP
A5C421	283-0140-00	B010100	B050483	CAP.,FXD,CER DI:4.7PF,5%,50V	72982	8101E003A479C
A5C421	----- -----			(C421 SELECTED)		
A5C421	281-0216-00	B050484		CAP.,VAR,CER DI:0.8-6.8PF,400V	52763	311609151
A5C430	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	04222	SR302E105ZAA
A5C431	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A5C450	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A5C451	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A5C452	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	04222	SR302E105ZAA
A5C460	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	04222	SR302E105ZAA
A5C470	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A5C471	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A5C472	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	04222	SR302E105ZAA
A5C480	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A5C486	283-0158-00	B010100	B050483	CAP.,FXD,CER DI:1PF,10%,50V	51642	100-050-NP0-109B
A5C486	283-0181-00	B010100	B050483	CAP.,FXD,CER DI:1.8PF,10%,100V	59660	8101B121COKO189B
A5C486	283-0185-00	B010100	B050483	CAP.,FXD,CER DI:2.5PF,5%,50V	96733	T-DG43BY2R5BP
A5C486	283-0140-00	B010100	B050483	CAP.,FXD,CER DI:4.7PF,5%,50V	72982	8101E003A479C
A5C486	----- -----			(C486 SELECTED)		
A5C486	281-0216-00	B050484		CAP.,VAR,CER DI:0.8-6.8PF,400V	52763	311609151
A5C520	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A5C521	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A5C531	281-0798-00	B010100	B019999	CAP.,FXD,CER DI:51PF,1%,100V	96733	R2928
A5C531	281-0765-00	B020000	B050595	CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710-100NP0101J
A5C531	281-0786-00	B050596		CAP.,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A5C532	283-0024-00	B020000		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	31433	C322C104M5R5CA
A5C540	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	31433	C322C104M5R5CA
A5C541	281-0798-00	B010100	B019999	CAP.,FXD,CER DI:51PF,1%,100V	96733	R2928
A5C541	281-0765-00	B020000	B050595	CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710-100NP0101J
A5C541	281-0786-00	B050596		CAP.,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A5C550	281-0758-00			CAP.,FXD,CER DI:15PF,20%,100V	04222	MA101A150MA

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A5C551	281-0758-00			CAP.,FXD,CER DI:15PF,20%,100V	04222	MA101A150MAA
A5C560	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A5C562	281-0758-00			CAP.,FXD,CER DI:15PF,20%,100V	04222	MA101A150MAA
A5C563	281-0758-00			CAP.,FXD,CER DI:15PF,20%,100V	04222	MA101A150MAA
A5C564	283-0024-00	B020000		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	31433	C322C104M5R5CA
A5C570	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	31433	C322C104M5R5CA
A5C571	281-0798-00	B010100	B019999	CAP.,FXD,CER DI:51PF,1%,100V	96733	R2928
A5C571	281-0765-00	B020000	B050595	CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710-100NP0101J
A5C571	281-0786-00	B050596		CAP.,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A5C572	281-0798-00	B010100	B019999	CAP.,FXD,CER DI:51PF,1%,100V	96733	R2928
A5C572	281-0765-00	B020000	B050595	CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710-100NP0101J
A5C572	281-0786-00	B050596		CAP.,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A5C583	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A5C584	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A5C630	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C631	281-0851-00			CAP.,FXD,CER DI:180PF,5%,100VDC	04222	MA101A181JAA
A5C632	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A5C633	281-0759-00	B010100	B050730	CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A5C660	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C670	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C682	281-0759-00	B010100	B050730	CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A5C683	281-0851-00			CAP.,FXD,CER DI:180PF,5%,100VDC	04222	MA101A181JAA
A5C684	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A5C720	281-0863-00			CAP.,FXD CER DI:240PF,5%,100V	04222	GC101A241J
A5C740	281-0863-00			CAP.,FXD CER DI:240PF,5%,100V	04222	GC101A241J
A5C760	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C770	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C780	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C850	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A5C851	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A5C860	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A5C861	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A5C880	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C921	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A5C922	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A5C923	283-0771-00			CAP.,FXD,MICA D:334PF,1%,500V	00853	D15-5F3340F0
A5C930	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	04222	SR302E105ZAA
A5C931	290-0920-00			CAP.,FXD,ELCTLT:33UF,+50-10%,35V	55680	ULB1V330TEAANA
A5C932	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	04222	SR302E105ZAA
A5C950	283-0671-00			CAP.,FXD,MICA D:164PF,1%,500V	00853	D155F1640F0
A5C960	290-0920-00			CAP.,FXD,ELCTLT:33UF,+50-10%,35V	55680	ULB1V330TEAANA
A5C972	281-0864-00			CAP.,FXD,CER DI:430PF,5%,100V	12969	CGD431JEN
A5C980	290-0920-00			CAP.,FXD,ELCTLT:33UF,+50-10%,35V	55680	ULB1V330TEAANA
A5C1020	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	04222	SR302E105ZAA
A5C1021	281-0770-00			CAP.,FXD,CER DI:1000 PF,20%,100V	96733	R2745
A5C1040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C1081	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A5CR230	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR251	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR252	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR273	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR520	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR530	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR531	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)

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A5CR541	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR550	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A5CR551	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A5CR562	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A5CR563	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A5CR571	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR572	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR583	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR584	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR830	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR831	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR834	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR846	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR910	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A5CR1012	152-0066-00			SEMICOND DVC DI:RECT,SI,400V,1A,D0-41	05828	GP10G-020
A5CR1030	152-0066-00			SEMICOND DVC DI:RECT,SI,400V,1A,D0-41	05828	GP10G-020
A5J100	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A5J100	----- -----			(QUANTITY OF 4)		
A5J1051	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A5J1051	----- -----			(QUANTITY OF 4)		
A5L320	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A5L380	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A5L381	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A5L430	108-0740-00			TRANSFORMER,RF:225NH	80009	108-0740-00
A5L450	108-0740-00			TRANSFORMER,RF:225NH	80009	108-0740-00
A5L460	108-0740-00			TRANSFORMER,RF:225NH	80009	108-0740-00
A5L472	108-0740-00			TRANSFORMER,RF:225NH	80009	108-0740-00
A5L480	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A5L850	108-0733-00			COIL,RF:FIXED,113NH	80009	108-0733-00
A5L851	108-0733-00			COIL,RF:FIXED,113NH	80009	108-0733-00
A5L860	108-0682-00			COIL,RF:66NH	80009	108-0682-00
A5L861	108-0682-00			COIL,RF:66NH	80009	108-0682-00
A5L910	108-0345-00			COIL,RF:FIXED,1.89UH	80009	108-0345-00
A5L980	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A5L1020	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A5L1080	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A5L1081	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A5L1082	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A5P420	131-0608-00	B050484		TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A5P420	----- -----			(QUANTITY OF 2)		
A5P480	131-0608-00	B050484		TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A5P480	----- -----			(QUANTITY OF 2)		
A5P510	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A5P510	----- -----			(QUANTITY OF 4, JUMPER STORAGE)		
A5Q230	153-0654-00			TRANSISTOR:MATCHED PAIR	80009	153-0654-00
A5Q240	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A5Q250	153-0654-00			TRANSISTOR:MATCHED PAIR	80009	153-0654-00
A5Q260	153-0654-00			TRANSISTOR:MATCHED PAIR	80009	153-0654-00
A5Q261	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A5Q270	153-0654-00			TRANSISTOR:MATCHED PAIR	80009	153-0654-00
A5Q310	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A5Q330	153-0654-00			TRANSISTOR:MATCHED PAIR	80009	153-0654-00
A5Q331	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A5Q340	153-0654-00			TRANSISTOR:MATCHED PAIR	80009	153-0654-00

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A5Q341	153-0654-00			TRANSISTOR:MATCHED PAIR	80009	153-0654-00
A5Q350	153-0654-00			TRANSISTOR:MATCHED PAIR	80009	153-0654-00
A5Q360	153-0654-00			TRANSISTOR:MATCHED PAIR	80009	153-0654-00
A5Q361	153-0654-00			TRANSISTOR:MATCHED PAIR	80009	153-0654-00
A5Q370	153-0654-00			TRANSISTOR:MATCHED PAIR	80009	153-0654-00
A5Q371	153-0654-00			TRANSISTOR:MATCHED PAIR	80009	153-0654-00
A5Q430	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A5Q440	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A5Q441	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A5Q460	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A5Q461	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A5Q480	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A5Q481	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A5Q510	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q511	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q530	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A5Q531	151-0448-00			TRANSISTOR:SILICON,NPN	04713	SRF504
A5Q540	151-0450-00			TRANSISTOR:SILICON,PNP,SEL FROM 2N5583	80009	151-0450-00
A5Q541	151-0448-00			TRANSISTOR:SILICON,NPN	04713	SRF504
A5Q550	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A5Q551	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A5Q552	151-0441-00			TRANSISTOR:SILICON,NPN	04713	SRF501
A5Q553	151-0441-00			TRANSISTOR:SILICON,NPN	04713	SRF501
A5Q560	151-0448-00			TRANSISTOR:SILICON,NPN	04713	SRF504
A5Q561	151-0450-00			TRANSISTOR:SILICON,PNP,SEL FROM 2N5583	80009	151-0450-00
A5Q570	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A5Q571	151-0448-00			TRANSISTOR:SILICON,NPN	04713	SRF504
A5Q610	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q611	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q620	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q621	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q710	151-1054-02			TRANSISTOR:SILICON,FET,N-CHANNEL,SCR	80009	151-1054-02
A5Q720	151-1054-02			TRANSISTOR:SILICON,FET,N-CHANNEL,SCR	80009	151-1054-02
A5Q810	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q811	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q812	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q813	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q814	151-0195-00			TRANSISTOR:SILICON,NPN	04713	SPS8800
A5Q815	151-0195-00			TRANSISTOR:SILICON,NPN	04713	SPS8800
A5Q820	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q821	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q822	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q823	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A5Q824	151-0104-00			TRANSISTOR:SILICON,NPN	49956	TA1075
A5Q830	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A5Q831	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A5Q832	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A5Q833	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A5Q950	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A5Q951	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A5R110	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A5R111	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A5R140	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A5R141	323-0120-00			RES.,FXD,FILM:174 OHM,1%,0.50W	91637	MFF1226G174R0F

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A5R150	323-0120-00			RES.,FXD,FILM:174 OHM,1%,0.50W	91637	MFF1226G174R0F
A5R151	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A5R160	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A5R161	323-0120-00			RES.,FXD,FILM:174 OHM,1%,0.50W	91637	MFF1226G174R0F
A5R170	323-0120-00			RES.,FXD,FILM:174 OHM,1%,0.50W	91637	MFF1226G174R0F
A5R171	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A5R181	321-0201-00			RES.,FXD,FILM:1.21K OHM,1%,0.125W	91637	CMF55116G12100F
A5R182	321-0290-00			RES.,FXD,FILM:10.2K OHM,1%,0.125W	91637	CMF55116G10201F
A5R210	311-2192-00			RES.,VAR,NONWIR:50K OHM,20%,0.25W	32997	7104D-410-503
A5R220	321-0254-00			RES.,FXD,FILM:4.32K OHM,1%,0.125W	91637	MFF1816G43200F
A5R221	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A5R222	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A5R223	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A5R230	321-0159-00			RES.,FXD,FILM:442 OHM,1%,0.125W	91637	CMF55116G442R0F
A5R231	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	57668	NTR25J-E 22E
A5R240	321-0111-00			RES.,FXD,FILM:140 OHM,1%,0.125W	91637	CMF55116G140R0F
A5R241	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A5R242	321-0233-00			RES.,FXD,FILM:2.61K OHM,1%,0.125W	91637	MFF1816G26100F
A5R243	321-0027-00			RES.,FXD,FILM:18.7 OHM,1%,0.125W	91637	CMF110216G18R70F
A5R244	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	57668	NTR25J-E 62E
A5R245	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	57668	NTR25J-E02K4
A5R246	321-0027-00			RES.,FXD,FILM:18.7 OHM,1%,0.125W	91637	CMF110216G18R70F
A5R250	321-0233-00			RES.,FXD,FILM:2.61K OHM,1%,0.125W	91637	MFF1816G26100F
A5R251	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	57668	NTR25J-E 22E
A5R252	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	57668	NTR25J-E 22E
A5R253	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A5R254	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A5R260	321-0111-00			RES.,FXD,FILM:140 OHM,1%,0.125W	91637	CMF55116G140R0F
A5R261	321-0233-00			RES.,FXD,FILM:2.61K OHM,1%,0.125W	91637	MFF1816G26100F
A5R262	321-0027-00			RES.,FXD,FILM:18.7 OHM,1%,0.125W	91637	CMF110216G18R70F
A5R263	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	57668	NTR25J-E 62E
A5R264	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	57668	NTR25J-E02K4
A5R265	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A5R271	321-0027-00			RES.,FXD,FILM:18.7 OHM,1%,0.125W	91637	CMF110216G18R70F
A5R272	321-0233-00			RES.,FXD,FILM:2.61K OHM,1%,0.125W	91637	MFF1816G26100F
A5R273	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	57668	NTR25J-E 22E
A5R280	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A5R281	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A5R310	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A5R311	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A5R312	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A5R320	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	24546	CT55 3011 F
A5R321	321-0297-00			RES.,FXD,FILM:12.1K OHM,1%,0.125W	91637	MFF1816G12101F
A5R322	315-0200-00			RES.,FXD,CMPSN:20 OHM,5%,0.25W	57668	NTR25J-E 20E
A5R323	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	57668	NTR25J-E02K4
A5R324	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A5R325	321-0129-00			RES.,FXD,FILM:215 OHM,1%,0.125W	91637	CMF55116G215R0F
A5R326	321-0285-00			RES.,FXD,FILM:9.09K OHM,1%,0.125W	91637	MFF1816G90900F
A5R330	315-0101-00	B010100	B050595	RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A5R330	315-0201-00	B050596		RES.,FXD,CMPSN:200 OHM,5%,0.25W	57668	NTR25J-E200E
A5R340	315-0150-00			RES.,FXD,CMPSN:15 OHM,5%,0.25W	57668	NTR25J-E 15E
A5R341	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A5R342	315-0560-00			RES.,FXD,CMPSN:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A5R343	315-0560-00			RES.,FXD,CMPSN:56 OHM,5%,0.25W	57668	NTR25J-E56E0

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A5R344	311-1237-00			RES.,VAR,NONWIR:1K OHM,10%,0.50W	32997	3386X-T07-102
A5R350	315-0101-00	B010100	B050595	RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A5R350	315-0201-00	B050596		RES.,FXD,CMPSN:200 OHM,5%,0.25W	57668	NTR25J-E200E
A5R351	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A5R352	315-0101-00	B010100	B050595	RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A5R352	315-0201-00	B050596		RES.,FXD,CMPSN:200 OHM,5%,0.25W	57668	NTR25J-E200E
A5R360	315-0150-00			RES.,FXD,CMPSN:15 OHM,5%,0.25W	57668	NTR25J-E 15E
A5R361	315-0101-00	B010100	B050595	RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A5R361	315-0201-00	B050596		RES.,FXD,CMPSN:200 OHM,5%,0.25W	57668	NTR25J-E200E
A5R362	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A5R363	315-0560-00			RES.,FXD,CMPSN:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A5R370	315-0560-00			RES.,FXD,CMPSN:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A5R371	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A5R372	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A5R373	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A5R374	321-0110-00			RES.,FXD,FILM:137 OHM,1%,0.125W	91637	CMF55116G137R0F
A5R375	321-0308-00			RES.,FXD,FILM:15.8K OHM,1%,0.125W	91637	MFF1816G15801F
A5R376	321-0110-00			RES.,FXD,FILM:137 OHM,1%,0.125W	91637	CMF55116G137R0F
A5R377	311-1237-00			RES.,VAR,NONWIR:1K OHM,10%,0.50W	32997	3386X-T07-102
A5R381	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A5R410	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A5R411	311-1244-00			RES.,VAR,NONWIR:100 OHM,10%,0.50W	32997	3386X-T07-101
A5R420	321-0298-00			RES.,FXD,FILM:12.4K OHM,1%,0.125W	91637	MFF1816G12401F
A5R421	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A5R422	321-0298-00			RES.,FXD,FILM:12.4K OHM,1%,0.125W	91637	MFF1816G12401F
A5R423	321-0119-00			RES.,FXD,FILM:169 OHM,1%,0.125W	91637	CMF55116G169R0F
A5R424	321-0202-00			RES.,FXD,FILM:1.24K OHM,1%,0.125W	91637	CMF55116G12400F
A5R425	321-0329-00			RES.,FXD,FILM:26.1K OHM,1%,0.125W	91637	MFF1816G26101F
A5R426	321-0243-00			RES.,FXD,FILM:3.32K OHM,1%,0.125W	91637	MFF1816G33200F
A5R430	321-0144-00			RES.,FXD,FILM:309 OHM,1%,0.125W	91637	CMF55116G309R0F
A5R431	321-0133-00			RES.,FXD,FILM:237 OHM,1%,0.125W	91637	CMF55116G237R0F
A5R432	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A5R440	321-0115-00			RES.,FXD,FILM:154 OHM,1%,0.125W	91637	CMF55116G154R0F
A5R450	321-0133-00			RES.,FXD,FILM:237 OHM,1%,0.125W	91637	CMF55116G237R0F
A5R451	321-0133-00			RES.,FXD,FILM:237 OHM,1%,0.125W	91637	CMF55116G237R0F
A5R452	321-0277-00			RES.,FXD,FILM:7.5K OHM,1%,0.125W	91637	MFF1816G75000F
A5R453	321-0277-00			RES.,FXD,FILM:7.5K OHM,1%,0.125W	91637	MFF1816G75000F
A5R461	321-0115-00			RES.,FXD,FILM:154 OHM,1%,0.125W	91637	CMF55116G154R0F
A5R470	321-0308-00			RES.,FXD,FILM:15.8K OHM,1%,0.125W	91637	MFF1816G15801F
A5R471	321-0133-00			RES.,FXD,FILM:237 OHM,1%,0.125W	91637	CMF55116G237R0F
A5R480	321-0330-00			RES.,FXD,FILM:26.7K OHM,1%,0.125W	91637	MFF1816G26701F
A5R481	321-0330-00			RES.,FXD,FILM:26.7K OHM,1%,0.125W	91637	MFF1816G26701F
A5R482	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A5R483	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A5R485	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A5R486	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A5R487	321-0129-00			RES.,FXD,FILM:215 OHM,1%,0.125W	91637	CMF55116G215R0F
A5R510	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A5R511	311-1244-00			RES.,VAR,NONWIR:100 OHM,10%,0.50W	32997	3386X-T07-101
A5R522	321-0144-00			RES.,FXD,FILM:309 OHM,1%,0.125W	91637	CMF55116G309R0F
A5R523	321-0202-00			RES.,FXD,FILM:1.24K OHM,1%,0.125W	91637	CMF55116G12400F
A5R524	321-0119-00			RES.,FXD,FILM:169 OHM,1%,0.125W	91637	CMF55116G169R0F
A5R530	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A5R541	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	57668	NTR25J-E220K

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A5R542	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A5R543	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	57668	NTR25J-E 10E0
A5R551	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	57668	NTR25J-E220K
A5R553	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	57668	NTR25J-E 10E0
A5R563	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	57668	NTR25J-E220K
A5R572	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	57668	NTR25J-E220K
A5R580	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	57668	NTR25J-E220K
A5R581	315-0333-00			RES.,FXD,CMPSN:33K OHM,5%,0.25W	57668	NTR25J-E33K0
A5R582	315-0333-00			RES.,FXD,CMPSN:33K OHM,5%,0.25W	57668	NTR25J-E33K0
A5R610	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A5R611	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A5R612	321-0168-00			RES.,FXD,FILM:549 OHM,1%,0.125W	91637	CMF55116G549R0F
A5R613	321-0200-00			RES.,FXD,FILM:1.18K OHM,1%,0.125W	91637	CMF55116G11800F
A5R614	321-0200-00			RES.,FXD,FILM:1.18K OHM,1%,0.125W	91637	CMF55116G11800F
A5R615	321-0168-00			RES.,FXD,FILM:549 OHM,1%,0.125W	91637	CMF55116G549R0F
A5R620	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A5R621	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A5R622	321-0168-00			RES.,FXD,FILM:549 OHM,1%,0.125W	91637	CMF55116G549R0F
A5R623	321-0200-00			RES.,FXD,FILM:1.18K OHM,1%,0.125W	91637	CMF55116G11800F
A5R625	321-0200-00			RES.,FXD,FILM:1.18K OHM,1%,0.125W	91637	CMF55116G11800F
A5R626	321-0168-00			RES.,FXD,FILM:549 OHM,1%,0.125W	91637	CMF55116G549R0F
A5R630	315-0510-00	B010100	B050730	RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A5R631	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	57668	NTR25J-E150E
A5R632	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	57668	NTR25J-E150E
A5R650	321-0437-00			RES.,FXD,FILM:348K OHM,1%,0.125W	91637	CMF55116G34802F
A5R680	321-0298-00			RES.,FXD,FILM:12.4K OHM,1%,0.125W	91637	MFF1816G12401F
A5R681	321-0298-00			RES.,FXD,FILM:12.4K OHM,1%,0.125W	91637	MFF1816G12401F
A5R682	315-0510-00	B010100	B050730	RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A5R683	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	57668	NTR25J-E150E
A5R684	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	57668	NTR25J-E150E
A5R710	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A5R711	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A5R712	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A5R713	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A5R720	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A5R721	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A5R722	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A5R723	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A5R730	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A5R731	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A5R732	321-0296-00			RES.,FXD,FILM:11.8K OHM,1%,0.125W	91637	MFF1816G11801F
A5R733	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A5R740	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A5R742	321-0296-00			RES.,FXD,FILM:11.8K OHM,1%,0.125W	91637	MFF1816G11801F
A5R743	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A5R750	307-0540-00	B010100	B050483	RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	57924	4306R-101-102
A5R750	307-0541-00	B050484		RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	MSP08A01-102G
A5R770	307-0539-00			RES NTWK,THK FI:(7)510 OHM,10%,1W	32997	4308R-101-511
A5R820	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A5R821	321-0130-00			RES.,FXD,FILM:221 OHM,1%,0.125W	91637	MFF1816G221R0F
A5R822	321-0262-00			RES.,FXD,FILM:5.23K OHM,1%,0.125W	91637	MFF1816G52300F
A5R831	321-0304-00			RES.,FXD,FILM:14.3K OHM,1%,0.125W	91637	MFF1816G14301F
A5R832	321-0172-00			RES.,FXD,FILM:604 OHM,1%,0.125W	91637	CMF55116G604R0F
A5R835	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	57668	NTR25J-E 15K

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A5R840	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	57668	NTR25J-E 15K
A5R841	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A5R842	321-0147-00			RES.,FXD,FILM:332 OHM,1%,0.125W	91637	CMF55116G332R0F
A5R843	321-0300-00			RES.,FXD,FILM:13K OHM,1%,0.125W	91637	MFF1816G13001F
A5R844	321-0206-00			RES.,FXD,FILM:1.37K OHM,1%,0.125W	91637	MFF1816G13700F
A5R845	321-0147-00			RES.,FXD,FILM:332 OHM,1%,0.125W	91637	CMF55116G332R0F
A5R846	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A5R850	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A5R870	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A5R871	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A5R880	315-0102-00	B010100	B050483	RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R881	315-0102-00	B010100	B050483	RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R882	315-0102-00	B010100	B050483	RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R920	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A5R921	321-0138-00			RES.,FXD,FILM:267 OHM,1%,0.125W	91637	CMF55116G267R0F
A5R922	321-0138-00			RES.,FXD,FILM:267 OHM,1%,0.125W	91637	CMF55116G267R0F
A5R923	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A5R931	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	57668	NTR25J-E180E
A5R940	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	57668	NTR25J-E180E
A5R950	315-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	57668	NTR25J-E 1K1
A5R960	315-0163-00			RES.,FXD,CMPSN:16K OHM,5%,0.25W	57668	NTR25J-E16K0
A5R961	315-0363-00			RES.,FXD,CMPSN:36K OHM,5%,0.25W	57668	NTR25J-E36K0
A5R962	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A5R963	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A5R970	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A5R972	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	57668	NTR25J-E150E
A5R980	321-0241-00			RES.,FXD,FILM:3.16K OHM,1%,0.125W	91637	MFF1816G31600F
A5R981	321-0219-00			RES.,FXD,FILM:1.87K OHM,1%,0.125W	91637	MFF1816G18700F
A5R982	321-0260-00			RES.,FXD,FILM:4.99K OHM,1%,0.125W	91637	MFF1816G49900F
A5R983	321-0241-00			RES.,FXD,FILM:3.16K OHM,1%,0.125W	91637	MFF1816G31600F
A5R1011	321-0362-00			RES.,FXD,FILM:57.6K OHM,1%,0.125W	91637	CMF55116G57601F
A5R1020	321-0260-00			RES.,FXD,FILM:4.99K OHM,1%,0.125W	91637	MFF1816G49900F
A5R1030	321-0084-00			RES.,FXD,FILM:73.2 OHM,1%,0.125W	91637	CMF55116G73R20F
A5R1031	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A5R1040	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A5R1041	315-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	57668	NTR25J-E 1K1
A5R1051	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	57668	NTR25J-E330E
A5R1052	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A5R1053	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A5R1070	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A5R1071	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A5R1080	321-0339-00			RES.,FXD,FILM:33.2K OHM,1%,0.125W	91637	MFF1816G33201F
A5R1081	321-0339-00			RES.,FXD,FILM:33.2K OHM,1%,0.125W	91637	MFF1816G33201F
A5RT830	307-0250-00			RES.,THERMAL:390 OHM,10%	15454	DG125390K
A5U220	156-0644-00			MICROCIRCUIT,DI:QUAD BILATERAL SWITCH	80009	156-0644-00
A5U280	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	LM358J
A5U320	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	LM358J
A5U420	156-0158-07			MICROCIRCUIT,LI:DUAL OPNL AMPL,SCREENED	01295	MC1458JG4
A5U440	156-1593-00			MICROCIRCUIT,DI:455/910 BIT ANALOG SHIFT	07263	SL92104
A5U460	156-1593-00			MICROCIRCUIT,DI:455/910 BIT ANALOG SHIFT	07263	SL92104
A5U630	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S10
A5U650	156-0419-02			MICROCIRCUIT,DI:DUAL 4 INP NAND LINE DRVR	07263	74S140
A5U651	156-0316-04			MICROCIRCUIT,DI:QUAD ECL TO TTL TRANS	04713	MC10125PD/LD
A5U670	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S10

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A5U671	156-0180-04			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00NP3
A5U730	156-0158-07			MICROCIRCUIT,LI:DUAL OPNL AMPL,SCREENED	01295	MC1458JG4
A5U740	156-0158-07			MICROCIRCUIT,LI:DUAL OPNL AMPL,SCREENED	01295	MC1458JG4
A5U750	156-0229-01			MICROCIRCUIT,DI:DUAL 4/5 INP OR NOR GATE	04713	MC10109PD/LD
A5U770	156-0229-01			MICROCIRCUIT,DI:DUAL 4/5 INP OR NOR GATE	04713	MC10109PD/LD
A5U850	156-0158-07			MICROCIRCUIT,LI:DUAL OPNL AMPL,SCREENED	01295	MC1458JG4
A5U870	156-1214-01			MICROCIRCUIT,DI:DUAL 2 WIDE,3 IN.OR GATE	04713	SC22689
A5U871	156-0860-02			MICROCIRCUIT,DI:TRIPLE LINE RECEIVER,SCRN	04713	MC10116PD/LD
A5U930	156-1590-00			MICROCIRCUIT,LI:A/D CONV,400NS	01281	TDS5318
A5U950	156-0158-07			MICROCIRCUIT,LI:DUAL OPNL AMPL,SCREENED	01295	MC1458JG4
A5U960	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A5U1050	156-0514-01			MICROCIRCUIT,DI:DIFF 4-CHANNEL MUX,SEL	80009	156-0514-01
A5VR1010	152-0317-00			SEMICOND DEVICE:ZENER,0.25W,6.2V,5%	04713	SZG20012
A5W630	131-0566-00	B050731		BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A5W651	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A5W671	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A5W682	131-0566-00	B050731		BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A6	670-7320-00	B010100	B040399	CKT BOARD ASSY:DISPLAY	80009	670-7320-00
A6	670-7320-01	B040400	B061194	CKT BVOARD ASSY:DISPLAY	80009	670-7320-01
A6	670-7320-02	B061195	B063249	CKT BOARD ASSY:DISPLAY	80009	670-7320-02
A6	670-7320-03	B063250		CKT BOARD ASSY:DISPLAY	80009	670-7320-03
A6C100	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C103	281-0863-00	B020000		CAP.,FXD CER DI:240PF,5%,100V	04222	GC101A241J
A6C120	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C210	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C220	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C410	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A6C411	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C511	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C600	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C711	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C712	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C801	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A6C810	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C811	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C820	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A6C920	290-0778-00			CAP.,FXD,ELCTLT:1UF,+50-10%,50V	55680	UEB1H010MAA1TD
A6C1011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C1020	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C1210	283-0665-00			CAP.,FXD,MICA D:190PF,1%,100V	00853	D155F191F0
A6C1211	283-0636-00			CAP.,FXD,MICA D:36PF,1.4%,100V	00853	D155E360G0
A6C1220	283-0665-00			CAP.,FXD,MICA D:190PF,1%,100V	00853	D155F191F0
A6C1221	283-0636-00			CAP.,FXD,MICA D:36PF,1.4%,100V	00853	D155E360G0
A6C1315	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C1316	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C1317	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C1325	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C1420	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A6C1520	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A6C1521	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A6C1600	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C1620	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A6C1621	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A6CR710	152-0322-00	B063250		SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A6CR711	152-0322-00	B063250		SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A6CR916	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR920	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR1119	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR1322	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6L1210	108-0240-00			COIL,RF:FIXED,820UH	76493	B5147
A6L1220	108-0240-00			COIL,RF:FIXED,820UH	76493	B5147
A6L1420	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A6L1520	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A6L1521	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A6L1620	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A6L1621	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A6Q300	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A6Q1001	151-0188-03			TRANSISTOR:SILICON,PNP,SEL	80009	151-0188-03
A6Q1015	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A6R100	307-0651-00			RES NTWK,FXD FI:5,3.3K OHM,5%,0.15W	01121	206A332
A6R101	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A6R102	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A6R103	321-0202-00			RES.,FXD,FILM:1.24K OHM,1%,0.125W	91637	CMF55116G12400F
A6R105	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R120	307-0651-00			RES NTWK,FXD FI:5,3.3K OHM,5%,0.15W	01121	206A332
A6R205	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A6R210	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A6R211	321-0220-00			RES.,FXD,FILM:1.91K OHM,1%,0.125W	91637	MFF1816G19100F
A6R410	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R710	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A6R711	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	57668	NTR25J-E02K4
A6R712	321-0267-00			RES.,FXD,FILM:5.9K OHM,1%,0.125W	91637	MFF1816G59000F
A6R714	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A6R715	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R801	321-0248-00			RES.,FXD,FILM:3.74K OHM,1%,0.125W	91637	CMF55116G37400F
A6R802	321-0215-00			RES.,FXD,FILM:1.69K OHM,1%,0.125W	91637	MFF1816G16900F
A6R820	321-0285-00			RES.,FXD,FILM:9.09K OHM,1%,0.125W	91637	MFF1816G90900F
A6R821	321-0285-00			RES.,FXD,FILM:9.09K OHM,1%,0.125W	91637	MFF1816G90900F
A6R822	321-0211-00			RES.,FXD,FILM:1.54K OHM,1%,0.125W	91637	MFF1816G15400F
A6R900	311-1248-00			RES.,VAR,NONWIR:500 OHM,10%,0.50W	73138	72-23-0
A6R903	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A6R904	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A6R905	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A6R906	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	57668	NTR25J-E620E
A6R907	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R908	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A6R909	321-0189-00			RES.,FXD,FILM:909 OHM,1%,0.125W	91637	CMF55116G909R0F
A6R910	321-0093-00			RES.,FXD,FILM:90.9 OHM,1%,0.125W	91637	MFF1816G90R90F
A6R911	321-0260-00			RES.,FXD,FILM:4.99K OHM,1%,0.125W	91637	MFF1816G49900F
A6R912	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A6R913	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A6R914	321-0612-00			RES.,FXD,FILM:500 OHM,1%,0.125W	91637	MFF1816G500R0F
A6R915	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A6R916	321-0342-00			RES.,FXD,FILM:35.7K OHM,1%,0.125W	91637	MFF1816G35701F
A6R917	315-0201-00	B010100	B061194	RES.,FXD,CMPSN:200 OHM,5%,0.25W	57668	NTR25J-E200E
A6R917	315-0471-00	B061195		RES.,FXD,CMPSN:470 OHM,5%,0.25W	57668	NTR25J-E470E
A6R918	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A6R920	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A6R921	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A6R1000	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A6R1001	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R1002	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A6R1005	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	57668	NTR25J-E75K0
A6R1006	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R1007	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	57668	NTR25J-E75K0
A6R1120	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R1121	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A6R1122	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A6R1200	321-0181-00			RES.,FXD,FILM:750 OHM,1%,0.125W	91637	CMF55116G750R0F
A6R1201	321-0135-00			RES.,FXD,FILM:249 OHM,1%,0.125W	91637	CMF55116G249R0F
A6R1202	321-0164-00			RES.,FXD,FILM:499 OHM,1%,0.125W	91637	CMF55116G499R0F
A6R1203	321-0164-00			RES.,FXD,FILM:499 OHM,1%,0.125W	91637	CMF55116G499R0F
A6R1204	321-0039-00			RES.,FXD,FILM:24.9 OHM,1%,0.125W	91637	CMF55116G24R90F
A6R1205	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	57668	NTR25J-E220E
A6R1207	321-0162-00			RES.,FXD,FILM:475 OHM,1%,0.125W	91637	CMF55116G475R0F
A6R1210	321-0229-00			RES.,FXD,FILM:2.37K OHM,1%,0.125W	24546	CT552371F

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A6R1220	321-0229-00			RES.,FXD,FILM:2.37K OHM,1%,0.125W	24546	CT552371F
A6R1221	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R1222	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R1223	315-0134-00			RES.,FXD,CMPSN:130K OHM,5%,0.25W	57668	NTR25J-E130K
A6R1310	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R1315	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	57668	NTR25J-E02K4
A6R1323	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A6R1324	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6R1325	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A6R1410	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R1411	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R1412	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R1413	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R1414	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R1415	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R1416	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R1417	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R1418	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R1421	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A6R1500	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A6U100	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A6U120	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR	01295	SN74LS393
A6U150	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A6U200	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A6U210	156-0465-02			MICROCIRCUIT,DI:8 INP NAND GATE	01295	SN74LS30NP3
A6U220	156-1258-01			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A6U300	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A6U310	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3
A6U320	156-1045-01			MICROCIRCUIT,DI:QUAD 2 INPUT MUX W/STORAGE	80009	156-1045-01
A6U400	156-0733-02			MICROCIRCUIT,DI:DUAL MONOSTABLE MV,SCRN	01295	SN74LS221N3
A6U410	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A6U420	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A6U500	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A6U510	156-0465-02			MICROCIRCUIT,DI:8 INP NAND GATE	01295	SN74LS30NP3
A6U520	156-1045-01			MICROCIRCUIT,DI:QUAD 2 INPUT MUX W/STORAGE	80009	156-1045-01
A6U600	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A6U610	156-0927-03			MICROCIRCUIT,LI:DIGITAL/ANALOG CONVERTER	80009	156-0927-03
A6U620	156-1045-01			MICROCIRCUIT,DI:QUAD 2 INPUT MUX W/STORAGE	80009	156-1045-01
A6U700	156-1555-00			MICROCIRCUIT,LI:D/A CONVERTER	34335	AM6080PC
A6U720	156-0927-03			MICROCIRCUIT,LI:DIGITAL/ANALOG CONVERTER	80009	156-0927-03
A6U800	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A6U810	156-0513-02			MICROCIRCUIT,DI:8-CHANNEL MUX,SEL	80009	156-0513-02
A6U820	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A6U905	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A6U1010	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A6U1020	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A6U1100	156-0513-02			MICROCIRCUIT,DI:8-CHANNEL MUX,SEL	80009	156-0513-02
A6U1215	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A6U1300	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A6U1305	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A6U1315	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A6U1325	156-1191-01			MICROCIRCUIT,LI:DUAL BI-FET OP-AMP,8 DIP	01295	TL072ACP3
A6U1400	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A6U1500	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A6U1510	156-0513-02			MICROCIRCUIT,DI:8-CHANNEL MUX,SEL	80009	156-0513-02
A6U1600	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04

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A7	670-7321-00	B010100	B061194	CKT BOARD ASSY:POWER SUPPLY	80009	670-7321-00
A7	670-7321-01	B061195		CKT BOARD ASSY:POWER SUPPLY	80009	670-7321-01
A7C110	290-0701-00			CAP.,FXD,ELCTLT:470UF,40%,16VDC	90201	TTX471U0161E1A3P
A7C130	290-0770-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	54473	ECE-A25V100L
A7C150	290-0770-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	54473	ECE-A25V100L
A7C211	281-0770-00			CAP.,FXD,CER DI:1000 PF,20%,100V	96733	R2745
A7C221	281-0707-00	B010100	B063299	CAP.,FXD,CER DI:15000PF,20%,100V	20932	402EM200AD153K
A7C221	281-0707-01	B063300		CAP.,FXD,CER DI:15000PF,20%,100V	04222	MA201C153MAA
A7C230	283-0178-00			CAP.,FXD,CER DI:0.1UF,+80-20%,100V	04222	ADVISE
A7C231	281-0770-00			CAP.,FXD,CER DI:1000 PF,20%,100V	96733	R2745
A7C250	290-0818-02			CAP.,FXD,ELCTLT:390UF,+100-10%,40V	00853	301AER391U04083
A7C310	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A7C311	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A7C312	283-0594-00			CAP.,FXD,MICA D:0.001UF,1%,100V	00853	D151F102F0
A7C360	290-0932-00			CAP.,FXD ELECT:390UF,+ 100-10%,15VDC	56289	6720676
A7C410	283-0339-00			CAP.,FXD,CER DI:0.22UF.10%,50V	51642	300 050X5R224K
A7C416	283-0339-00			CAP.,FXD,CER DI:0.22UF.10%,50V	51642	300 050X5R224K
A7C420	290-0964-00			CAP.,FXD,ELCTLT:1200UF,+100-10%,12V	90201	VPR122N012E1L1J
A7C430	290-0964-00			CAP.,FXD,ELCTLT:1200UF,+100-10%,12V	90201	VPR122N012E1L1J
A7C450	290-0932-00			CAP.,FXD ELECT:390UF,+ 100-10%,15VDC	56289	6720676
A7C451	290-0932-00			CAP.,FXD ELECT:390UF,+ 100-10%,15VDC	56289	6720676
A7C510	290-0932-00			CAP.,FXD ELECT:390UF,+ 100-10%,15VDC	56289	6720676
A7C550	290-0932-00			CAP.,FXD ELECT:390UF,+ 100-10%,15VDC	56289	6720676
A7C640	283-0212-00			CAP.,FXD,CER DI:2UF,20%,50V	51642	400-050-Z5U205M
A7C650	290-0932-00			CAP.,FXD ELECT:390UF,+ 100-10%,15VDC	56289	6720676
A7C750	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	55680	ULA1C470TEA
A7C760	281-0770-00			CAP.,FXD,CER DI:1000 PF,20%,100V	96733	R2745
A7C763	281-0770-00			CAP.,FXD,CER DI:1000 PF,20%,100V	96733	R2745
A7C764	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	04222	SR302E105ZAA
A7C810	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A7C811	290-0771-00			CAP.,FXD,ELCTLT:220UF,+50-10%,10VDC	56289	502D231
A7C840	290-0771-00			CAP.,FXD,ELCTLT:220UF,+50-10%,10VDC	56289	502D231
A7C850	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A7CR110	152-0107-00			SEMICOND DEVICE:SILICON,400V,400MA	12969	G727
A7CR230	152-0107-00			SEMICOND DEVICE:SILICON,400V,400MA	12969	G727
A7CR232	152-0333-00			SEMICOND DVC DI:SW,SI,55V,200MA,D0-35	03508	DJ2011
A7CR250	152-0066-00	B061195		SEMICOND DVC DI:RECT,SI,400V,1A,D0-41	05828	GP10G-020
A7CR311	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A7CR340	152-0581-00			SEMICOND DEVICE:SILICON,20V,1A	04713	1N5817
A7CR350	152-0754-00			SEMICOND DEVICE:RECT,SI,SCHOTTKY,40V,8A	81483	95-4421
A7CR419	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A7CR640	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A7CR761	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A7L140	108-0422-00			COIL,RF:FIXED,82UH	80009	108-0422-00
A7L150	108-0422-00			COIL,RF:FIXED,82UH	80009	108-0422-00
A7L230	108-0813-00			COIL,RF:10UH	80009	108-0813-00
A7L250	108-0813-00			COIL,RF:10UH	80009	108-0813-00
A7L330	108-0556-00			COIL,RF:12UH	80009	108-0556-00
A7L450	108-0813-00			COIL,RF:10UH	80009	108-0813-00
A7LR670	108-0184-00			COIL,RF:3.2UH(WOUND ON A 10 OHM RES	80009	108-0184-00
A7Q220	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A7Q230	151-0124-00			TRANSISTOR:SILICON,NPN,SEL FROM 2N3501	04713	SM8138
A7Q330	151-0701-00			TRANSISTOR:SILICON,NPN	80009	151-0701-00

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A7Q630	151-0192-00			TRANSISTOR:SELECTED	04713	SPS8801
A7Q641	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A7Q650	151-0426-00			TRANSISTOR:SILICON,NPN	03508	X44H242
A7Q660	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A7R210	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A7R211	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	57668	NTR25J-E470E
A7R220	307-0106-00			RES.,FXD,CMPSN:4.7 OHM,5%,0.25W	01121	CB47G5
A7R221	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A7R231	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A7R250	315-0473-00	B061195		RES.,FXD,CMPSN:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A7R310	321-0172-00			RES.,FXD,FILM:604 OHM,1%,0.125W	91637	CMF55116G604R0F
A7R311	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	57668	NTR25J-E470E
A7R312	321-0337-00			RES.,FXD,FILM:31.6K OHM,1%,0.125W	91637	MFF1816G31601F
A7R313	321-0260-00			RES.,FXD,FILM:4.99K OHM,1%,0.125W	91637	MFF1816G49900F
A7R314	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A7R315	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A7R316	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A7R330	301-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.5W	57668	TR50J-E 47E
A7R331	308-0678-00			RES.,FXD,WW:0.1 OHM,5%,2W	75042	BWH-R1000J
A7R410	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A7R411	321-0604-00			RES.,FXD,FILM:30K OHM,0.25%,0.125W	91637	MFF1816D30001C
A7R412	321-0743-02			RES.,FXD,FILM:16.26K OHM,0.5%,0.125W	91637	CMF110216D16261D
A7R413	315-0913-00			RES.,FXD,CMPSN:91K OHM,5%,0.25W	57668	NTR25J-E 91K
A7R414	321-0260-00			RES.,FXD,FILM:4.99K OHM,1%,0.125W	91637	MFF1816G49900F
A7R415	321-0327-00			RES.,FXD,FILM:24.9K OHM,1%,0.125W	91637	MFF1816G24901F
A7R416	321-0692-00			RES.,FXD,FILM:49.9K OHM,0.5%,0.125W	91637	MFF1816G49901D
A7R417	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A7R419	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	57668	NTR25J-E620E
A7R610	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A7R611	321-0251-00			RES.,FXD,FILM:4.02K OHM,1%,0.125W	91637	MFF1816G40200F
A7R612	321-0293-00			RES.,FXD,FILM:11K OHM,1%,0.125W	91637	MFF1816G11001F
A7R613	321-0251-00			RES.,FXD,FILM:4.02K OHM,1%,0.125W	91637	MFF1816G40200F
A7R614	321-0293-00			RES.,FXD,FILM:11K OHM,1%,0.125W	91637	MFF1816G11001F
A7R615	321-0251-00			RES.,FXD,FILM:4.02K OHM,1%,0.125W	91637	MFF1816G40200F
A7R616	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A7R617	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A7R618	321-0251-00			RES.,FXD,FILM:4.02K OHM,1%,0.125W	91637	MFF1816G40200F
A7R620	321-0251-00			RES.,FXD,FILM:4.02K OHM,1%,0.125W	91637	MFF1816G40200F
A7R621	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A7R622	321-0251-00			RES.,FXD,FILM:4.02K OHM,1%,0.125W	91637	MFF1816G40200F
A7R623	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A7R630	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A7R631	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A7R640	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A7R641	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A7R642	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A7R650	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A7R651	308-0678-00			RES.,FXD,WW:0.1 OHM,5%,2W	75042	BWH-R1000J
A7R652	323-0063-00			RES.,FXD,FILM:44.2 OHM,1%,0.5W	91637	CMF65116G44R20F
A7R653	322-0617-00			RES.,FXD,FILM:47.7 OHM,1%,0.25W	19701	MF52C47R70F
A7R660	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A7R661	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A7R662	321-0377-00			RES.,FXD,FILM:82.5K OHM,1%,0.125W	91637	MFF1816G82501F
A7R663	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F

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A7R664	321-0189-00			RES.,FXD,FILM:909 OHM,1%,0.125W	91637	CMF55116G909R0F
A7R724	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A7R760	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A7R761	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A7R762	321-0924-02			RES.,FXD,FILM:40K OHM,0.5%,0.125W	24546	NE55 4002 B
A7R763	321-0318-02			RES.,FXD,FILM:20K OHM,0.5%,0.125W	91637	CMF55116D20001D
A7R870	307-0106-00			RES.,FXD,CMPSN:4.7 OHM,5%,0.25W	01121	CB47G5
A7R871	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A7R872	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A7R873	307-0106-00			RES.,FXD,CMPSN:4.7 OHM,5%,0.25W	01121	CB47G5
A7R874	307-0106-00			RES.,FXD,CMPSN:4.7 OHM,5%,0.25W	01121	CB47G5
A7R875	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A7R876	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A7R877	307-0106-00			RES.,FXD,CMPSN:4.7 OHM,5%,0.25W	01121	CB47G5
A7RT653	307-0126-00			RES.,THERMAL:100 OHM,10%	14193	2D21-101-D
A7T340	120-1356-00			XFMR,PWR,STPDN:HF CONVERTOR	80009	120-1356-00
A7U220	156-0277-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	07263	MICROA7805UC
A7U310	156-1225-01			MICROCIRCUIT,LI:DUAL COMPARATOR,SCREENED	27014	LM393N/A+
A7U610	156-0513-02			MICROCIRCUIT,DI:8-CHANNEL MUX,SEL	80009	156-0513-02
A7U640	156-0206-02			MICROCIRCUIT,DI:CORE DRIVER,SCREENED	01295	SN75325(NP3 OR J
A7U660	156-1191-01			MICROCIRCUIT,LI:DUAL BI-FET OP-AMP,8 DIP	01295	TL072ACP3
A7U710	156-0682-02			MICROCIRCUIT,DI:HEX D FLIP-FLOP,SEL	27014	MM74C174
A7U711	156-0682-02			MICROCIRCUIT,DI:HEX D FLIP-FLOP,SEL	27014	MM74C174
A7U740	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A7U741	156-0206-02			MICROCIRCUIT,DI:CORE DRIVER,SCREENED	01295	SN75325(NP3 OR J
A7U840	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A7VR230	152-0749-00			SEMICOND DEVICE:ZEN,SI,82V,5%,5W	04713	SZP40096
A7VR419	152-0168-00			SEMICOND DEVICE:ZENER,0.4W,12V,5%	04713	SZG35009K4

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A8	670-7322-00			CKT BOARD ASSY:MEMORY	80009	670-7322-00
A8C200	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C210	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C310	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C320	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C400	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C410	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C510	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C520	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C610	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C700	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C710	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C810	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C910	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C920	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1000	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1020	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1110	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1410	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1420	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1600	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C1720	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A8C1721	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A8CR1621	152-0066-00			SEMICOND DVC DI:RECT,SI,400V,1A,D0-41	05828	GP10G-020
A8L1720	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A8L1721	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A8R320	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8R625	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8R720	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8R1125	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8R1225	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8R1310	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8R1620	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A8U200	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A8U210	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A8U220	156-0452-02			MICROCIRCUIT,DI:4-WIDE,2-INP AOI,SCREENED	01295	SN74LS54 NP3/JP4
A8U300	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A8U310	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A8U320	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74LS1759NP3 OR
A8U400	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A8U410	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A8U420	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A8U500	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A8U510	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A8U600	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A8U610	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A8U620	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A8U700	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A8U710	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A8U720	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A8U800	156-0989-02			MICROCIRCUIT,DI:4 X 4 RGTR FILE,BURN-IN	04713	SN74LS670NDS
A8U810	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A8U820	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A8U900	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A8U910	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A8U920	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A8U1000	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A8U1010	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A8U1020	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A8U1100	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A8U1110	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A8U1120	156-0953-02			MICROCIRCUIT,DI:4 BIT MAGNITUDE CMPRTR	01295	SN74LS85
A8U1210	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A8U1220	156-0874-02			MICROCIRCUIT,DI:8 BIT ADDRESSABLE LCH	04713	SN74LS259
A8U1310	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A8U1320	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A8U1410	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A8U1420	156-0381-02			MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A8U1510	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	04713	SN74LS373 ND/JD
A8U1520	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A8U1600	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A8U1700	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A8VR1620	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A8VR1720	152-0732-00			SEMICOND DEVICE:ZENER,1.5W,3.3V,5%	04713	IN5913B

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A9	670-7323-00	B010100	B029999	CKT BOARD ASSY:MPU	80009	670-7323-00
A9	670-7323-01	B030000	B061869	CKT BOARD ASSY:MPU	80009	670-7323-01
A9	670-7323-03	B061369	B061869	CKT BOARD ASSY:MPU	80009	670-7323-03
A9	670-7323-04	B061870	B062199	CKT BOARD ASSY:MPU	80009	670-7323-04
A9	670-7323-05	B062200		CKT BOARD ASSY:MPU	80009	670-7323-05
A9C100	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C101	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C115	281-0812-00	B010100	B061368	CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A9C115	281-0826-00	B061870		CAP.,FXD,CER DI:2200PF,5%,100V	96733	R3207
A9C118	281-0765-00	B010100	B061869	CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710-100NP0101J
A9C211	290-0804-00	B010100	B061869	CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A9C215	290-0782-00	B010100	B061869	CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A9C300	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C310	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C315	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C320	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C325	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C400	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C500	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C510	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C525	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C600	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C610	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C620	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C621	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C622	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C623	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	04222	MA101C271KAA
A9C624	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	04222	MA101A680KAA
A9C715	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C800	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C920	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A9C921	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A9C924	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	55680	ULA1A101TEA
A9C1000	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	55680	ULA1A101TEA
A9C1020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C1021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C1023	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C1024	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9CR118	152-0141-02	B010100	B061869	SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A9CR925	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A9L1010	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A9L1020	120-0407-00			XFMR,TOROID:5 TURNS SINGLE	80009	120-0407-00
A9L1021	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A9L1022	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A9L1023	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A9L1024	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A9Q211	151-0221-00	B061870		TRANSISTOR:SILICON,PNP	04713	SPS246
A9R110	315-0181-00	B010100	B061869	RES.,FXD,CMPSN:180 OHM,5%,0.25W	57668	NTR25J-E180E
A9R110	315-0472-00	B061870		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A9R115	315-0561-00	B010100	B061869	RES.,FXD,CMPSN:560 OHM,5%,0.25W	57668	NTRERJ-E 560E
A9R115	315-0224-00	B061870		RES.,FXD,CMPSN:220K OHM,5%,0.25W	57668	NTR25J-E220K
A9R116	315-0361-00	B010100	B061869	RES.,FXD,CMPSN:360 OHM,5%,0.25W	57668	NTR25J-E 360E
A9R116	315-0511-00	B061870		RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E

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A9R118	315-0102-00	B010100	B061869	RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A9R118	315-0331-00	B061870		RES.,FXD,CMPSN:330 OHM,5%,0.25W	57668	NTR25J-E330E
A9R119	315-0511-00	B061870		RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A9R120	315-0681-00	B061870		RES.,FXD,CMPSN:680 OHM,5%,0.25W	57668	NTR25J-E680E
A9R120	315-0472-00	B061870		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A9R121	321-0289-00	B061870		RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A9R122	321-0282-00	B061870		RES.,FXD,FILM:8.45K OHM,1%,0.125W	91637	MFF1816G84500F
A9R320	321-0202-00			RES.,FXD,FILM:1.24K OHM,1%,0.125W	91637	CMF55116G12400F
A9R321	315-0152-00	B062200		RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A9R322	321-0231-00			RES.,FXD,FILM:2.49K OHM,1%,0.125W	91637	MFF1816G24900F
A9R323	321-0202-00			RES.,FXD,FILM:1.24K OHM,1%,0.125W	91637	CMF55116G12400F
A9R325	321-0202-00			RES.,FXD,FILM:1.24K OHM,1%,0.125W	91637	CMF55116G12400F
A9R410	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	01121	106A103
A9R520	321-0202-00			RES.,FXD,FILM:1.24K OHM,1%,0.125W	91637	CMF55116G12400F
A9R522	321-0202-00			RES.,FXD,FILM:1.24K OHM,1%,0.125W	91637	CMF55116G12400F
A9R523	321-0231-00			RES.,FXD,FILM:2.49K OHM,1%,0.125W	91637	MFF1816G24900F
A9R525	321-0202-00			RES.,FXD,FILM:1.24K OHM,1%,0.125W	91637	CMF55116G12400F
A9R621	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A9R622	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A9R626	321-0483-00			RES.,FXD,FILM:1.05M OHM,1%,0.125W,TC=TO	03888	A3AT75
A9R627	321-0452-00			RES.,FXD,FILM:499K OHM,1%,0.125W	91637	CMF55116G49902F
A9R628	321-0618-00			RES.,FXD,FILM:250K OHM,1%,0.125W	91637	MFF1816G25002F
A9R720	315-0241-00	B010100	B061869	RES.,FXD,CMPSN:240 OHM,5%,0.25W	57668	NTR25J-E 240E
A9R810	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	01121	106A103
A9R820	321-0195-00	B061870		RES.,FXD,FILM:1.05K OHM,1%,0.125W	91637	CMF55116G10500F
A9R821	321-0169-00	B061870		RES.,FXD,FILM:562 OHM,1%,0.125W	91637	CMF55116G562R0F
A9R905	307-0586-00			RES NTWK,FXD FI:9.39K OHM,2%,1.25W	91637	CSC10A01393G
A9R920	321-0280-00			RES.,FXD,FILM:8.06K OHM,1%,0.125W	91637	MFF1816G80600F
A9R922	321-0285-00			RES.,FXD,FILM:9.09K OHM,1%,0.125W	91637	MFF1816G90900F
A9R925	315-0151-00	B061870		RES.,FXD,CMPSN:150 OHM,5%,0.25W	57668	NTR25J-E150E
A9R1000	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272
A9R1001	307-0637-00			RES NTWK,FXD,FI:5,2K OHM,2%,0.125W	01121	206A202
A9U100	156-1654-00			MICROCIRCUIT,DI:NMOS,1024 X 1 NVRAM W/3 STA	T1282	X2201-30
A9U110	156-0721-02	B010100	B061869	MICROCIRCUIT,DI:QUAD 2-IN NAND SCHMITT TRI	04713	SN74LS132NDS
A9U110	156-0722-02	B061870		MICROCIRCUIT,DI:TPL 3-INPUT POS NAND GATE	04713	SN74LS12NDS
A9U120	156-0645-02	B010100	B061869	MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A9U125	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A9U200	160-1164-01	B010100	B029999	MICROCIRCUIT,DI:8192 X 8 EPROM PROGRAMMED	80009	160-1164-01
A9U200	160-1164-02	B030000		MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1164-02
A9U210	156-0874-02			MICROCIRCUIT,DI:8 BIT ADDRESSABLE LCH	04713	SN74LS259
A9U215	156-1631-00	B061870		MICROCIRCUIT,LI:ADJ SHUNT REGULATOR	01295	TL431C-LP
A9U220	156-0513-02			MICROCIRCUIT,DI:8-CHANNEL MUX,SEL	80009	156-0513-02
A9U300	160-1165-01	B010100	B029999	MICROCIRCUIT,DI:8192 X 8 EPROM PROGRAMMED	80009	160-1165-01
A9U300	160-1165-02	B030000		MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1165-02
A9U310	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3 OR
A9U315	156-0874-02			MICROCIRCUIT,DI:8 BIT ADDRESSABLE LCH	04713	SN74LS259
A9U320	156-0927-02			MICROCIRCUIT,LI:DIGITAL/ANALOG CONVERTER	04713	MC3410CLD
A9U325	156-1191-01			MICROCIRCUIT,LI:DUAL BI-FET OP-AMP,8 DIP	01295	TL072ACP3
A9U400	160-1163-01	B010100	B029999	MICROCIRCUIT,DI:8192 X 8 EPROM PROGRAMMED	80009	160-1163-01
A9U400	160-1163-02	B030000		MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1163-02
A9U410	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3 OR
A9U420	156-0927-02			MICROCIRCUIT,LI:DIGITAL/ANALOG CONVERTER	04713	MC3410CLD
A9U500	160-1162-01	B010100	B029999	MICROCIRCUIT,DI:8192 X 8 EPROM PROGRAMMED	80009	160-1162-01
A9U500	160-1162-02	B030000	B061368	MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1162-02
A9U500	160-1162-03	B061369		MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1162-03

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A9U510	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A9U515	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A9U520	156-1173-00			MICROCIRCUIT,LI:VOLTAGE REFERENCE	04713	MC1403UDS
A9U525	156-1595-00			MICROCIRCUIT,DI:CMOS,A/D CONV	15818	8701CN
A9U600	160-1676-01	B010100	B029999	MICROCIRCUIT,DI:8192 X 8 EPROM PROGRAMMED	80009	160-1676-01
A9U600	160-1676-02	B030000		MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1676-02
A9U610	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A9U700	160-1757-01	B010100	B029999	MICROCIRCUIT,DI:8192 X 8 EPROM PROGRAMMED	80009	160-1757-01
A9U700	160-1757-02	B030000	B061368	MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1757-02
A9U700	160-1757-03	B061369		MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1757-03
A9U710	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A9U715	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A9U720	156-0721-02			MICROCIRCUIT,DI:QUAD 2-IN NAND SCHMITT TRI	04713	SN74LS132NDS
A9U725	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A9U800	156-1594-00			MICROCIRCUIT,DI:2048 X 8 SRAM	T1015	HM6116P-3(DP-24)
A9U810	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A9U815	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A9U820	156-1126-01	B061870		MICROCIRCUIT,LI:VOLTAGE COMPARATOR,SEL	01295	LM311JG4
A9U825	156-0172-02			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	07263	74123(PCQR)
A9U900	156-1594-00			MICROCIRCUIT,DI:2048 X 8 SRAM	T1015	HM6116P-3(DP-24)
A9U910	156-1494-00			MICROCIRCUIT,DI:8-BIT MICROPRO PRC	04713	MC68B09(S OR L)
A9U915	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A9U925	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A9U1000	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245 N3ORJ4
A9U1010	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A9VR720	152-0688-00	B010100	B61869	SEMICOND DEVICE:ZENER,2.4V,5%,0.4W	04713	1N4370A
A9Y825	158-0122-00			XTAL UNIT,QTZ:6.25MHZ,0.01%	75378	ORD BY DESCR

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A10	670-7324-00	B010100	B040399	CKT BOARD ASSY:TRIGGER	80009	670-7324-00
A10	670-7324-01	B040400	B062019	CKT BOARD ASSY:TRIGGER	80009	670-7324-01
A10	670-7324-02	B062020		CKT BOARD ASSY:TRIGGER	80009	670-7324-02
A10C100	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C110	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A10C130	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A10C131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C132	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C133	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C200	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C220	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10V	54473	ECE-B1AV470S
A10C221	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C230	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C231	281-0864-00			CAP.,FXD,CER DI:430PF,5%,100V	12969	CGD431JEN
A10C232	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C240	281-0765-00			CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710-100NP0101J
A10C300	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C310	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A10C340	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C430	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A10C431	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A10C432	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C433	283-0167-00			CAP.,FXD,CER DI:0.1UF,10%,100V	72982	8131N145X5R0104K
A10C440	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C500	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	04222	MA101A5R6DAA
A10C510	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10V	54473	ECE-B1AV470S
A10C520	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10V	54473	ECE-B1AV470S
A10C530	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C546	283-0198-00			CAP.,FXD,CER DI:0.22UF,20%,50V	04222	ADVISE
A10C600	290-0778-00			CAP.,FXD,ELCTLT:1UF,+50-10%,50V	55680	UEB1H010MAA1TD
A10C601	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	04222	MA101A5R6DAA
A10C611	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A10C620	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C630	283-0198-00			CAP.,FXD,CER DI:0.22UF,20%,50V	04222	ADVISE
A10C730	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C800	281-0852-00	B010100	B062400	CAP.,FXD,CER DI:1800PF,10%,100VDC	04222	MA101C182KAA
A10C800	281-0910-00	B062401		CAP.,FXD,CER DI:1800PF,1%,50V	96733	T-W512BY182W
A10C810	281-0852-00	B010100	B062400	CAP.,FXD,CER DI:1800PF,10%,100VDC	04222	MA101C182KAA
A10C810	281-0910-00	B062401		CAP.,FXD,CER DI:1800PF,1%,50V	96733	T-W512BY182W
A10C811	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A10C812	281-0852-00	B010100	B062400	CAP.,FXD,CER DI:1800PF,10%,100VDC	04222	MA101C182KAA
A10C812	281-0910-00	B062401		CAP.,FXD,CER DI:1800PF,1%,50V	96733	T-W512BY182W
A10C813	281-0852-00			CAP.,FXD,CER DI:1800PF,10%,100VDC	04222	MA101C182KAA
A10C814	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A10C830	283-0339-00			CAP.,FXD,CER DI:0.22UF.10%,50V	51642	300 050X5R224K
A10C900	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A10C910	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A10C911	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A10C912	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A10C913	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A10C920	281-0788-00			CAP.,FXD,CER DI:470PF,10%,100V	96733	R3015
A10C921	281-0788-00			CAP.,FXD,CER DI:470PF,10%,100V	96733	R3015

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A10C922	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	MA201C472KAA
A10C930	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C940	281-0863-00			CAP.,FXD CER DI:240PF,5%,100V	04222	GC101A241J
A10C941	283-0103-00			CAP.,FXD,CER DI:180PF,5%,500V	59660	831-518-Z5D0181J
A10C942	283-0779-00			CAP.,FXD,MICA D:27PF,2%,500V	00853	D155E270G0
A10C1030	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A10C1040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C1041	283-0103-00			CAP.,FXD,CER DI:180PF,5%,500V	59660	831-518-Z5D0181J
A10C1042	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C1043	281-0709-00			CAP.,FXD,CER DI:7PF,+/-0.1PF,500V	59660	3740018C0H0709B
A10CR140	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A10CR243	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR244	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR430	152-0246-00			SEMICOND DEVICE:SW,SI,40V,200MA	14433	WG1537TK
A10CR431	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR432	152-0246-00			SEMICOND DEVICE:SW,SI,40V,200MA	14433	WG1537TK
A10CR530	152-0246-00			SEMICOND DEVICE:SW,SI,40V,200MA	14433	WG1537TK
A10CR531	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR532	152-0246-00			SEMICOND DEVICE:SW,SI,40V,200MA	14433	WG1537TK
A10CR730	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR810	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR811	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR830	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR831	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR840	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR841	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR901	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR902	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR933	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR935	152-0242-00			SEMICOND DVC:SIG,SI,225V,0.2A,D0-7	07263	FDH5004
A10CR1000	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR1030	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A10CR1040	152-0242-00			SEMICOND DVC:SIG,SI,225V,0.2A,D0-7	07263	FDH5004
A10L330	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A10L331	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A10L341	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A10L410	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A10L411	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A10L430	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A10L930	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A10L1020	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A10L1030	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A10L1031	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A10LR920	108-0328-00			COIL,RF:0.3UH	80009	108-0328-00
A10LR921	108-0328-00			COIL,RF:0.3UH	80009	108-0328-00
A10Q110	151-0221-05			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0221-05
A10Q120	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A10Q140	151-0198-00			TRANSISTOR:SELECTED	04713	SPS8802-1
A10Q141	151-0198-00			TRANSISTOR:SELECTED	04713	SPS8802-1
A10Q240	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A10Q630	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A10Q631	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A10Q640	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A10Q800	151-0223-03			TRANSISTOR:NPN,SI,PRESTRESSED & TESTED	80009	151-0223-03

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A10Q801	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A10Q830	151-1025-00			TRANSISTOR:SILICON,JFE,N-CHANNEL	01295	SFB8129
A10Q930	151-1025-00			TRANSISTOR:SILICON,JFE,N-CHANNEL	01295	SFB8129
A10Q931	151-0223-03			TRANSISTOR:NPN,SI,PRESTRESSED & TESTED	80009	151-0223-03
A10Q940	151-1025-00			TRANSISTOR:SILICON,JFE,N-CHANNEL	01295	SFB8129
A10Q1010	151-0427-00			TRANSISTOR:SILICON,NPN	07263	S39287
A10Q1011	151-0427-00			TRANSISTOR:SILICON,NPN	07263	S39287
A10Q1020	151-0223-03			TRANSISTOR:NPN,SI,PRESTRESSED & TESTED	80009	151-0223-03
A10Q1022	151-0223-03			TRANSISTOR:NPN,SI,PRESTRESSED & TESTED	80009	151-0223-03
A10Q1030	151-0223-03			TRANSISTOR:NPN,SI,PRESTRESSED & TESTED	80009	151-0223-03
A10Q1040	151-1025-00			TRANSISTOR:SILICON,JFE,N-CHANNEL	01295	SFB8129
A10R100	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A10R110	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A10R112	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A10R113	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A10R114	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A10R120	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R121	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	57668	NTR25J-E 3K6
A10R122	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R123	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A10R124	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A10R130	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R131	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A10R132	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A10R133	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A10R134	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A10R135	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A10R140	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A10R141	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A10R142	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A10R143	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A10R144	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A10R145	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A10R146	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A10R200	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A10R201	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A10R203	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A10R210	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	57668	NTR25J-E470E
A10R220	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A10R230	321-0130-00			RES.,FXD,FILM:221 OHM,1%,0.125W	91637	MFF1816G221R0F
A10R231	321-0222-00	B010100	B040399	RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A10R231	131-0566-00	B040400		BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A10R232	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R240	311-1247-00			RES.,VAR,NONWIR:1M OHM,10%,0.5OW	73138	72-35-0
A10R241	311-1247-00			RES.,VAR,NONWIR:1M OHM,10%,0.5OW	73138	72-35-0
A10R242	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R243	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R300	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A10R301	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	57668	NTR25J-E 22K
A10R302	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A10R310	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A10R311	321-0232-00			RES.,FXD,FILM:2.55K OHM,1%,0.125W	24546	CT552551F
A10R320	321-0232-00			RES.,FXD,FILM:2.55K OHM,1%,0.125W	24546	CT552551F
A10R330	321-0296-00			RES.,FXD,FILM:11.8K OHM,1%,0.125W	91637	MFF1816G11801F

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A10R331	321-0197-00			RES.,FXD,FILM:1.1K OHM,1%,0.125W	91637	CMF55116G11000F
A10R332	315-0132-00			RES.,FXD,CMPSN:1.3K OHM,5%,0.25W	57668	NTR25J-E01K3
A10R333	307-0103-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.25W	01121	CB27G5
A10R334	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A10R340	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R341	315-0205-00			RES.,FXD,CMPSN:2M OHM,5%,0.25W	01121	CB2055
A10R342	315-0200-00			RES.,FXD,CMPSN:20 OHM,5%,0.25W	57668	NTR25J-E 20E
A10R343	315-0475-00			RES.,FXD,CMPSN:4.7M OHM,5%,0.25W	01121	CB4755
A10R344	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	57668	NTR25J-E470E
A10R402	311-1238-00			RES.,VAR,NONWIR:5K OHM,10%,0.50W	73138	72-27-0
A10R430	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A10R431	321-0510-00			RES.,FXD,FILM:2M OHM,1%,0.125W	91637	HFF188G20003F
A10R432	321-0510-00			RES.,FXD,FILM:2M OHM,1%,0.125W	91637	HFF188G20003F
A10R433	321-0510-00			RES.,FXD,FILM:2M OHM,1%,0.125W	91637	HFF188G20003F
A10R434	315-0684-00			RES.,FXD,CMPSN:680K OHM,5%,0.25W	01121	CB6845
A10R440	311-1198-00			RES.,VAR,NONWIR:20K OHM,20%,0.5W	73138	72-29-0
A10R441	321-0481-00			RES.,FXD,FILM:1M OHM,1%,0.125W	91637	CMF55116G10003F
A10R442	321-0418-00			RES.,FXD,FILM:221K OHM,1%,0.125W	91637	MFF1816G22102F
A10R443	321-0450-00			RES.,FXD,FILM:475K OHM,1%,0.125W	91637	CMF55116G47502F
A10R444	311-1238-00			RES.,VAR,NONWIR:5K OHM,10%,0.50W	73138	72-27-0
A10R500	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A10R510	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A10R511	315-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	57668	NTR25J-E 1K1
A10R520	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	57668	NTR25J-E39K0
A10R521	315-0106-00			RES.,FXD,CMPSN:10M OHM,5%,0.25W	01121	CB1065
A10R532	321-0510-00			RES.,FXD,FILM:2M OHM,1%,0.125W	91637	HFF188G20003F
A10R533	321-0423-00	B010100	B050730	RES.,FXD,FILM:249K OHM,1%,0.125W	91637	CMF55116G24902F
A10R533	321-0421-00	B050731		RES.,FXD,FILM:237K OHM,1%,0.125W	91637	MFF1816G23702F
A10R534	321-0510-00			RES.,FXD,FILM:2M OHM,1%,0.125W	91637	HFF188G20003F
A10R535	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	57668	NTR25J-E 240K
A10R540	321-0418-00			RES.,FXD,FILM:221K OHM,1%,0.125W	91637	MFF1816G22102F
A10R541	311-1241-00			RES.,VAR,NONWIR:100K OHM,10%,0.5W	32997	3386X-T07-104
A10R542	315-0475-00			RES.,FXD,CMPSN:4.7M OHM,5%,0.25W	01121	CB4755
A10R543	311-1198-00			RES.,VAR,NONWIR:20K OHM,20%,0.5W	73138	72-29-0
A10R544	321-0481-00			RES.,FXD,FILM:1M OHM,1%,0.125W	91637	CMF55116G10003F
A10R545	321-0450-00			RES.,FXD,FILM:475K OHM,1%,0.125W	91637	CMF55116G47502F
A10R546	311-1239-00			RES.,VAR,NONWIR:2.5K OHM,10%,0.50W	73138	72-26-0
A10R600	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	57668	NTR25J-E51E0
A10R601	315-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	57668	NTR25J-E 1K1
A10R610	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A10R630	315-0106-00			RES.,FXD,CMPSN:10M OHM,5%,0.25W	01121	CB1065
A10R631	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	57668	NTR25J-E07K5
A10R632	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A10R633	315-0163-00			RES.,FXD,CMPSN:16K OHM,5%,0.25W	57668	NTR25J-E16K0
A10R634	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A10R635	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	57668	NTR25J-E07K5
A10R636	315-0623-00			RES.,FXD,CMPSN:62K OHM,5%,0.25W	57668	NTR25J-E 62K
A10R637	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A10R640	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A10R641	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A10R642	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A10R643	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A10R644	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A10R645	311-1239-00			RES.,VAR,NONWIR:2.5K OHM,10%,0.50W	73138	72-26-0

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A10R700	315-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	57668	NTR25J-E 1K1
A10R701	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A10R702	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A10R703	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A10R704	321-0248-00			RES.,FXD,FILM:3.74K OHM,1%,0.125W	91637	CMF55116G37400F
A10R710	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A10R711	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A10R712	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A10R713	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A10R714	321-0262-00			RES.,FXD,FILM:5.23K OHM,1%,0.125W	91637	MFF1816G52300F
A10R720	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A10R730	321-0419-00			RES.,FXD,FILM:226K OHM,1%,0.125W	91637	MFF1816G22602F
A10R730	321-0420-00			RES.,FXD,FILM:232K OHM,1%,0.125W	91637	MFF1816G23202F
A10R730	321-0421-00			RES.,FXD,FILM:237K OHM,1%,0.125W	91637	MFF1816G23702F
A10R730	----- -----			(R730 SELECTED)		
A10R731	321-0326-00			RES.,FXD,FILM:24.3K OHM,1%,0.125W	91637	CMF55116G24301F
A10R732	315-0433-00			RES.,FXD,CMPSN:43K OHM,5%,0.25W	57668	NTR25J-E043K
A10R733	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A10R734	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A10R735	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A10R740	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A10R741	315-0226-00			RES.,FXD,CMPSN:22M OHM,5%,0.25W	01121	CB2265
A10R742	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A10R743	321-0377-00			RES.,FXD,FILM:82.5K OHM,1%,0.125W	91637	MFF1816G82501F
A10R744	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A10R800	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A10R801	321-0069-00			RES.,FXD,FILM:51.1 OHM,1%,0.125W	91637	CMF55116G51R10F
A10R802	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A10R803	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R810	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A10R811	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A10R812	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A10R813	321-0069-00			RES.,FXD,FILM:51.1 OHM,1%,0.125W	91637	CMF55116G51R10F
A10R814	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A10R815	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	57668	NTR25J-E 10E0
A10R818	317-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.125W	01121	BB7505
A10R820	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A10R821	315-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	57668	NTR25J-E 1K1
A10R822	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A10R830	321-0325-00			RES.,FXD,FILM:23.7K OHM,1%,0.125W	91637	MFF1816G23701F
A10R840	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A10R841	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	57668	NTR25J-E39K0
A10R842	315-0396-00			RES.,FXD,CMPSN:39M OHM,5%,0.25W	01121	CB3965
A10R843	315-0270-00			RES.,FXD,CMPSN:27 OHM,5%,0.25W	57668	NTR25J-E 27E
A10R900	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	57668	NTR25J-E300E
A10R901	321-0457-00			RES.,FXD,FILM:562K OHM,1%,0.125W	91637	CMF55116G56202F
A10R902	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A10R903	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A10R904	321-0285-00			RES.,FXD,FILM:9.09K OHM,1%,0.125W	91637	MFF1816G90900F
A10R910	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A10R911	315-0390-00			RES.,FXD,CMPSN:39 OHM,5%,0.25W	57668	NTR25J-E39E0
A10R912	315-0390-00			RES.,FXD,CMPSN:39 OHM,5%,0.25W	57668	NTR25J-E39E0
A10R921	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	57668	NTR25J-E470E
A10R922	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3

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A10R930	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R931	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A10R932	321-0405-00			RES.,FXD,FILM:162K OHM,1%,0.125W	91637	MFF1816G16202F
A10R933	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	57668	NTR25J-E 820E
A10R934	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A10R940	321-0312-00			RES.,FXD,FILM:17.4K OHM,1%,0.125W	91637	MFF1816G17401F
A10R941	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R942	321-0404-00			RES.,FXD,FILM:158K OHM,1%,0.125W	91637	MFF1816G15802F
A10R1001	307-0113-00			RES.,FXD,CMPSN:5.1 OHM,5%,0.25W	01121	CB51G5
A10R1002	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A10R1010	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R1011	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A10R1012	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A10R1013	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	57668	NTR25J-E620E
A10R1020	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R1021	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R1022	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A10R1023	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R1024	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	57668	NTR25J-E 3K6
A10R1025	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	57668	NTR25J-E 130E
A10R1026	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A10R1030	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A10R1040	315-0566-00			RES.,FXD,CMPSN:56M OHM,5%,0.25W	01121	CB5665
A10R1041	315-0566-00			RES.,FXD,CMPSN:56M OHM,5%,0.25W	01121	CB5665
A10R1042	321-0473-00			RES.,FXD,FILM:825K OHM,1%,0.125W	91637	MFF1816G82502F
A10R1043	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A10T500	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A10T600	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A10U100	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A10U101	156-0384-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS03
A10U140	156-0302-02			MICROCIRCUIT,DI:DUAL 2-INP NAND DRVR,SCRN	01295	SN75452(PP3 OR J
A10U200	156-0796-01			MICROCIRCUIT,DI:8 STG SHF & STORE BUS RGTR	80009	156-0796-01
A10U201	156-0796-01			MICROCIRCUIT,DI:8 STG SHF & STORE BUS RGTR	80009	156-0796-01
A10U210	156-0796-01			MICROCIRCUIT,DI:8 STG SHF & STORE BUS RGTR	80009	156-0796-01
A10U230	156-1272-00			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	18324	NE5532 FE-B
A10U300	156-0513-02			MICROCIRCUIT,DI:8-CHANNEL MUX,SEL	80009	156-0513-02
A10U310	156-1255-01			MICROCIRCUIT,LI:D/A CONVERTER,BURN-IN	04713	DAC-08HQDS
A10U430	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A10U530	156-1200-01			MICROCIRCUIT,LI:OPERATIONAL AMPL,QUAD	01295	TL074CN/PEP3
A10U610	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A10U710	156-0514-01			MICROCIRCUIT,DI:DIFF 4-CHANNEL MUX,SEL	80009	156-0514-01
A10U740	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A10U830	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	LM358J
A10U900	155-0196-00			MICROCKT,INTFC:TRIGGER	80009	155-0196-00
A10U940	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A10VR932	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738RL
A10W210	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

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A11	670-7325-00	B010100	B050595	CKT BOARD ASSY:TIME BASE	80009	670-7325-00
A11	670-7325-02	B050596		CKT BOARD ASSY:TIME BASE	80009	670-7325-02
A11C110	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C130	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A11C131	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A11C132	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A11C203	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	04222	MA101A5R6DAA
A11C204	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	04222	MA101A5R6DAA
A11C410	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C420	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C430	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C431	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A11C520	283-0646-00			CAP.,FXD,MICA D:170PF,1%,100V	00853	D155F171F0
A11C531	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C532	281-0758-00			CAP.,FXD,CER DI:15PF,20%,100V	04222	MA101A150MAA
A11C710	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C730	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C820	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C821	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C930	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A11C1010	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C1110	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C1130	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C1310	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C1330	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C1430	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C1630	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11C1700	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A11CR700	152-0066-00			SEMICOND DVC DI:RECT,SI,400V,1A,D0-41	05828	GP10G-020
A11CR701	152-0066-00			SEMICOND DVC DI:RECT,SI,400V,1A,D0-41	05828	GP10G-020
A11CR730	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A11L130	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A11L131	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A11L132	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A11L930	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A11P1430	131-1857-00	B050596		TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65507-136
A11P1432	131-1851-00	B050596		CONN,RCPT,ELEC:CKT CD,1 FEMALE CONT	80009	131-1851-00
A11Q100	151-0221-05			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0221-05
A11Q101	151-0221-05			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0221-05
A11Q220	151-0221-05			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0221-05
A11Q221	151-0221-05			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0221-05
A11Q520	151-0221-05			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0221-05
A11Q521	151-0220-05			TRANSISTOR:SCREENED	80009	151-0220-05
A11Q530	151-1045-00			TRANSISTOR:SILICON,JFE,P-CHANNEL	04713	SPS628
A11Q531	151-0283-00			TRANSISTOR:SILICON,NPN	07263	S032790
A11Q532	151-0283-00			TRANSISTOR:SILICON,NPN	07263	S032790
A11Q533	151-0220-05			TRANSISTOR:SCREENED	80009	151-0220-05
A11Q620	151-0221-05			TRANSISTOR:SILICON,PNP,SCREENED	80009	151-0221-05
A11Q621	151-0220-05			TRANSISTOR:SCREENED	80009	151-0220-05
A11Q630	151-1025-00			TRANSISTOR:SILICON,JFE,N-CHANNEL	01295	SFB8129
A11R100	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A11R101	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A11R110	307-0651-00			RES NTWK,FXD FI:5,3.3K OHM,5%,0.15W	01121	206A332

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A11R120	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	57668	NTR25J-E910E
A11R121	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A11R122	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A11R201	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	57668	NTR25J-E620E
A11R202	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	57668	NTR25J-E620E
A11R203	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A11R204	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A11R220	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	57668	NTR25J-E330E
A11R231	315-0434-00			RES.,FXD,CMPSN:430K OHM,5%,0.25W	57668	NTR25J-E430K
A11R232	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A11R233	321-0816-03			RES.,FXD,FILM:5K OHM,0.25%,0.125W	91637	CMF55116D50000C
A11R234	321-0289-07			RES.,FXD,FILM:10K OHM,0.1%,0.125W	91637	CMF55116C10001B
A11R235	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A11R320	311-1227-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	32997	3386F-T04-502
A11R420	321-0646-00			RES.,FXD,FILM:200K OHM,0.5%,0.125W	91637	MFF1816D20002D
A11R421	315-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.25W	57668	NTR25J-E82E0
A11R422	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	19701	5043ED1K00F
A11R423	321-0260-00			RES.,FXD,FILM:4.99K OHM,1%,0.125W	91637	MFF1816G49900F
A11R430	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A11R431	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A11R432	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A11R530	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A11R531	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	57668	NTR25J-E910E
A11R532	321-0135-00			RES.,FXD,FILM:249 OHM,1%,0.125W	91637	CMF55116G249R0F
A11R620	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A11R701	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A11R720	315-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.25W	57668	NTR25J-E82E0
A11R721	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	57668	NTR25J-E680E
A11R722	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A11R723	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	57668	NTR25J-E 15K
A11R724	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	24546	CT55 3011 F
A11R730	321-0164-00			RES.,FXD,FILM:499 OHM,1%,0.125W	91637	CMF55116G499R0F
A11R731	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A11R732	311-1227-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	32997	3386F-T04-502
A11R830	321-0085-00			RES.,FXD,FILM:75 OHM,1%,0.125W	91637	CMF55116G75R00F
A11R1720	307-0651-00			RES NTWK,FXD FI:5,3.3K OHM,5%,0.15W	01121	206A332
A11U110	156-0720-02			MICROCIRCUIT,DI:HEX DRVR,4 TO 2 LINE	01295	SN74LS368
A11U210	156-1258-01			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A11U300	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A11U310	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A11U400	156-0721-02			MICROCIRCUIT,DI:QUAD 2-IN NAND SCHMITT TRI	04713	SN74LS132NDS
A11U410	156-0381-02			MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A11U430	156-1191-01			MICROCIRCUIT,LI:DUAL BI-FET OP-AMP,8 DIP	01295	TL072ACP3
A11U500	156-0910-02			MICROCIRCUIT,DI:DUAL DECADE COUNTER	01295	SN74LS390
A11U510	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74LS1759NP3 OR
A11U600	156-0910-02			MICROCIRCUIT,DI:DUAL DECADE COUNTER	01295	SN74LS390
A11U610	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A11U710	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U800	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3
A11U810	156-0788-01			MICROCIRCUIT,DI:SYN 4-BIT CNTR,W/SYN CLEAR	01295	SN74LS162NP3/JP4
A11U830	156-0116-00			MICROCIRCUIT,LI:DUAL COMPARATOR	27014	LM711CN
A11U900	156-0784-02			MICROCIRCUIT,DI:SYNC 4 BIT BINARY COUNTER	27014	DM74LS163ANA+
A11U910	156-1258-01			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A11U1000	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A11U1010	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A11U1030	156-0118-03			MICROCIRCUIT,DI:1 DUAL J-K FF,BURN-IN	01295	SN74S112JP3
A11U1100	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U1110	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR	01295	SN74LS393
A11U1120	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U1130	156-0118-03			MICROCIRCUIT,DI:1 DUAL J-K FF,BURN-IN	01295	SN74S112JP3
A11U1200	156-0118-03			MICROCIRCUIT,DI:1 DUAL J-K FF,BURN-IN	01295	SN74S112JP3
A11U1210	156-0789-02			MICROCIRCUIT,DI:8 BIT SR,PRL LOAD,SCRN	80009	156-0789-02
A11U1220	156-0118-03			MICROCIRCUIT,DI:1 DUAL J-K FF,BURN-IN	01295	SN74S112JP3
A11U1300	156-0629-01			MICROCIRCUIT,DI:30 MHZ PRESETTABLE BIN	01295	SN74LS197
A11U1310	156-0796-01			MICROCIRCUIT,DI:8 STG SHF & STORE BUS RGTR	80009	156-0796-01
A11U1320	156-0789-02			MICROCIRCUIT,DI:8 BIT SR,PRL LOAD,SCRN	80009	156-0789-02
A11U1400	156-0629-01			MICROCIRCUIT,DI:30 MHZ PRESETTABLE BIN	01295	SN74LS197
A11U1410	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A11U1420	156-1040-01			MICROCIRCUIT,DI:2 WIDE 2 INPUT/INVERT GATE	80009	156-1040-01
A11U1500	156-0629-01			MICROCIRCUIT,DI:30 MHZ PRESETTABLE BIN	01295	SN74LS197
A11U1510	156-0796-01			MICROCIRCUIT,DI:8 STG SHF & STORE BUS RGTR	80009	156-0796-01
A11U1520	156-0910-02			MICROCIRCUIT,DI:DUAL DECADE COUNTER	01295	SN74LS390
A11U1530	156-0324-02	B010100	B063609	MICROCIRCUIT,DI:8 INPUT DATA SEL MULT,SEL	01295	SN74AS151(N)
A11U1530	156-0324-03	B063610		MICROCIRCUIT,DI:8 INP DATA SEL,SCRN	01295	SN74S151
A11U1600	156-0629-01			MICROCIRCUIT,DI:30 MHZ PRESETTABLE BIN	01295	SN74LS197
A11U1610	156-0796-01			MICROCIRCUIT,DI:8 STG SHF & STORE BUS RGTR	80009	156-0796-01
A11U1620	156-1044-01			MICROCIRCUIT,DI:4 BIT SYNC BIN CNTR,SCRN	07263	F93S16DCQR
A11U1630	119-1408-00			OSC,XTAL CLOCK:16MHZ,0.01%	22929	X0-33B16
A11U1700	156-0629-01			MICROCIRCUIT,DI:30 MHZ PRESETTABLE BIN	01295	SN74LS197
A11U1710	156-0796-01			MICROCIRCUIT,DI:8 STG SHF & STORE BUS RGTR	80009	156-0796-01
A11U1730	119-1460-00			OSCILLATOR,RF:40.0MHZ		
A11VR820	152-0278-00			SEMICOND DEVICE:ZENER,0.4W,3V,5%	04713	SZG35009K20
A11VR821	152-0149-00			SEMICOND DEVICE:ZENER,0.4W,10V,5%	04713	SZG35009K3

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A12	119-1444-00			ATTENUATOR,VAR:CHANNEL 2	80009	119-1444-00
A12K101	148-0138-00			RELAY,ARMATURE:4 CONT,250MA,COIL 7VDC	80009	148-0138-00
A12K102	148-0138-00			RELAY,ARMATURE:4 CONT,250MA,COIL 7VDC	80009	148-0138-00
A12K103	148-0138-00			RELAY,ARMATURE:4 CONT,250MA,COIL 7VDC	80009	148-0138-00
A12K104	148-0138-00			RELAY,ARMATURE:4 CONT,250MA,COIL 7VDC	80009	148-0138-00
A13	119-1444-00			ATTENUATOR,VAR:CHANNEL 2	80009	119-1444-00
A13K101	148-0138-00	B010100	B062079	RELAY,ARMATURE:4 CONT,250MA,COIL 7VDC	80009	148-0138-00
A13K101	148-0138-01	B062080		RELAY,ARMATURE:4 CONT,250MA,COIL 7VDC	80009	148-0138-01
A13K102	148-0138-00	B010100	B062079	RELAY,ARMATURE:4 CONT,250MA,COIL 7VDC	80009	148-0138-00
A13K102	148-0138-01	B062080		RELAY,ARMATURE:4 CONT,250MA,COIL 7VDC	80009	148-0138-01
A13K103	148-0138-00	B010100	B062079	RELAY,ARMATURE:4 CONT,250MA,COIL 7VDC	80009	148-0138-00
A13K103	148-0138-01	B062080		RELAY,ARMATURE:4 CONT,250MA,COIL 7VDC	80009	148-0138-01
A13K104	148-0138-00	B010100	B062079	RELAY,ARMATURE:4 CONT,250MA,COIL 7VDC	80009	148-0138-00
A13K104	148-0138-01	B062080		RELAY,ARMATURE:4 CONT,250MA,COIL 7VDC	80009	148-0138-01
				CHASSIS PARTS		
R10	311-1332-00			RES.,VAR,NONWIR:5K OHM,10%,2W	12697	CM40936
R20	311-1332-00			RES.,VAR,NONWIR:5K OHM,10%,2W	12697	CM40936

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DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

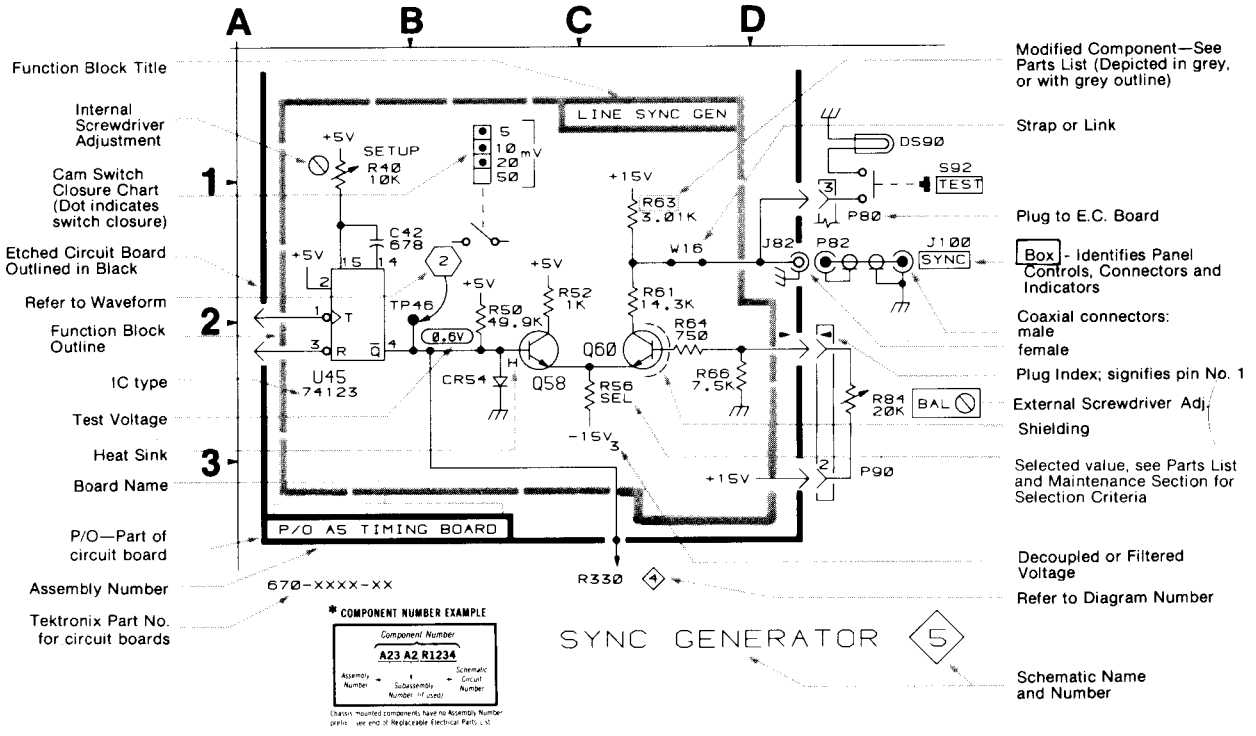
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



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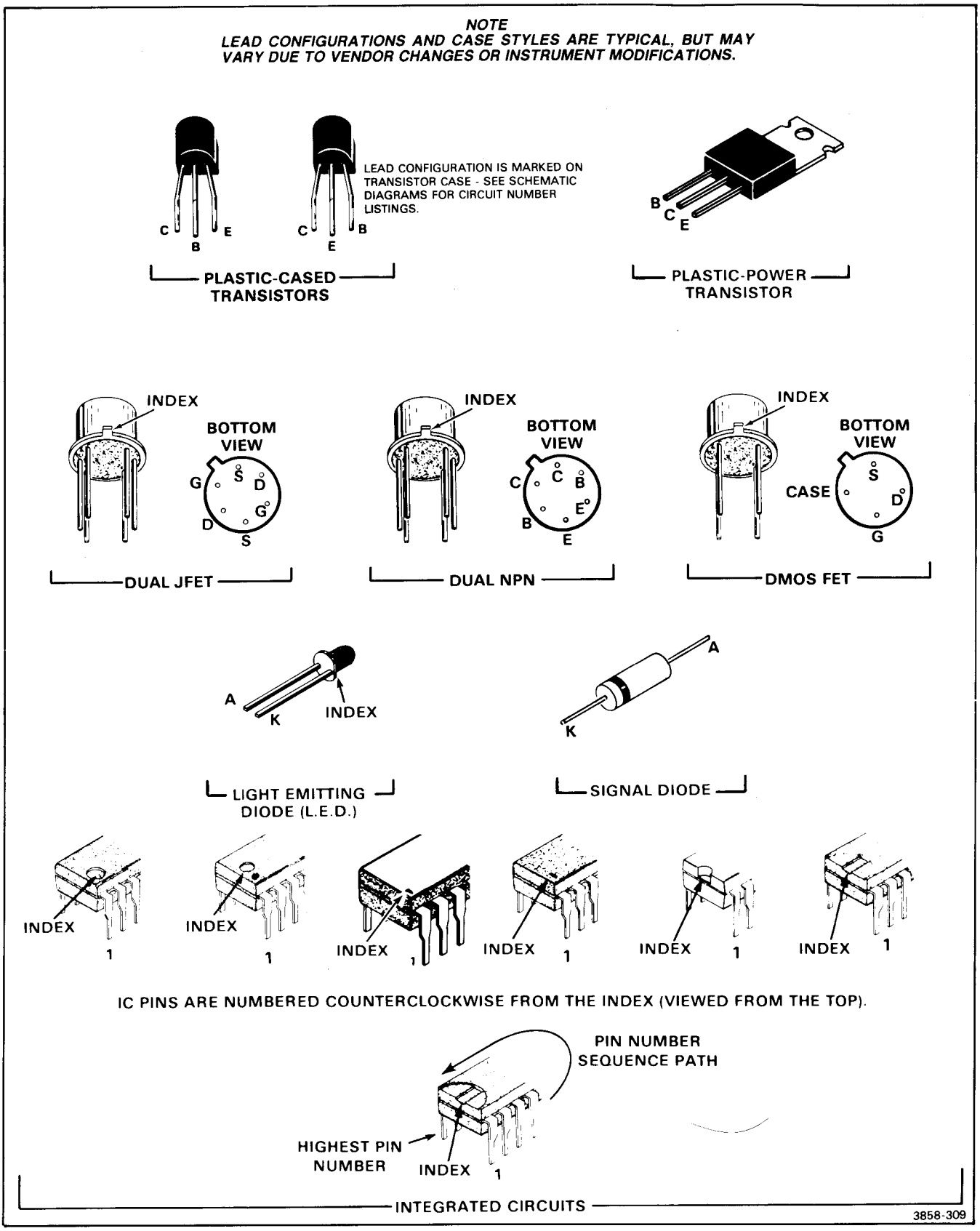

Figure 7-1. Semiconductor Lead Configurations.

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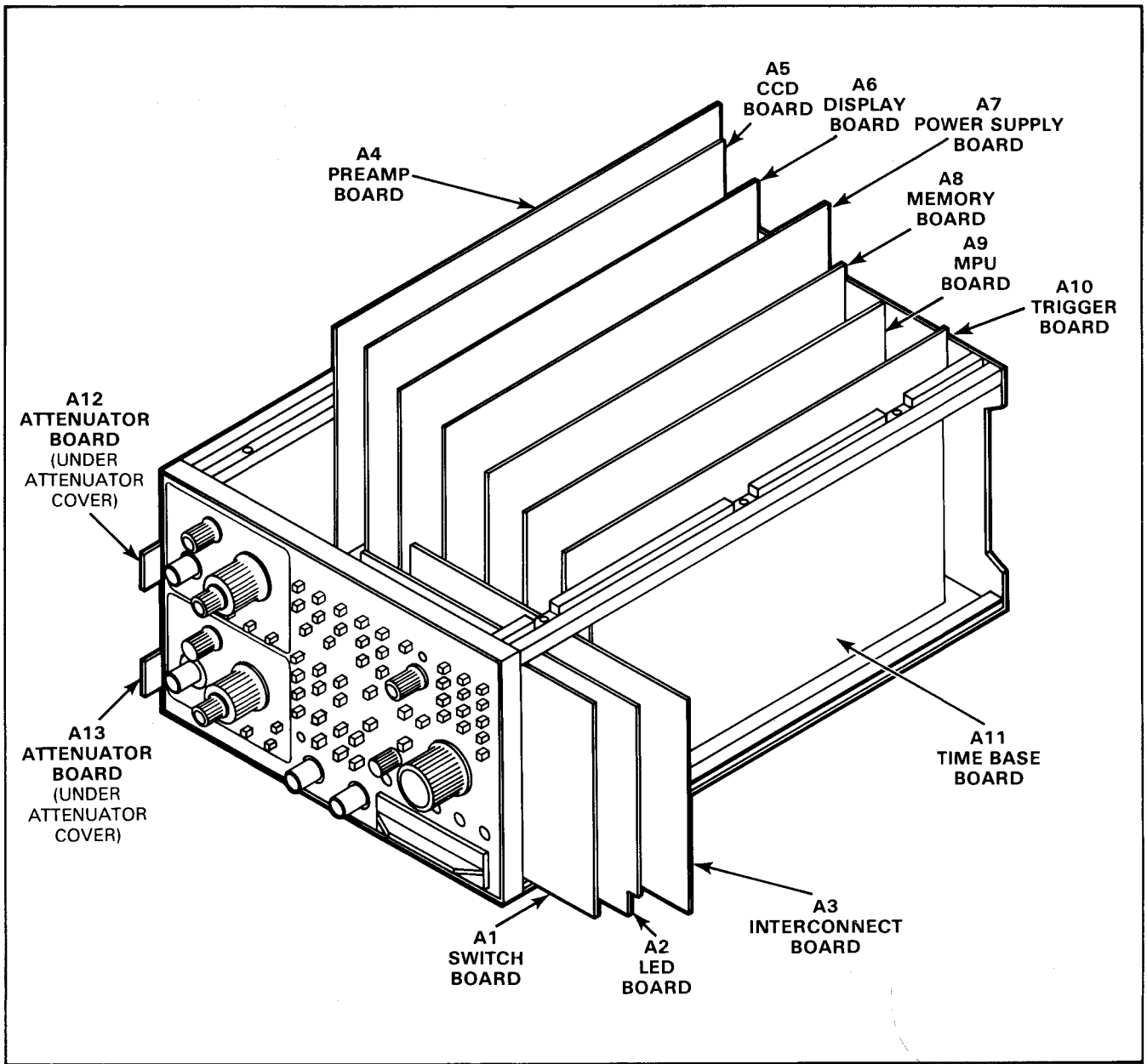

BOARD LOCATOR BY BOARD NAME			BOARD LOCATOR BY ASSEMBLY NUMBER		
Board Name	Assembly Number	Schematic Location	Assembly Number	Board Name	Diagram Number
Attenuator (CH 1)	A12	4	A1	Switch	1
Attenuator (CH 2)	A13	4	A2	LED	2,5,7,8,9
CCD	A5	6,7	A3	Interconnect	3,5,7,8,9
Display	A6	5,8,9	A4	Preamp	4,5,9
Interconnect	A3	3,5,7,8,9	A5	CCD	6,7
LED	A2	2,5,7,8,9	A6	Display	5,8,9
Memory	A8	11	A7	Power Supply	10
MPU	A9	5,9,12	A8	Memory	11
Power Supply	A7	10	A9	MPU	5,9,12
Preamp	A4	4,5,9	A10	Trigger	8,9,13
Switch	A1	1	A11	Timebase	14,15,16
Timebase	A11	14,15,16	A12	Attenuator (CH 1)	4
Trigger	A10	8,9,13	A13	Attenuator (CH 2)	4

3858-701

Figure 7-2. 7D20 Board Locator.

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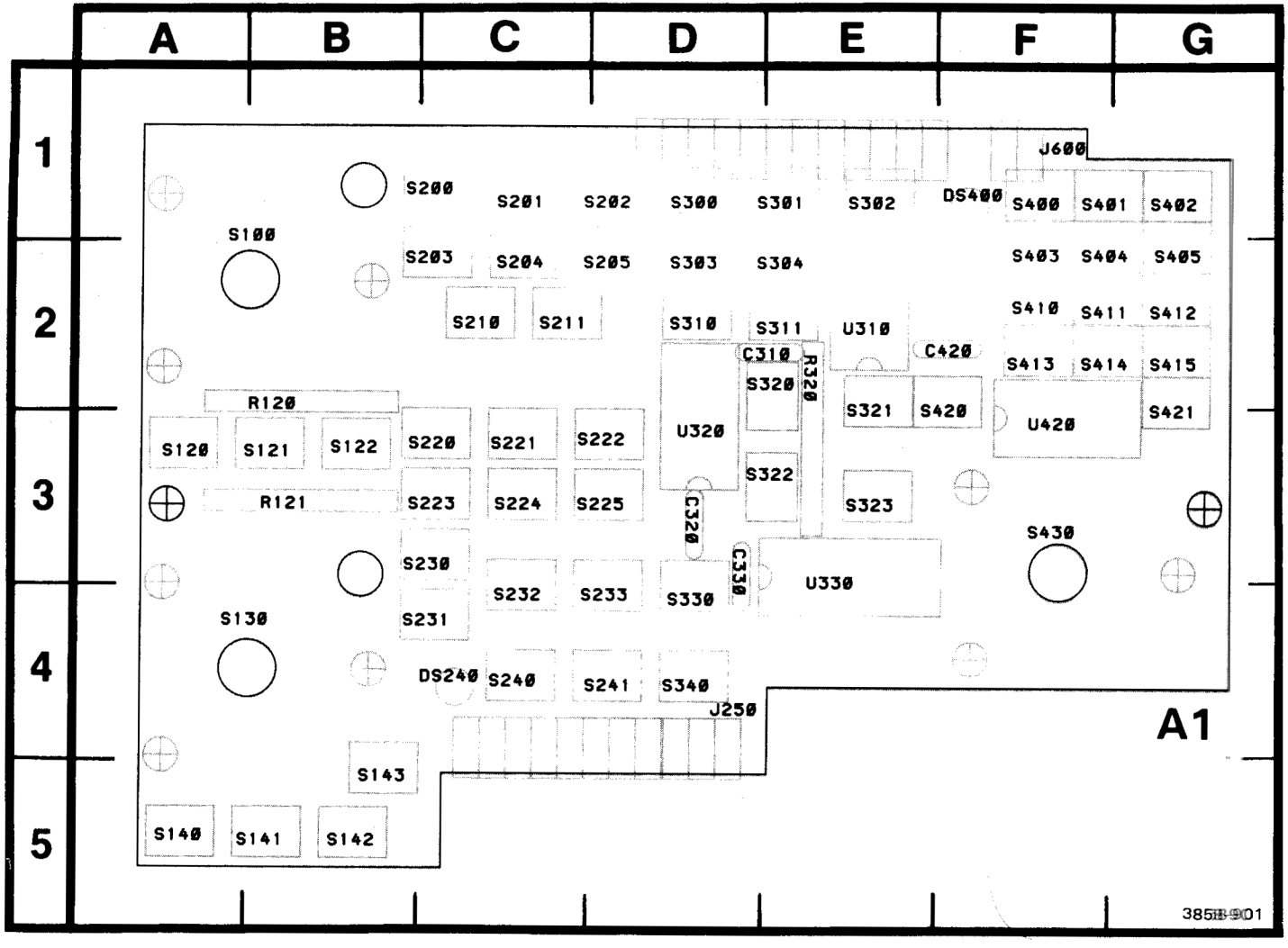
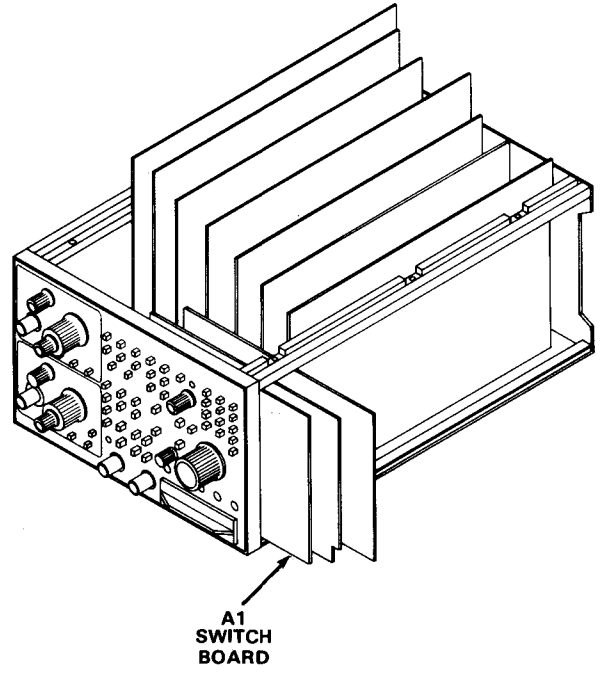


Figure 7-3. A1—Switch circuit board assembly.



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SWITCH BOARD DIAGRAM 1

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C310	A1	E2
C320	A1	D3
C330	A1	D3
C420	A1	F2
DS240	A3	C4
DS400	A2	F1
J250	A3	D4
J600	A1	F1
J600	G1	F1
P250	A4	D4
R120A	F2	B2
R120B	F3	B2
R120C	F1	B2
R120D	F1	B2
R120E	F2	B2
R120F	F2	B2
R120G	F2	B2
R120J	F1	B2
R121	E5	B3
R320	E4	E2
R320	F4	E2
S100	E4	B1
S100	G4	B1
S120	B1	A3
S121	B2	B3
S122	B2	B3
S130	E5	A4
S130	G4	A4
S140	B2	A5
S141	B2	B5
S142	B3	B5
S143	B3	B5
S200	B1	C1
S201	B1	C1
S202	C1	D1
S203	B1	C2
S204	B1	C2
S205	C1	D2
S210	B1	C2
S211	C1	C2
S220	B2	C3
S221	C2	C3
S222	D2	D3
S223	B2	C3
S224	C2	C3
S225	D2	D3
S230	B2	C3
S231	B2	C4
S232	C2	C4
S233	D2	D4
S240	C3	C4
S241	C2	D4
S300	D1	D1
S301	D1	E1
S302	D1	E1
S303	D1	D2
S304	D1	E2
S310	D1	D2
S311	D2	E2
S320	D2	E2
S321	E2	E2
S322	D2	E3
S323	E3	E3
S330	D2	D4
S340	D2	D4
S400	E1	F1
S401	E1	F1
S402	E1	G1
S403	E1	F2
S404	E1	F2
S405	E1	G2
S410	E2	F2
S411	E2	F2
S412	E2	G2
S413	E2	F2
S414	E2	F2
S415	E2	G2
S420	E2	F2
S421	E3	G3
S430	E4	F3
S430	G2	F3
U310	F5	E2
U320	B3	D3
U330	F1	E3
U420	F4	F3

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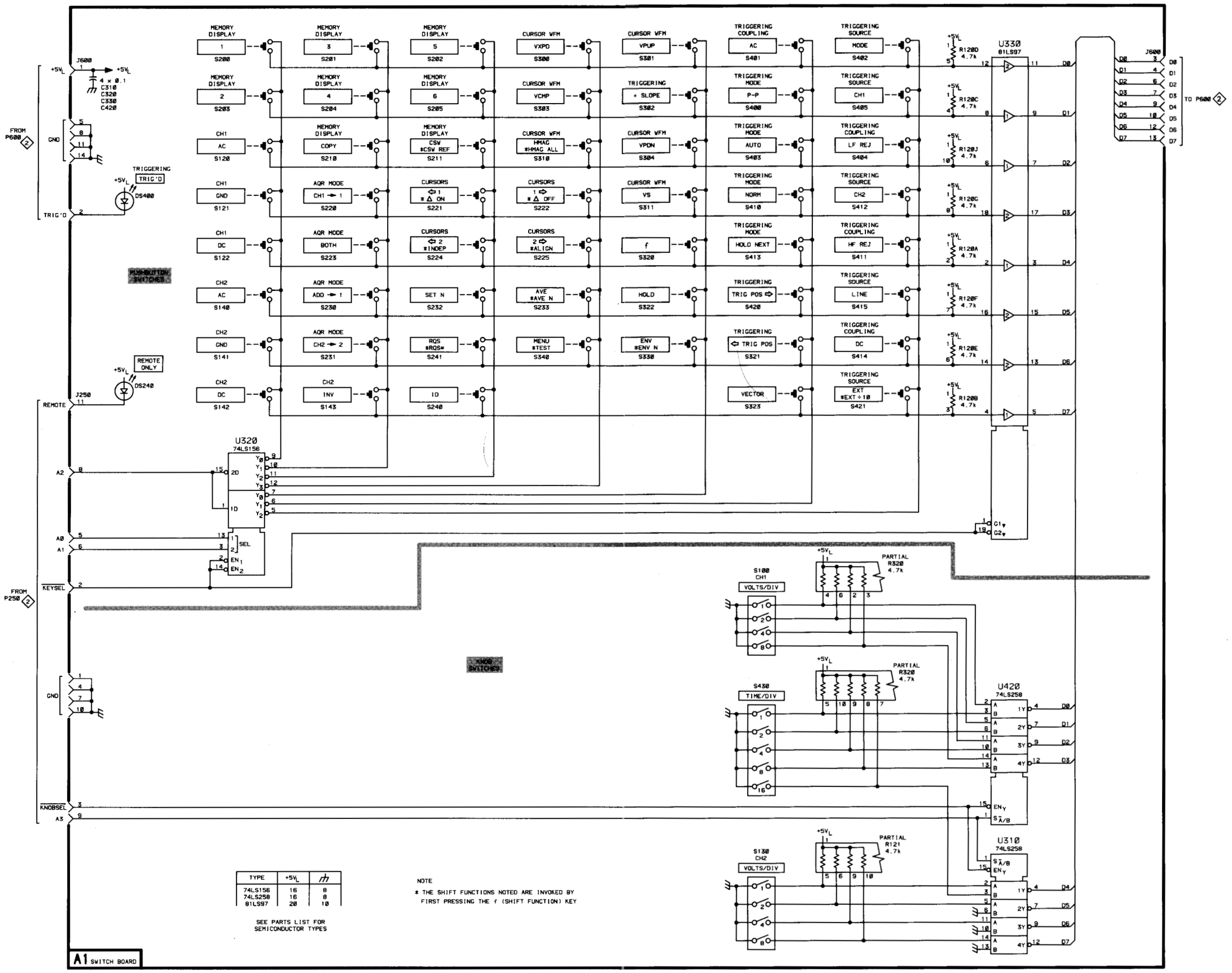

TYPE	+5VL	⏚
74LS156	16	8
74LS258	16	8
81LS97	20	10

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

NOTE

* THE SHIFT FUNCTIONS NOTED ARE INVOKED BY FIRST PRESSING THE f (SHIFT FUNCTION) KEY

A1 SWITCH BOARD

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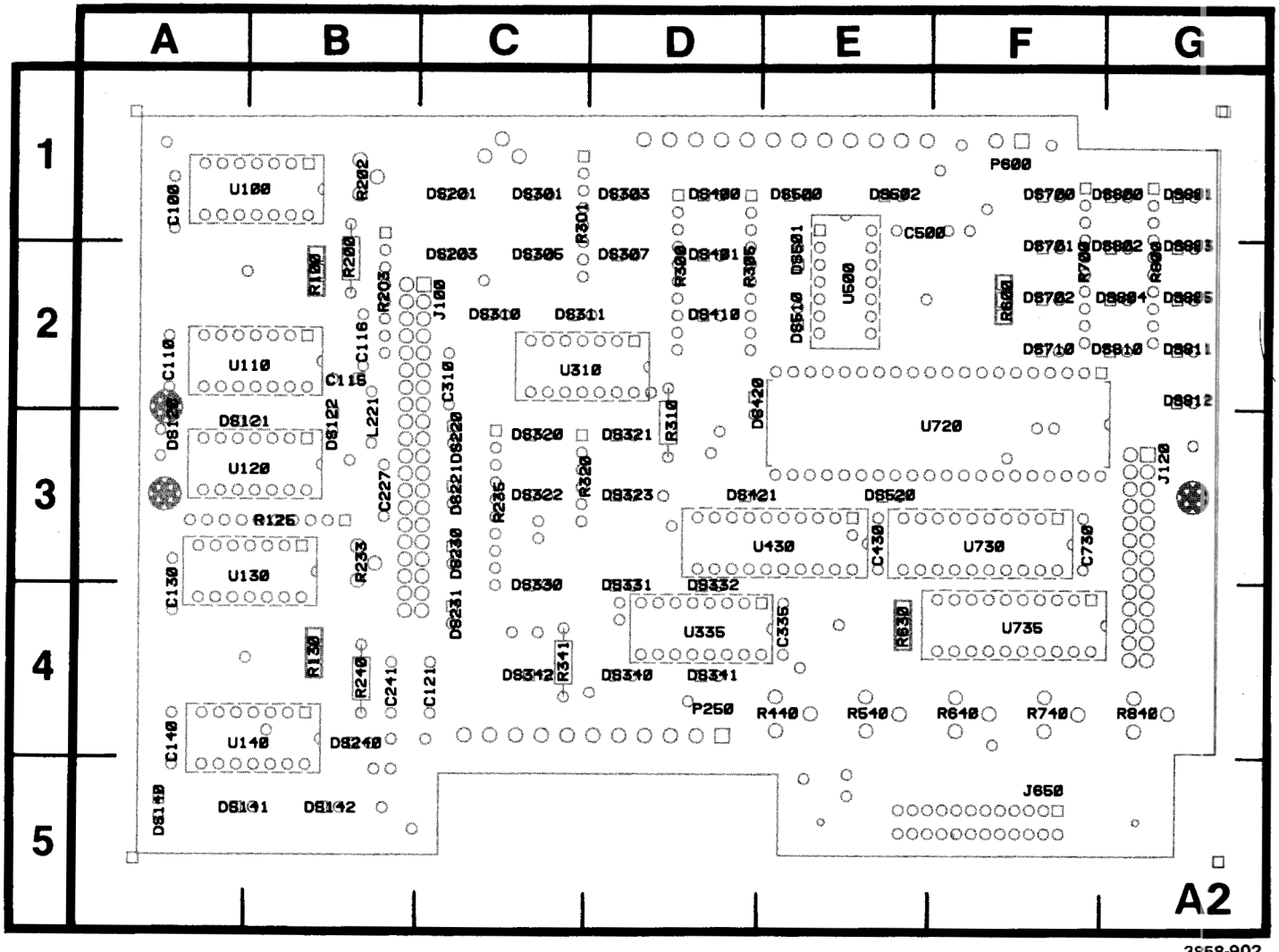
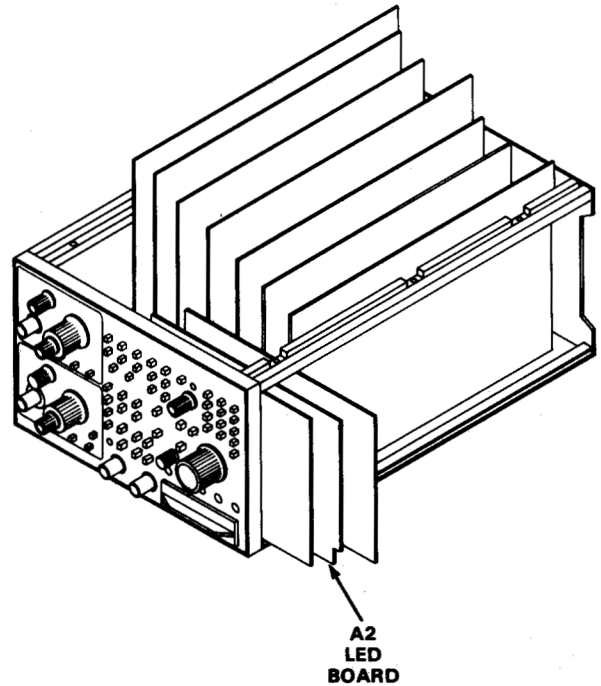


Figure 7-4. A2—LED circuit board assembly.



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LED BOARD DIAGRAM 2

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	A4	A1
C110	A4	A2
C115	A4	B2
C116	A4	B2
C121	A5	C4
C130	A4	A3
C140	A5	A4
C227	A4	B3
C241	A5	B4
C310	A4	C2
C335	A4	E4
C430	A4	E3
C500	A4	E1
C730	A5	F3
DS120	C2	A3
DS121	E3	A3
DS122	C2	B3
DS140	C2	A5
DS141	C2	A5
DS142	C3	B5
DS201	F2	C1
DS203	F1	C2
DS220	G2	C3
DS221	G2	C3
DS230	G1	C3
DS231	G1	C4
DS240	C3	B4
DS301	F3	C1
DS303	F3	D1
DS305	F1	D2
DS307	F2	D2
DS310	F2	C2
DS311	F2	C2
DS320	H2	C3
DS321	H1	D3
DS322	H2	C3
DS323	H1	D3
DS330	G2	C3
DS331	G3	D4
DS332	G3	D4
DS340	G2	D4
DS341	C1	D4
DS342	H2	C4
DS400	E2	D1
DS401	E1	D2
DS410	E1	D2
DS420	E2	D3
DS421	E3	D3
DS500	D1	E1
DS501	D1	E2
DS502	E2	E1
DS510	D2	E2
DS520	E2	E3
DS700	D3	F1
DS701	D3	F2
DS702	D2	F2
DS710	D2	F2
DS800	D2	G1
DS801	E1	G1
DS802	E3	G2
DS803	E3	G2
DS804	E1	G2
DS805	E2	G2
DS810	E2	G2
DS811	E2	G2
DS812	E2	G2
J650	D5	F5
L221	A4	B3
P250	H1	D4
P250	H4	D4
P600	H3	F1
R100	A1	B2
R125A	C2	B3
R125B	C3	B3
R125E	C2	B3
R125F	C3	B3
R125G	F3	B3
R125H	C2	B3
R125J	C2	B3
R130	A2	B4
R200	A1	B2
R202	A3	B1
R203A	A5	B2
R203C	A5	B2
R203D	A5	B2
R203	H5	B2
R233	A3	B3
R235A	G2	C3
R235B	H2	C3
R235C	G2	C3
R235D	G3	C3
R235E	G2	C3
R235F	G2	C3
R235G	G3	C3
R235H	G1	C3
R235J	G1	C3
R240	A2	B4
R300A	F3	D2
R300B	F3	D2
R300C	F2	D2
R300D	C1	D2
R300E	F2	D2
R300F	F1	D2
R300G	F2	D2
R300H	F1	D2
R300J	F2	D2
R301A	A5	C1
R301B	A5	C1
R301C	A5	C1
R301D	A5	C1
R301	H5	C1
R305A	F2	D2
R305B	F1	D2
R305C	F2	D2
R305E	F1	D2
R305G	F3	D2
R305H	F2	D2
R305J	F2	D2
R310	H3	D3
R320A	H2	C3
R320B	H1	C3
R320C	H2	C3
R320D	H1	C3
R320E	C3	C3
R341	C1	C4
R440	A2	E4
R540	A2	E4
R600	A1	F2
R630	A2	E4
R640	A3	F4
R700A	D2	F2
R700B	D3	F2
R700C	D3	F2
R700E	D2	F2
R700F	D2	F2
R700G	D1	F2
R700H	D1	F2
R700J	D2	F2
R740	A3	F4
R800A	E1	G2
R800B	E3	G2
R800C	E3	G2
R800E	E2	G2
R800F	E1	G2
R800G	E2	G2
R800H	E2	G2
R800J	E2	G2
R840	A3	G4
U100	D1	A1
U110	E1	A2
U120	F1	A3
U130	G1	A3
U140	C1	B4
U310	G1	C2
U335	B4	D4
U430	B4	E3
U500	D1	E2
U720	C4	F3
U730	D4	F3
U735	D5	F4

Partial A2 also shown on diagrams 5, 7, 8 and 9.

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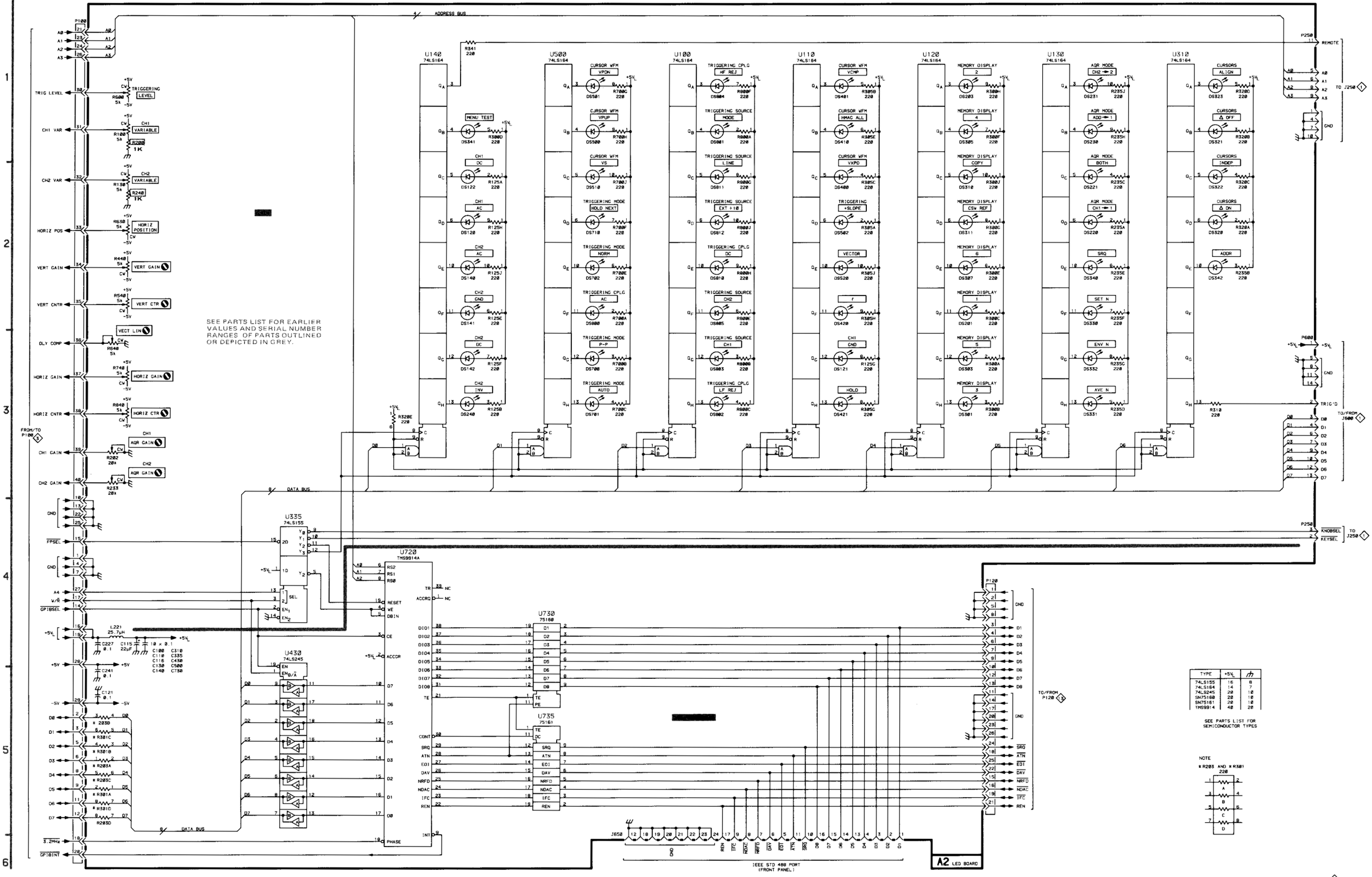

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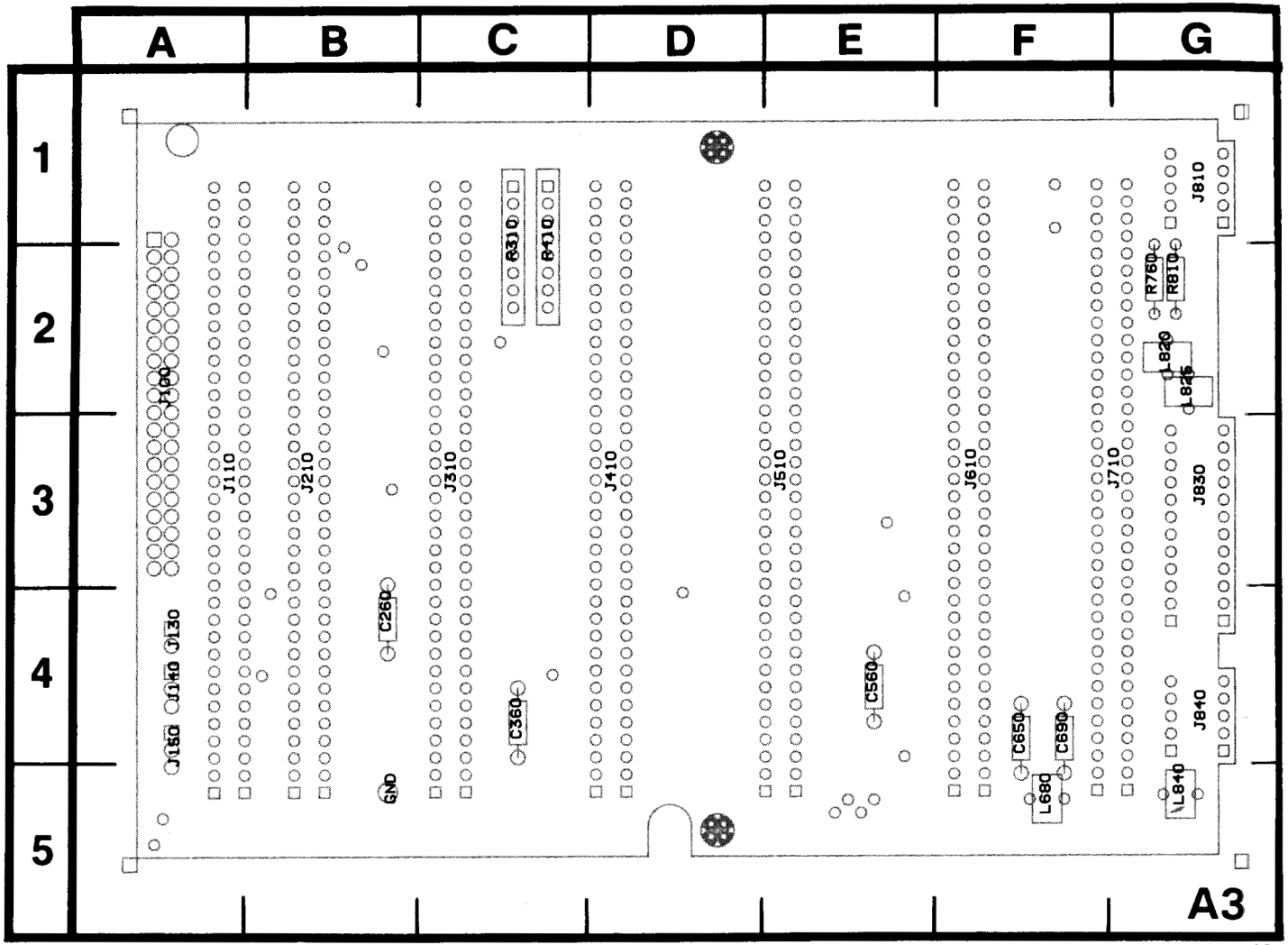
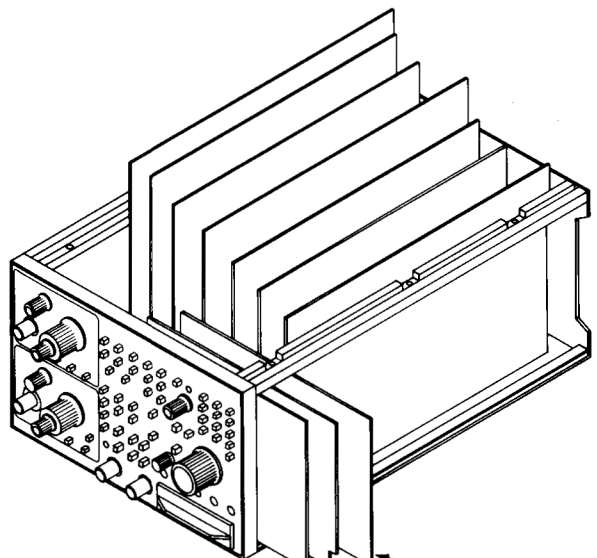


3958-903

Figure 7-5. A3—Interconnect circuit board assembly.



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INTERCONNECT DIAGRAM 3

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C260	F5	B4	J410	E6	D3	L825	A3	G2
C360	A3	C4	J510	D1	E3	L840	A4	G5
C560	A3	E4	J510	D6	E3			
C650	A3	F4	J610	C1	F3	R310A	E1	C1
C690	G5	F4	J610	C6	F3	R310B	E1	C1
			J710	B1	G3	R310C	E1	C1
J110	G1	A3	J710	B6	G3	R310D	E1	C1
J110	G6	A3	J810	A1	G1	R410A	E1	C1
J210	F1	B3	J830	A3	G3	R410B	E1	C1
J210	F6	B3	J840	A5	G4	R410C	E1	C1
J310	E1	C3				R410D	E1	C1
J310	E6	C3	L680	A3	F5	R760	A2	G2
J410	E1	D3	L820	A3	G2	R810	B2	G2

Partial A3 also shown on diagram 5.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	
R10	I5	CHASSIS	R20	I5	CHASSIS	

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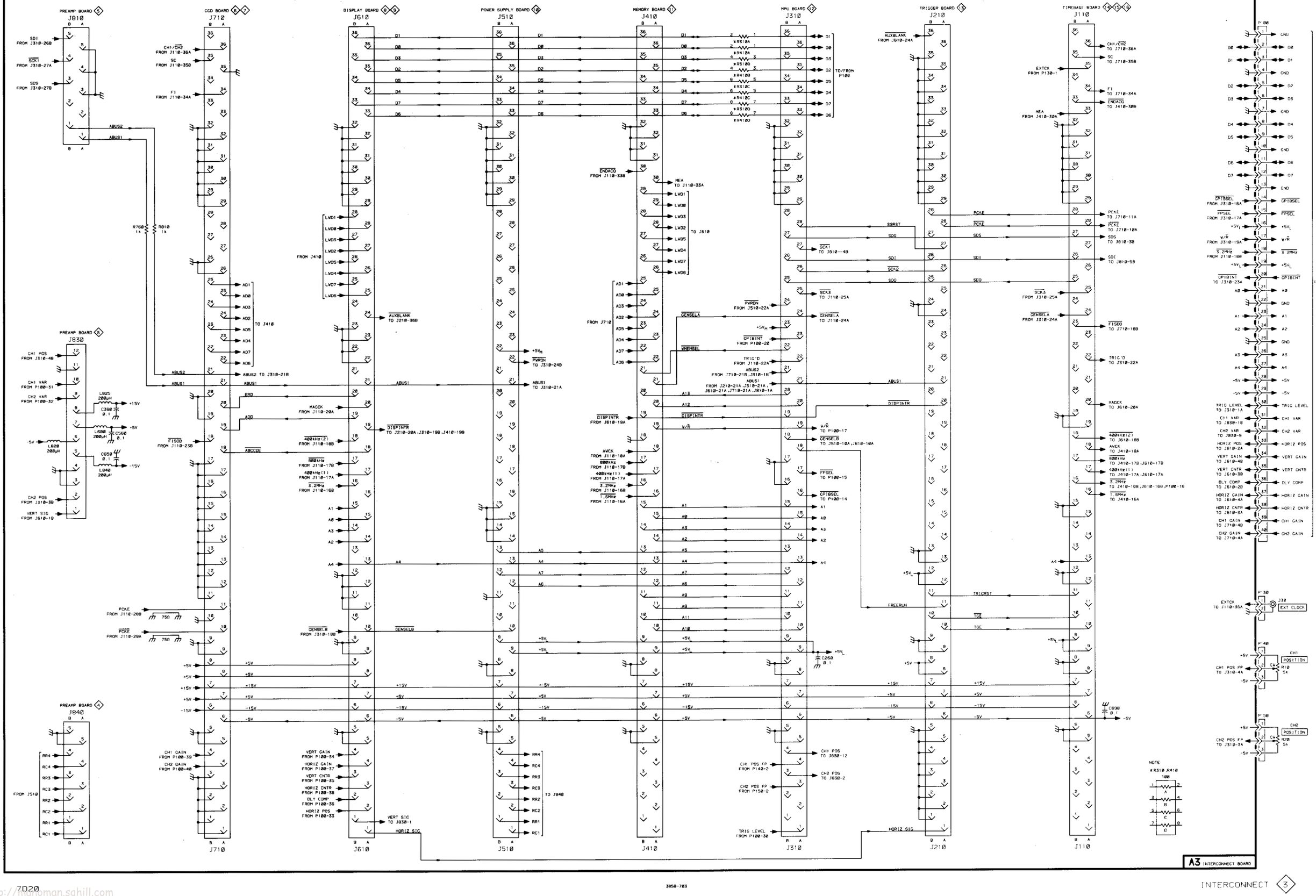

3058-703

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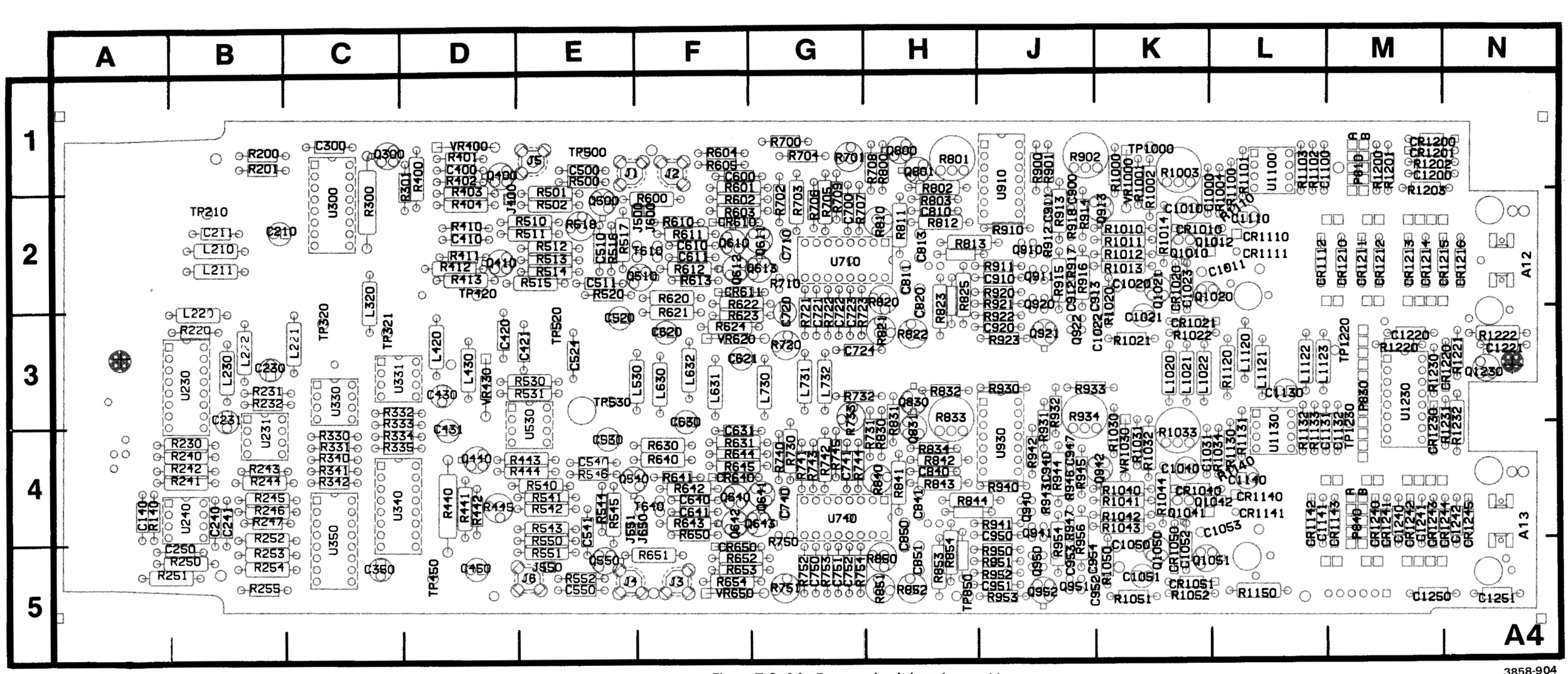
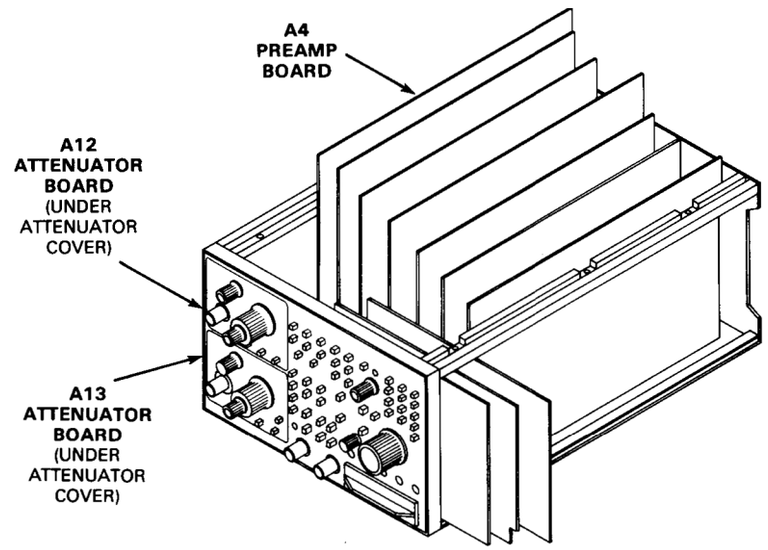


3858-904

Figure 7-6. A4—Preamp circuit board assembly.



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CH1 AND CH2 ATTENUATOR DIAGRAM 4

ASSEMBLY A4

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C900	F2	J2
C911	F2	J2
C912 *	F2	J2
C913 *	F2	J2
C940	F4	J4
C947	F4	J4
C952	F4	J5
C953 *	F4	J5
C954 *	F4	J5
C1000	E1	L2
C1010	B5	K2
C1011	D1	L2
C1020	D2	K2
C1021	C4	K3
C1022	F2	K3
C1023	E2	K2
C1031	E3	K4
C1040	B5	K4
C1050	D4	K5
C1051	C4	K5
C1052	E4	K5
C1053	D4	L4
C1100	D1	L1
C1110	B4	L2
C1130	C5	L3
C1131	D3	L4
C1140	B4	L4
C1141	C2	L4
C1200	A1	M1
C1221	B2	N3
C1240	B2	M4
C1241	B2	M4
C1242	A2	N4
C1250	A4	M5
C1251	B3	N5
CR1010	D2	K2
CR1020	D2	K2
CR1021	E2	K3
CR1040	D4	K4
CR1050	D4	K5
CR1051	E5	K5
CR1110	D1	L2
CR1111	D1	L2
CR1112	C2	L2
CR1140	D3	L4
CR1141	D4	L4
CR1142	C3	L4
CR1143	C3	M4
CR1200	A1	M1
CR1201	A1	M1
CR1210	C2	M2
CR1211	B2	M2
CR1212	B2	M2
CR1213	B2	M2
CR1214	B2	M2
CR1215	A2	M2
CR1216	A2	N2
CR1220	A4	N3
CR1230	A4	M4
CR1240	B3	M4
CR1241	B3	M4
CR1242	B3	M4
CR1243	B3	M4
CR1244	A3	M4
CR1245	A3	N4
L1020	C4	K3
L1021	C4	K3
L1022	B5	K3
L1120	B5	L3
L1121	C5	L3
L1122	B4	L3
L1123	B4	L3
P840	A2	M4
Q910	G2	J2
Q911	F2	J2
Q913	E1	K2
Q920	F2	J2
Q921	F1	J3
Q922	F2	J3
Q940	G4	J4
Q941	F4	J4
Q942	E3	K4
Q950	F4	J5
Q951	F4	J5
Q952	F4	J5
Q1010	E1	K2
Q1012	D1	L2
Q1020	D2	K2
Q1020	G3	K2
Q1021	E2	K2
Q1041	E4	K4
Q1042	D3	K4
Q1050	E4	K5
Q1051	D5	K5
Q1051	G3	K5
Q1230	B2	N3
R900	E1	J1
R901	E1	J1
R902	C1	J1
R910	F1	J2
R911	F1	J2
R912	F2	J2
R913	F2	J2
R914	E2	J2
R915	F2	J2
R916	F2	J2
R917	F2	J2
R918	F2	J2
R920	F2	J2
R923	F1	J3
R930	E3	J3
R931	E3	J4
R932	E4	J3
R933	E3	J3
R934	C4	J3
R940	F3	J4
R941	F4	J4
R942	E3	J4
R943	F4	J4
R944	F4	J4
R945	E4	J4
R946	F4	J4
R947	F4	J4
R950	F4	J5
R953	F4	J5
R954	F4	J5
R956	F4	J5
R1000	D1	K1
R1001	D1	K1
R1002	D2	K1
R1003	D2	K1
R1004	D1	L2
R1010	E2	K2
R1011	E2	K2
R1012	E2	K2
R1013	E2	K2
R1014	D2	K2
R1020 *	F2	K2
R1021	C4	K3
R1022	E2	K3
R1030	D3	K4
R1031	D3	K4
R1032	D4	K4
R1033	D4	K4
R1034	D3	L4
R1040	E4	K4
R1041	E4	K4
R1042	E4	K4
R1043	E4	K4
R1044	D4	K4
R1050 *	F4	K5
R1051	C4	K5
R1052	E5	K5
R1100	D1	L2
R1101	D1	L1
R1102	D1	L1
R1103	D1	L1
R1110	D1	L2
R1120	D2	L3
R1130	D4	L4
R1131	D4	L4
R1132	D4	L4
R1133	D4	L4
R1140	D3	L4
R1150	D5	L5
R1202	A1	M1
R1221	B2	N3
R1222	B2	N3
R1230	B2	M3
R1231	A4	N4
R1232	B3	N4
U910	F1	J1
U930	F3	J4
U1100	D1	L1
U1130	D3	L4
VR1000	E1	K1
VR1030	E3	K4

Partial A4 also shown on diagrams 5 and 9.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1	A1	CHASSIS
C2	A3	CHASSIS
J1	A1	CHASSIS
J2	A3	CHASSIS

***See Parts List for serial number ranges.**

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VOLTAGE CONDITIONS

Use a digital voltmeter with a 10 MΩ input impedance such as the TEKTRONIX DM 501A Digitial Multimeter installed in a TM 500- or TM 5000-series power module, or a TEKTRONIX 7D13A Digital Multimeter in a readout-equipped Tektronix 7000-series oscilloscope mainframe. Connect the voltmeter ground lead to A4TP1000.

Setup the 7D20 as follows:

Set the CH 1 and CH 2 POSITION controls to midrange.

To horizontally center the display, rotate the HORIZ POSITION control fully clockwise into the switch detent.

Initialize the 7D20 control settings as follows:

a. Press MENU (pushbutton will light).

b. If MASTER MENU is not displayed, press MEMORY DISPLAY pushbutton number 6.

c. From displayed MASTER MENU list select UTILITIES by pressing MEMORY DISPLAY pushbutton number 4.

d. From displayed UTILITIES list select INIT FRONT PANEL by pressing MEMORY DISPLAY pushbutton number 5.

e. To return to MASTER MENU, press MEMORY DISPLAY pushbutton number 6. To turn off MASTER MENU display, press MENU.

Selectable Electrical Parts Table
For Diagram 4

Component Number	Reason For Selection	Component Value (See Replaceable Electrical Parts)
A4C900 A4C911 A4C912 A4R917 A4R918	To improve transient response. This may be required when semiconductors are replaced in the CH 1 Impedance Converter Amplifier and CH 1 Step Attenuator blocks.	0.5 pF - 2.2 pF 0.5 pF - 1.8 pF 2.2 pF - 10 pF 910 Ω nominal 1.1 kΩ nominal
A4C940 A4C947 A4C953 A4R946 A4R947	To improve transient response. This may be required when semiconductors are replaced in the CH 2 Impedance Converter Amplifier and CH 2 Step Attenuator blocks.	0.5 pF - 1.8 pF 0.5 pF - 2.2 pF 2.2 pF - 10 pF 1.1 kΩ nominal 910 Ω nominal
A4R1020 A4R1050	To compensate for HF variations in FET's Q922, Q920, Q951 & Q950, use lower resistance to roll response and higher to peak response (20 & 50 mV/div settings).	13Ω, 18Ω & 24Ω

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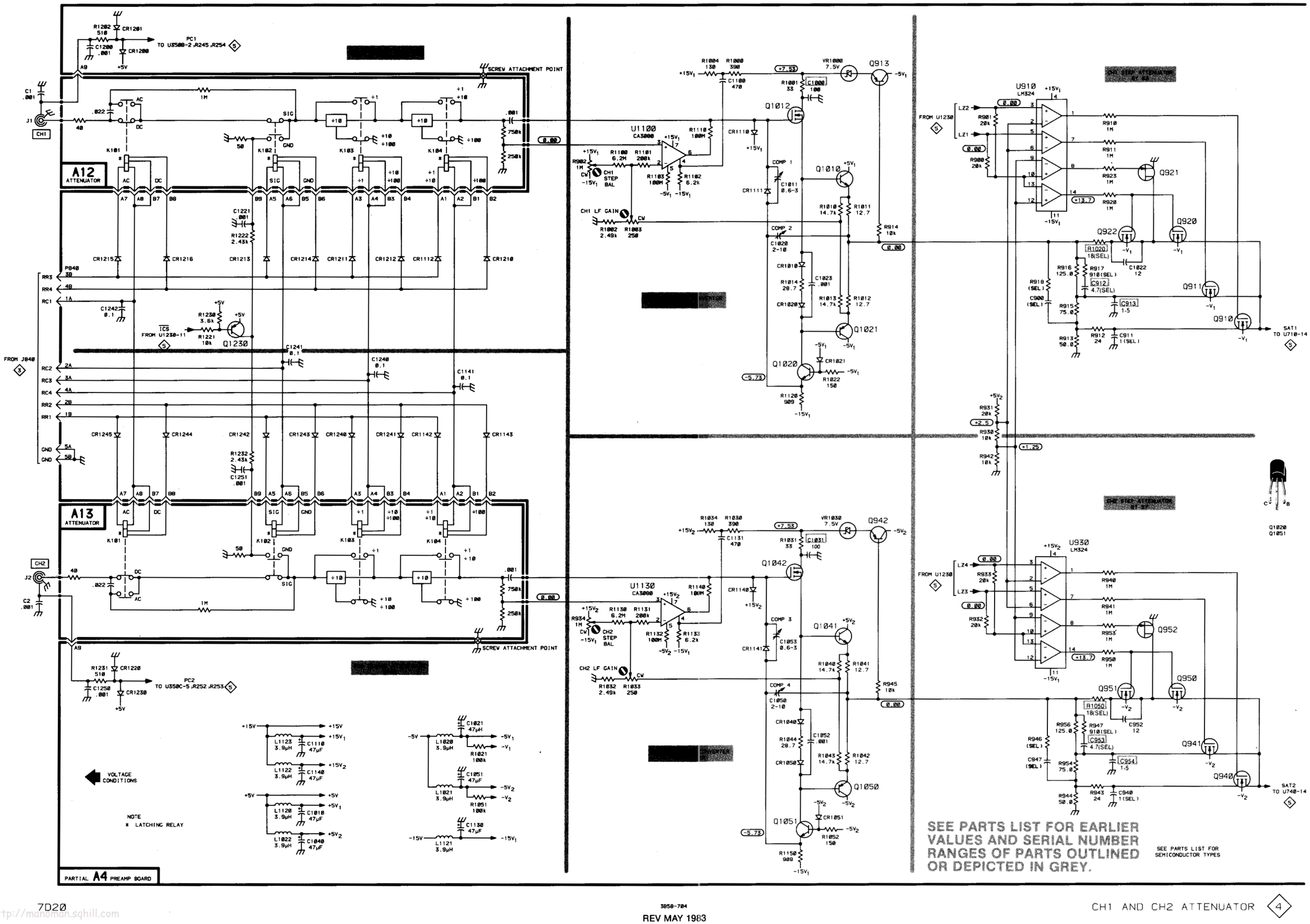

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VERTICAL PREAMP AND CONTROL DIAGRAM 5

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
R100	A4	B2	R130	A4	B4	R200	A4	B2
						R240	A4	B4

Partial A2 also shown on diagrams 2, 7, 8 and 9.

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
L820	A2	G2

Partial A3 also shown on diagram 3.

ASSEMBLY A4

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C140	B6	A4	C920	C1	J3	Q611	E2	G2	R443	F5	E4	R700	C2	G1	R853	D5	H5
C210	B6	B2	C950	C5	J4	Q612	E1	F2	R444	F6	E4	R701	D2	G1	R854	C5	H5
C211	A6	B2	C951	C5	J5	Q613	E2	G2	R445	F5	D4	R702	E2	G2	R921	C1	J2
C230	B5	B3	C1132	B3	M4	Q640	E6	F4	R500	F2	E1	R703	E2	G2	R922	C1	J3
C231	B3	B3	C1220	B5	M3	Q641	E6	G4	R501	F2	E1	R704	D1	G1	R951	C5	J5
C240	B4	B4				Q642	E5	F4	R502	F2	E2	R705	D3	G2	R952	C5	J5
C241	F4	B4	CR610	E2	F2	Q643	E5	G4	R510	F2	E2	R706	D1	G2	R1200	A1	M1
C250	F4	B5	CR611	E1	F2	Q800	C2	H1	R511	F2	E2	R707	D2	G2	R1201	A1	M1
C300	B6	C1	CR640	E6	F4	Q801	C1	H1	R512	F2	E2	R708	C2	H1	R1203	A1	M2
C350	B6	C5	CR650	E5	F5	Q830	C6	H3	R513	F2	E2	R709	D2	G2	R1220	B5	M3
C400	F3	D1				Q831	C5	H4	R514	F2	E2	R710	E2	G2			
C410	F1	D2	J1	F1	F1				R515	F1	E2	R720	D3	G3	T610	E1	F2
C420	A4	D3	J2	F1	F1	R140	F4	A4	R516	F2	E2	R721	D3	G3	T640	E6	F4
C421	A5	E3	J3	G6	F5	R200	G4	B1	R517	F2	E2	R722	D2	G3			
C430	B5	D3	J4	G6	E5	R201	G4	B1	R518	F2	E2	R723	D3	G3	TP210	A5	B2
C431	B3	D4	J5	G2	E1	R220	E4	B3	R520	F1	E2	R730	E5	G4	TP320	B4	C3
C450	B6	D5	J6	G6	E5	R230	G5	B4	R530	F2	E3	R731	C6	H4	TP321	B5	C3
C500	F3	E1	J400	G2	D2	R231	D3	B3	R531	F2	E3	R732	C5	G3	TP420	B6	D2
C510	F2	E2	J500	E1	F2	R232	F3	B3	R540	F6	E4	R733	D6	G3	TP450	A5	D5
C511	F1	E2	J550	G6	E5	R240	G4	B4	R541	F6	E4	R740	E6	G4	TP500	A6	E1
C520	B4	E3	J551	G6	E4	R241	F4	B4	R542	F6	E4	R741	D6	G4	TP520	A6	E3
C524	B2	E3	J600	E1	F2	R242	F4	B4	R543	F5	E4	R742	D5	G4	TP850	A6	H5
C530	B5	E4	J650	G6	F4	R243	D4	B4	R544	F6	E4	R743	D6	G4	TP1000	A6	K1
C540	F6	E4				R244	D3	B4	R545	F5	E4	R744	D6	G4	TP1220	B3	M3
C541	F5	E4	L210	A6	B2	R245	D3	B4	R546	F6	E4	R745	D6	G4	TP1230	B3	M4
C550	F5	E5	L211	A4	B2	R246	E4	B4	R550	F5	E4	R750	E5	G5			
C600	E2	F1	L220	A5	B3	R247	E4	B4	R551	F5	E5	R751	D4	G5	U230	G3	B3
C610	E2	F2	L221	B6	C3	R250	F4	B5	R552	F5	E5	R752	D4	G5	U231A	D4	B4
C611	E1	F2	L222	B5	B3	R251	F4	B5	R600	F2	F2	R753	C5	G5	U231B	E4	B4
C620	B5	F3	L230	A3	B3	R252	E4	B4	R601	E2	F1	R754	D4	G5	U240A	F4	B4
C621	B2	F3	L320	B6	C3	R253	E4	B5	R602	E3	F2	R800	C1	H1	U240B	F4	B4
C630	B5	F3	L420	B5	D3	R254	D3	B5	R603	E2	F2	R801	C1	H1	U300	B2	C2
C631	B5	F4	L430	A3	D3	R255	F4	B5	R604	C1	F1	R802	C2	H1	U330A	C3	C3
C640	E6	F4	L530	B4	F3	R300	C2	C2	R605	C2	F1	R803	D2	H2	U330B	C4	C3
C641	E5	F4	L630	B5	F3	R301	C2	D1	R610	F2	F2	R810	D2	H2	U331	C5	C3
C700	D1	G2	L631	B5	F3	R330	C3	C4	R611	E2	F2	R811	D2	H2	U340A	C4	C4
C710	E2	G2	L632	B5	F3	R331	C3	C4	R612	E1	F2	R812	C2	H2	U340C	C4	C4
C720	B6	G3	L730	A2	G3	R332	C4	C3	R613	F1	F2	R813	C1	H2	U340D	C5	C4
C721	D3	G3	L731	B6	G3	R333	C4	C3	R620	F2	F2	R820	D1	H2	U340	B1	C4
C722	D2	G3	L732	B6	G3	R334	C4	C4	R621	B5	F3	R821	D3	H3	U350B	D4	C4
C723	D1	G3				R335	C5	C4	R622	E1	F2	R822	D1	H3	U350C	E4	C4
C724	B3	G3	P810	A1	M1	R340	C4	C4	R623	E1	F3	R823	D1	H3	U350	C1	C4
C740	E6	G4	P810	G4	M1	R341	C4	C4	R624	E1	F3	R825	C1	H2	U530A	F5	E3
C741	D6	G4	P830	A2	M3	R342	C3	C4	R630	B5	F4	R830	C5	H4	U530B	F2	E3
C750	D4	G5	P830	F4	M3	R400	C1	D1	R631	E6	F4	R831	C6	H4	U710	D1	G2
C751	D5	G5	P830	G3	M3	R401	F3	D1	R640	F6	F4	R832	C6	H3	U740	D6	G4
C752	D6	G5				R402	F2	D1	R641	F6	F4	R833	C5	H3	U1230	B1	M3
C810	D2	H2	Q300	C2	C1	R403	F2	D1	R642	E6	F4	R834	D6	H4			
C811	D1	H2	Q400	F3	D1	R404	F2	D2	R643	E5	F4	R840	D6	H4	VR400	C2	D1
C813	D2	H2	Q410	F1	D2	R410	F1	D2	R644	E6	F4	R841	D6	H4	VR430	C6	D3
C820	D1	H2	Q440	C5	D4	R411	F1	D2	R645	E6	F4	R842	C6	H4	VR620	D1	F3
C840	D6	H4	Q500	F3	E2	R412	F1	D2	R650	F5	F4	R843	C5	H4	VR650	D4	F5
C841	D6	H4	Q510	F1	F2	R413	F1	D2	R651	F5	F5	R844	C5	H4			
C850	D5	H4	Q540	F6	E4	R440	C5	D4	R652	E5	F5	R850	D5	H5			
C851	D5	H5	Q550	F5	E5	R441	C5	D4	R653	E5	F5	R851	D4	H5			
C910	C1	J2	Q610	E2	F2	R442	C5	D4	R654	E5	F5	R852	D5	H5			

Partial A4 also shown on diagrams 4 and 9.

ASSEMBLY A9

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P310	A1	L3	P310	H4	L3

Partial A9 also shown on diagrams 9 and 12.

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VOLTAGE CONDITIONS

Use a digital voltmeter with a 10 MΩ input impedance such as the TEKTRONIX DM 501A Digitial Multimeter installed in a TM 500- or TM 5000-series power module, or a TEKTRONIX 7D13A Digital Multimeter in a readout-equipped Tektronix 7000-series oscilloscope mainframe. Connect the voltmeter ground lead to A4TP1000.

Setup the 7D20 as follows:

Set the CH 1 and CH 2 POSITION controls to midrange.

To horizontally center the display, rotate the HORIZ POSITION control fully clockwise into the switch detent.

Initialize the 7D20 control settings as follows:

a. Press MENU (pushbutton will light).

b. If MASTER MENU is not displayed, press MEMORY DISPLAY pushbutton number 6.

c. From displayed MASTER MENU list select UTILITIES by pressing MEMORY DISPLAY pushbutton number 4.

d. From displayed UTILITIES list select INIT FRONT PANEL by pressing MEMORY DISPLAY pushbutton number 5.

e. To return to MASTER MENU, press MEMORY DISPLAY pushbutton number 6. To turn off MASTER MENU display, press MENU.

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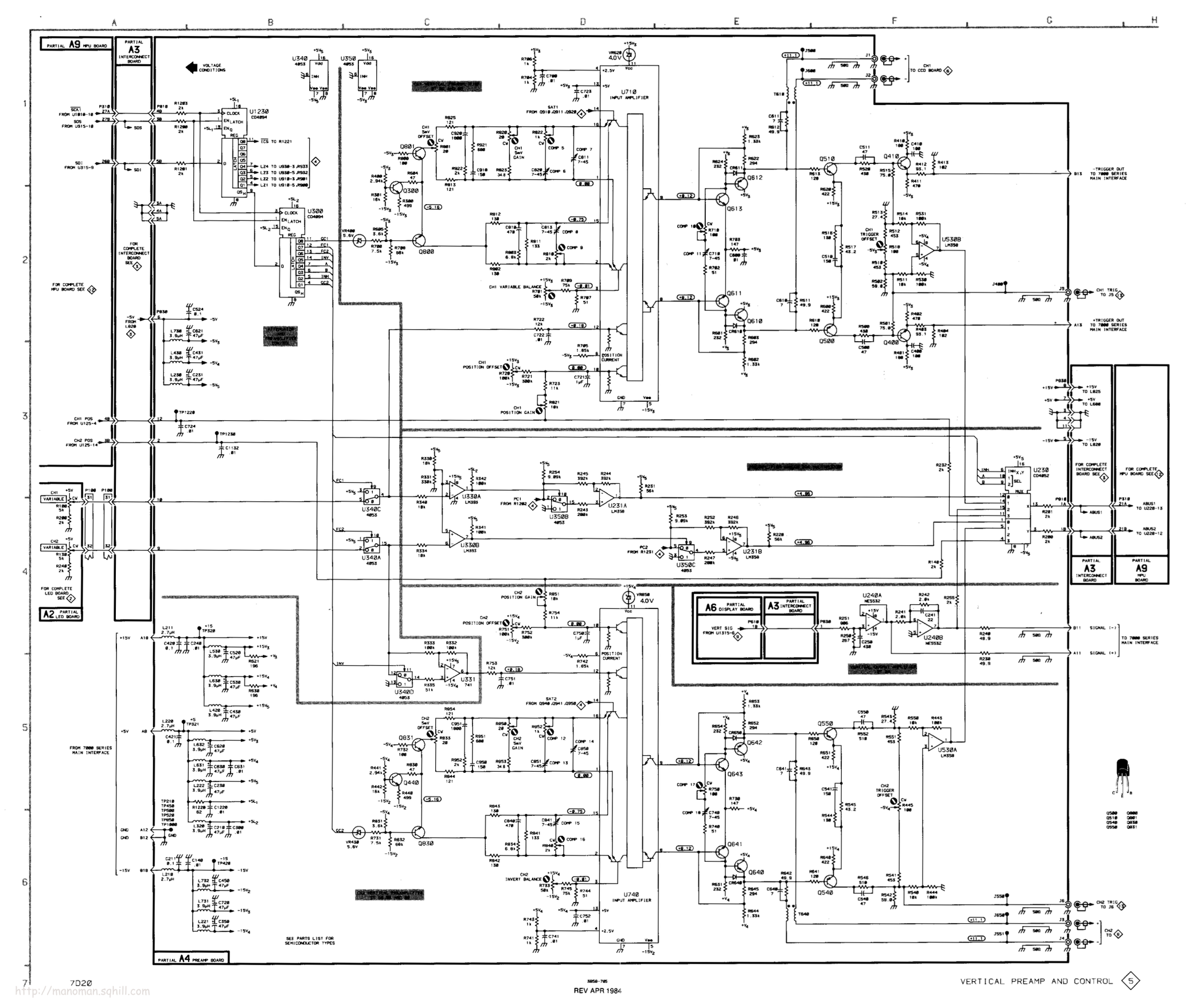

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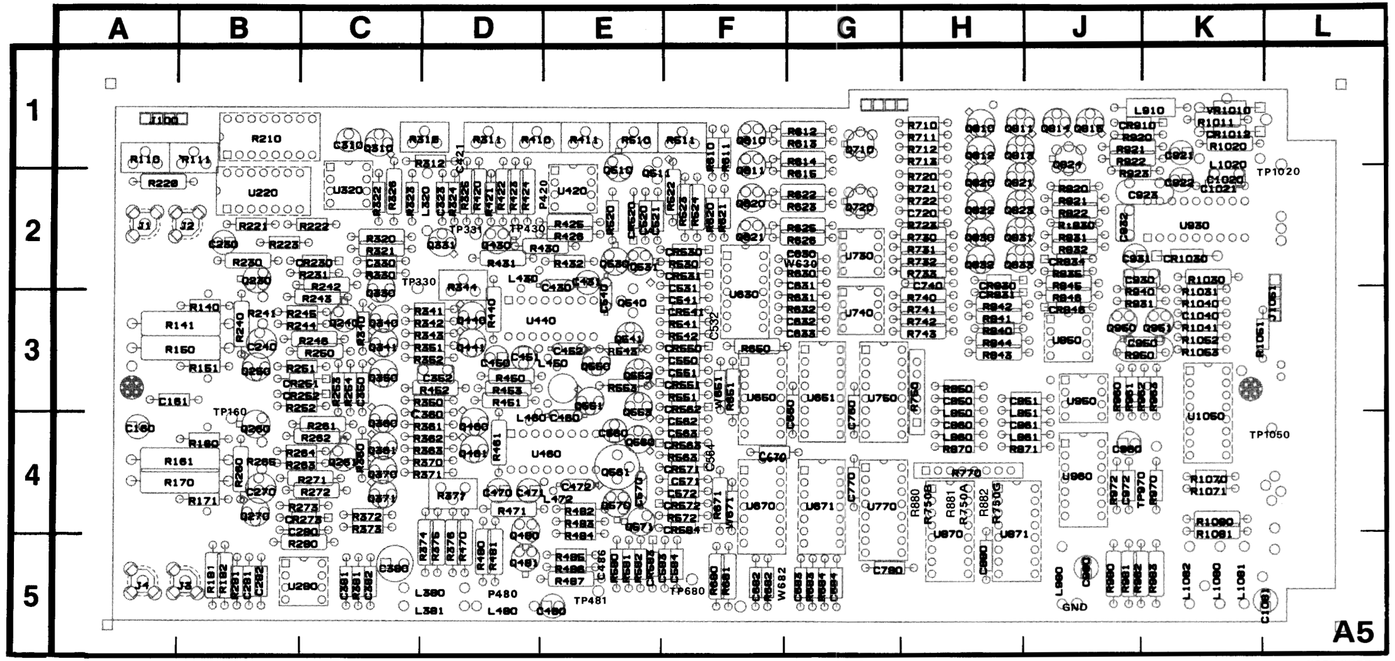
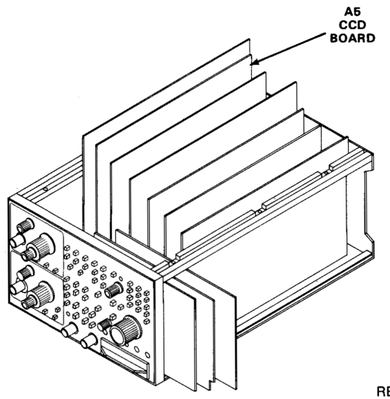


Figure 7-7. A5—CCD circuit board assembly.



CCD DRIVERS DIAGRAM ◈6

ASSEMBLY A5

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C160	G1	A4
C161	G1	A3
C230	G2	B2
C240	B3	B3
C270	B5	B4
C280	C5	C4
C281	B5	B5
C282	B4	B5
C310	F1	C1
C323	F1	D2
C330	C4	C2
C350	C6	C3
C352	F6	D3
C360	C6	D4
C380	G2	C5
C381	B5	C5
C382	B5	C5
C430	F3	E2
C431	G5	E2
C450	G3	D3
C451	F4	D3
C452	F4	E3
C460	F5	E4
C470	G5	D4
C471	F6	D4
C472	F6	E4
C480	G1	E5
C520	C1	E2
C521	C1	E2
C531 ●	D1	F2
C532 ●	G1	F3
C540	G1	E3
C541 ●	D2	F3
C550	E2	F3
C551	E2	F3
C560	G5	E4
C562	D2	F4
C563	D2	F4
C564 ●	G1	F4
C570	G1	E4
C571 ●	D2	F4
C572 ●	D3	F4
C583	E3	F5
C584	E3	F5
C630	G1	G2
C631	C1	G2
C632	C1	G3
C633 ●	D1	G3
C660	G2	G4
C670	G1	F4
C682 ●	D3	F5
C683	C3	G5
C684	C3	G5
C760	G2	G4
C770	G1	G4
P710	A1	G1
P710	H1	G1
Q230	B4	B2
Q240	B4	C3
Q250	B3	B3
Q260	B6	B4
Q261	B6	C4
Q270	B5	B4
Q310	F1	C1
Q330	B4	C3
Q340	C4	C3
Q341	C3	C3
Q350	B3	C3
Q360	B6	C4
Q361	C6	C4
Q370	C5	C4
Q371	B5	C4
Q440	C3	D3
Q441	C4	D3
Q460	C5	D4
Q461	C6	D4
Q530	D1	E2
Q531	D1	E2
Q540	D1	E3
Q541	D2	E3
Q550	E2	E3
Q551	E2	E3
Q552	E2	E3
Q553	E2	E4
Q560	D3	E4
Q561	D2	E4
Q570	E3	E4
Q571	E3	E4
R110	F6	A1
R111	F5	B1
R140	A4	B3
R141	A4	A3
R450	A3	A3
R151	A3	B3
R160	A6	B4
R161	A6	A4
R170	A5	A4
R171	A5	B4
R181	B5	B5
R182	B5	B5
R210A	F6	B1
R210B	F5	B1
R210C	F4	B1
R210D	F3	B1
R220	F6	A2
R221	F5	B2
R222	F4	C2
R223	F6	B2
R230	C5	B2
R231	B4	C2
R240	A4	B3
R241	B4	B3
R242	B4	C2
R243	B4	C3
R244	B4	C3
R245	B4	C3
R246	B3	C3
R250	B3	C3
R251	B3	C3
R252	B6	C3
R253	B4	C3
R254	B4	C3
R260	A6	B4
R261	B6	C4
R262	B6	C4
R263	B6	C4
R264	B5	C4
R265	B6	B4
R271	B5	C4
R272	B5	C4
R273	B5	C4
R280	C5	C5
R281	B5	B5
R310	F4	D1
R311	F3	D1
R312	F3	D1
R320	F1	C2
R321	F1	C2
R322	F1	C2
R323	F1	C2
R326	F3	C2
R330 ●	C4	C2
R340	C4	C3
R341	C4	D3
R342	C3	D3
R343	C4	D3
R344	D3	D2
R350 ●	C6	D3
R351	C3	D3
R352 ●	C4	D3
R360	C6	C4
R361 ●	C6	D4
R362	C6	D4
R363	C5	D4
R370	C6	D4
R371	C5	D4
R372	B5	C4
R373	B5	C4
R374	D4	D5
R375	D4	D5
R376	D6	D5
R377	C6	D4
R381	B5	C5
R431	D3	D2
R432	E2	E2
R440	D4	D3
R450	D4	D3
R451	D5	D3
R452	F6	D3
R453	F4	D3
R461	D5	D4
R470	D6	D5
R471	D6	D4
R480	D6	D5
R481	D4	D5
R482	E2	E4
R483	E2	E4
R484	E3	E5
R520	C1	E2
R530	E1	F2
R541	D1	F3
R542	E1	F3
R543	D1	E3
R551	E2	F3
R553	D3	E3
R563	D2	F4
R572	D2	F4
R580	E3	E5
R581	G5	E5
R582	G5	E5
R630 ●	D1	G2
R631	C1	G3
R632	C1	G3
R682 ●	D3	F5
R683	C3	G5
R684	C2	G5
R750A ●	A2	H4
R750B ●	A1	H4
R750C ●	D2	H3
R750D ●	D2	H3
R750E ●	D2	H3
R750F ●	D2	H3
R750G ●	A2	H4
R770A	B2	H4
R770B	B2	H4
R770C	B3	H4
R770D	B2	H4
R770E	C2	H4
R770F	C2	H4
R770G	C2	H4
R850	C2	H3
R870	C2	H4
R871	C2	J4
R880 ●	A1	H4
R881 ●	A2	H4
R882 ●	A2	H4
R960	E4	J3
R961	E4	J3
R970	A1	K4
R972	B1	J4
R980	A1	J5
R981	A1	J5
R982	A1	J5
R983	A1	K5
R1051	B1	K3
R1070	A1	K4
R1071	A1	K4
TP160	A2	B4
TP330	A3	D3
TP970	E4	J4
U220A	F6	B2
U220B	F4	B2
U220C	F6	B2
U220D	F4	B2
U280A	B4	C5
U280B	B5	C5
U320B	F1	C2
U440	G3	D3
U460	G5	E4
U630A	C1	F3
U630B	D1	F3
U630C	C1	F3
U650A	E2	F3
U650B	D2	F3
U651A	D2	G3
U651B	D2	G3
U651C	B1	G3
U651D	B2	G3
U670A	C3	F4
U670B	D2	F4
U670C	C2	F4
U671A	C2	G4
U671B	C3	G4
U671C	C1	G4
U671D	C1	G4
U750A	D2	G3
U750B	D2	G3
U770A	C2	G4
U770B	C2	G4
U870	B1	H5
U871A	A2	H5
U871B	A1	H5
U871C	A1	H5
U871	F1	H5
U950A	E4	J3
U950B	E4	J3
U960B	E4	J4
U960C	B1	J4
U960D	B1	J4
W630 ●	D1	G2
W651	D1	F3
W671	D2	F4
W682 ●	D3	F5

Partial A5 also shown on diagram 7.

***See Parts List for serial number ranges.**

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VOLTAGE CONDITIONS

Use a digital voltmeter with a 10 MΩ input impedance such as the TEKTRONIX DM 501A Digital Multimeter installed in a TM 500- or TM 5000-series power module, or a TEKTRONIX 7D13A Digital Multimeter in a readout-equipped Tektronix 7000-series oscilloscope mainframe. Connect the voltmeter ground lead to A5TPGND.

Setup the 7D20 as follows:

Turn off power to oscilloscope mainframe. Remove the A5 CCD Board and place it on the 067-1050-00 extender board. Refer to the A5 CCD Board removal procedure in the Maintenance section of this manual. Use the long coaxial cables furnished with the 067-1050-00 extender set to extend cables from connectors J3 and J4. Turn on oscilloscope mainframe power when A5 has been extended.

Set the CH 1 and CH 2 POSITION controls to midrange.

To horizontally center the display, rotate the HORIZ POSITION control fully clockwise into the switch detent.

Initialize the 7D20 control settings as follows:

a. Press MENU (pushbutton will light).

b. If MASTER MENU is not displayed, press MEMORY DISPLAY pushbutton number 6.

c. From displayed MASTER MENU list select UTILITIES by pressing MEMORY DISPLAY pushbutton number 4.

d. From displayed UTILITIES List select INIT FRONT PANEL by pressing MEMORY DISPLAY pushbutton number 5.

e. To return to MASTER MENU, press MEMORY DISPLAY pushbutton number 6. To turn off MASTER MENU display, press MENU.

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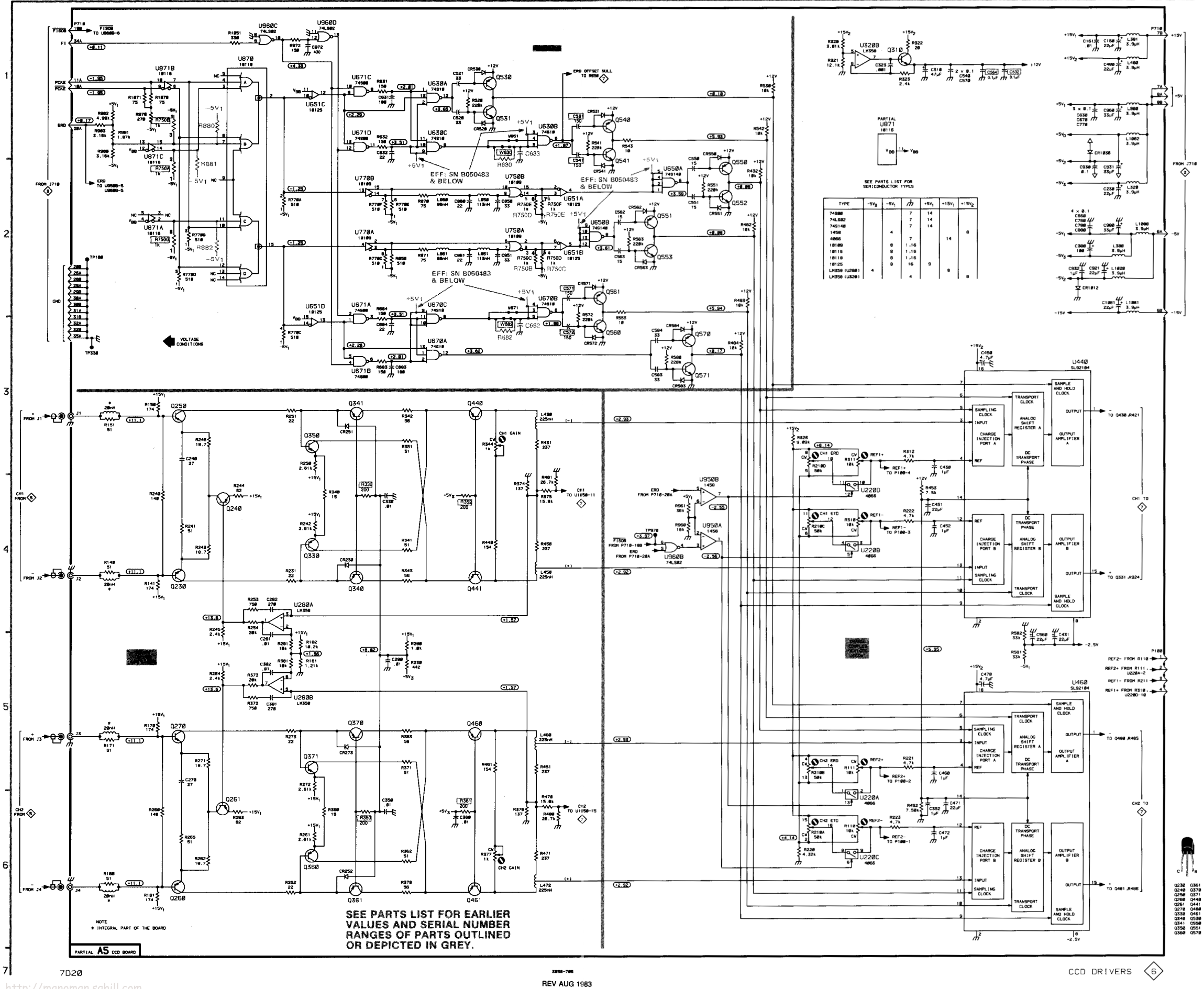

TYPE	-5V$_2$	-5V$_1$		+5V$_1$	+15V$_1$	+15V$_2$
74S08			7	14		
74LS02			7	14		
74S140			7	14		
1458		4				8
4066			7		14	
10109		8	1,16			
10116		8	1,16			
10118		8	1,16			
10125		8	16	9	8	
LH358 (U280)	4		4			8
LH358 (U320)						

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CCD OUTPUT DIAGRAM 7

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
R202	B1	B1	R233	B5	B3

Partial A2 also shown on diagrams 2, 5, 8 and 9.

ASSEMBLY A5

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C421 *†	A2	D2	Q832	D3	H2	R743	B4	H3
C486 *†	A4	E5	Q833	D3	H2	R820	E3	J2
C720	C2	H2	Q950	E4	J3	R821	E3	J2
C740	C4	H2	Q951	E4	K3	R822	E3	J2
C922	F4	K2				R831	E3	J2
C923	F3	J2	R324	A2	D2	R832	E3	J2
C950	E4	J3	R325	B2	D2	R835	D3	J2
C1020	F3	K2	R410	A2	D1	R840	D3	H3
C1021	F4	K2	R411	B2	E1	R841	D3	H3
C1040	E4	K3	R420	A2	D2	R842	D3	H3
CR830	D5	H2	R421	A2	D2	R843	D3	H3
CR831	D5	H3	R422	A1	D2	R844	D3	H3
CR834	D1	J2	R423	B1	D2	R845	D3	J2
CR846	D1	J3	R424	B2	D2	R846	D3	J3
CR910	E3	J1	R425	D4	E2	R920	E4	J1
J1051	F4	L1	R426	D4	E2	R921	E3	J1
			R430	D4	E2	R922	E1	J1
L910	F3	K1	R485	A4	E5	R923	D5	J2
P420 *	A2	D2	R486	A4	E5	R931	F4	J3
P480 *	A4	D5	R487	B4	E5	R940	F4	J3
P710	A1	G1	R510	A4	E1	R950	F4	J3
P710	B1	G1	R511	B4	F1	R962	A3	J3
P710	B5	G1	R522	D2	F2	R963	A1	K3
P710	F1	G1	R523	B4	F2	R1011	F3	K1
P710	F2	G1	R524	B4	F2	R1020	F3	K1
P710	F3	G1	R610	D5	F1	R1030	E4	K2
P710	F4	G1	R611	D5	F1	R1031	E4	K3
Q331	A3	D2	R612	C2	G1	R1040	E4	K3
Q430	A1	D2	R613	C2	G1	R1041	E4	K3
Q480	A3	D5	R614	C2	G1	R1052	F2	K3
Q481	A5	D5	R615	C2	G2	R1053	F2	K3
Q510	D4	E2	R620	C5	F2	R1080	B4	K4
Q511	D2	E2	R621	C5	F2	R1081	B2	K5
Q610	C3	F1	R622	C4	G2			
Q611	C1	F2	R623	C4	G2	RT830	F3	J2
Q620	C4	F2	R625	C4	G2			
Q621	C5	F2	R626	C4	G2	TP331	B3	D2
Q710A	C2	G1	R650	E3	F3	TP430	B1	D2
Q710B	C2	G1	R680	A4	F5	TP481	B5	E5
Q720A	C4	G2	R681	A4	F5	TP680	B3	F5
Q720B	C4	G2	R710	C2	H1	TP1020	A5	L1
Q810	D3	H1	R711	C2	H1	TP1050	F4	L4
Q811	D1	H1	R712	D1	H1			
Q812	D4	H1	R713	C1	H1	U420A	D4	E2
Q813	D2	H1	R720	C4	H2	U420B	D5	E2
Q814	E1	J1	R721	C4	H2	U730A	B2	G2
Q815	E3	J1	R722	C1	H2	U730B	B2	G2
Q820	D4	H2	R723	D1	H2	U740A	B4	G3
Q821	D2	H2	R730	B2	H2	U740B	B4	G3
Q822	D5	H2	R731	B2	H2	U850A	D1	J3
Q823	D3	H2	R732	B2	H2	U930	F3	K2
Q824A	E1	J1	R733	B2	H2	U960A	D3	J4
Q824B	E3	J1	R740	B4	H3	U1050	F2	K4
Q830	D3	H2	R741	B4	H3			
Q831	D3	H2	R742	B4	H3	VR1010	E4	K1

Partial A5 also shown on diagram 6.

***See Parts List for serial number ranges.**

† Located on back of board.

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VOLTAGE CONDITIONS

Use a digital voltmeter with a 10 MΩ input impedance such as the TEKTRONIX DM 501A Digital Multimeter installed in a TM 500- or TM 5000-series power module, or a TEKTRONIX 7D13A Digital Multimeter in a readout-equipped Tektronix 7000-series oscilloscope mainframe. Connect the voltmeter ground lead to A5TPGND.

Setup the 7D20 as follows:

Turn off power to oscilloscope mainframe. Remove the A5 CCD Board and place it on the 067-1050-00 extender board. Refer to the A5 CCD Board removal procedure in the Maintenance section of this manual. Use the long coaxial cables furnished with the 067-1050-00 extender set to extend cables from connectors J3 and J4. Turn on oscilloscope mainframe power when A5 has been extended.

Set the CH 1 and CH 2 POSITION controls to midrange.

To horizontally center the display, rotate the HORIZ POSITION control fully clockwise into the switch detent.

Initialize the 7D20 control settings as follows:

a. Press MENU (pushbutton will light).

b. If MASTER MENU is not displayed, press MEMORY DISPLAY pushbutton number 6.

c. From displayed MASTER MENU list select UTILITIES by pressing MEMORY DISPLAY pushbutton number 4.

d. From displayed UTILITIES List select INIT FRONT PANEL by pressing MEMORY DISPLAY pushbutton number 5.

e. To return to MASTER MENU, press MEMORY DISPLAY pushbutton number 6. To turn off MASTER MENU display, press MENU.

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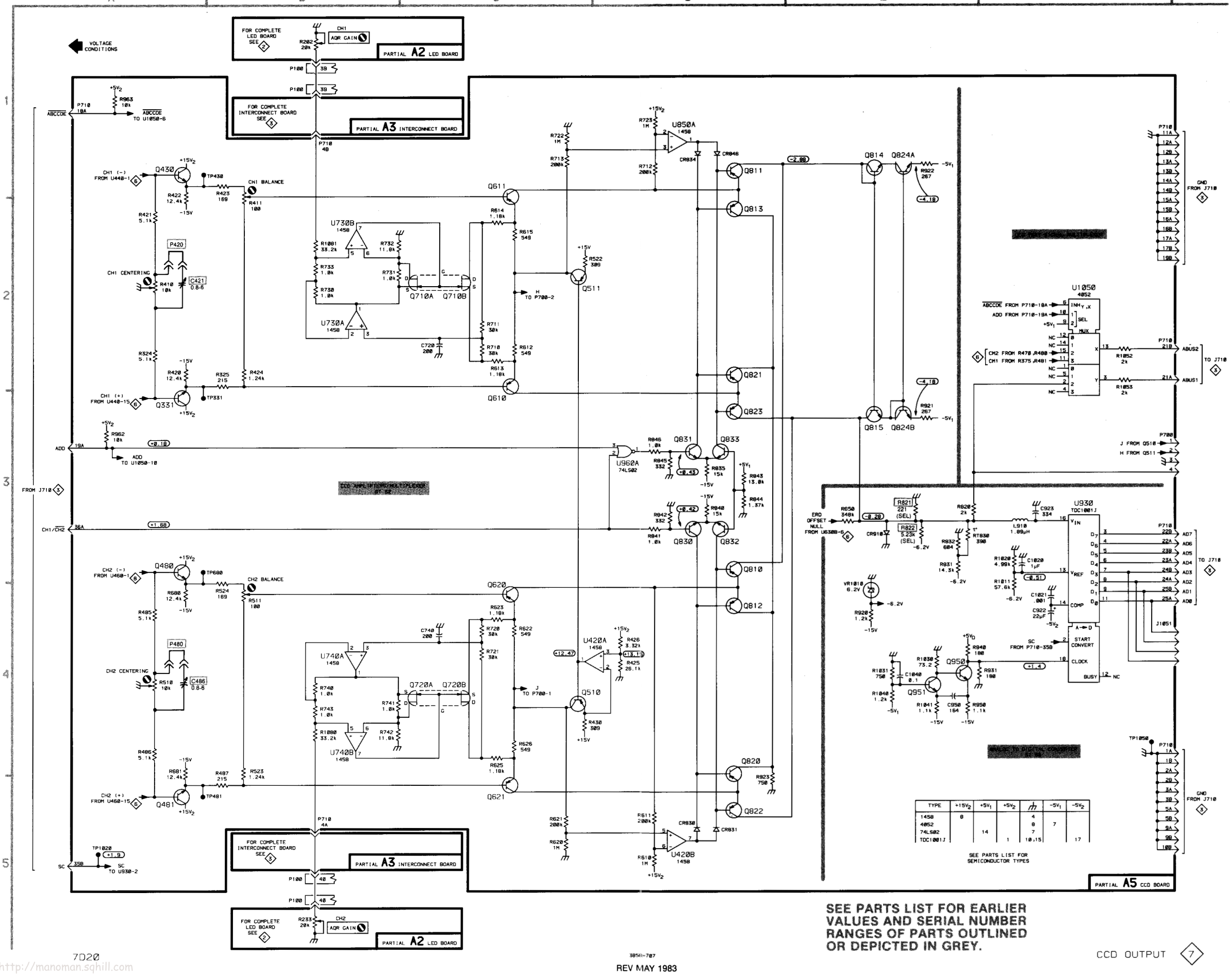

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.

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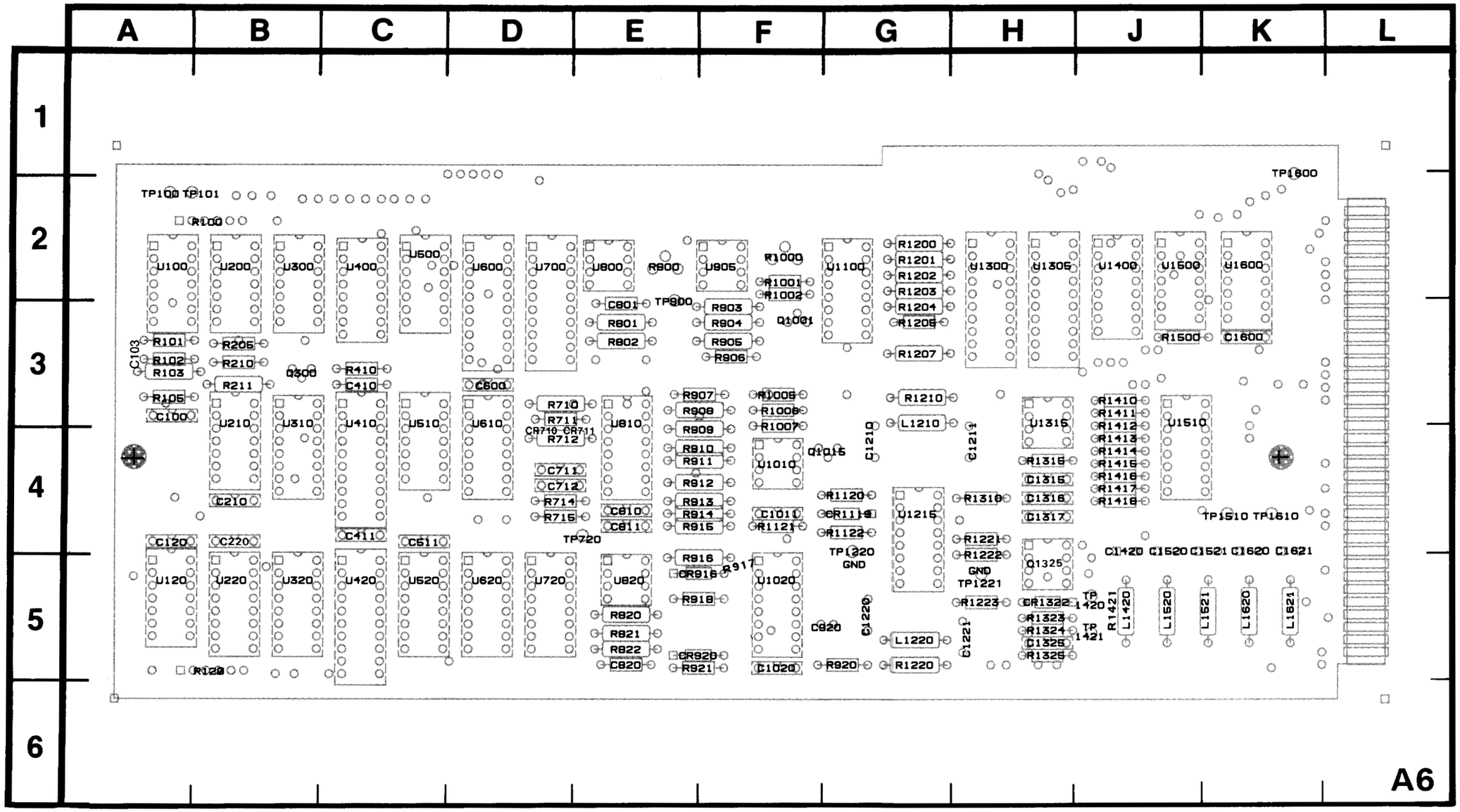
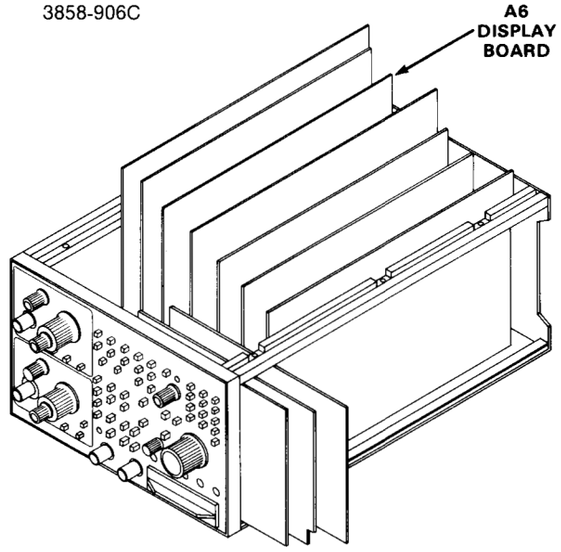


Figure 7-8. A6—Display circuit board assembly.

3858-906C



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DISPLAY - DIGITAL DIAGRAM 8

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
R640	A2	F4

Partial A2 also shown on diagrams 2, 5, 7 and 9.

ASSEMBLY A6

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	C1	A3	R120D	B3	B5	U300B	F1	B2
C103	G1	A3	R205	E4	B3	U300C	A2	B2
C120	A3	A4	R210	F1	B3	U300D	F2	B2
C210	A3	B4	R211	C1	B3	U310	C2	B3
C220	A3	B4	R410	D1	C3	U320	E2	B5
C410	C2	C3	R714	C1	D4	U400A	D1	C2
C411	A3	C4	R1500	F2	J3	U400B	C2	C2
C511	A3	C4				U410	D1	C3
C600	A3	D3	TP100	G1	A2	U420	D1	C5
C1600	A3	K3	TP101	B2	B2	U500A	C4	C2
C1621	A3	K4	TP1510	A3	K4	U500B	C4	C2
CR710*	C2	D4	TP1600	G4	K2	U510	F1	C3
CR711*	C1	E4	TP1610	A4	K4	U520	E3	C5
L1621	A3	K5				U600	B5	D2
Q300	C2	B3	U100A	F1	A2	U620	E3	D5
R100A	A3	B2	U100C	C4	A2	U1300	C5	H2
R100B	B4	B2	U100D	F1	A2	U1305	D5	H2
R100D	A2	B2	U120A	D2	A5	U1400	A4	J2
R100E	C4	B2	U120B	D3	A5	U1500A	F2	J2
R101	F1	A3	U200A	A2	B2	U1600A	A2	K2
R102	D4	A3	U200B	F1	B2	U1600B	A2	K2
R103	C2	A3	U210	B4	B3	U1600C	A2	K2
R105	C2	A3	U220A	D3	B5	U1600D	A3	K2
R120B	D3	B5	U220B	D4	B5	U1600E	D4	K2
R120C	D3	B5	U300A	F1	B2	U1600F	E2	K2

Partial A6 also shown on diagram 9.

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
Q110	G1	C3	R100	G1	B2	R120	G1	C3
			R114	G1	C3			

Partial A10 also shown on diagrams 9 and 13.

***See Parts List for serial number ranges.**

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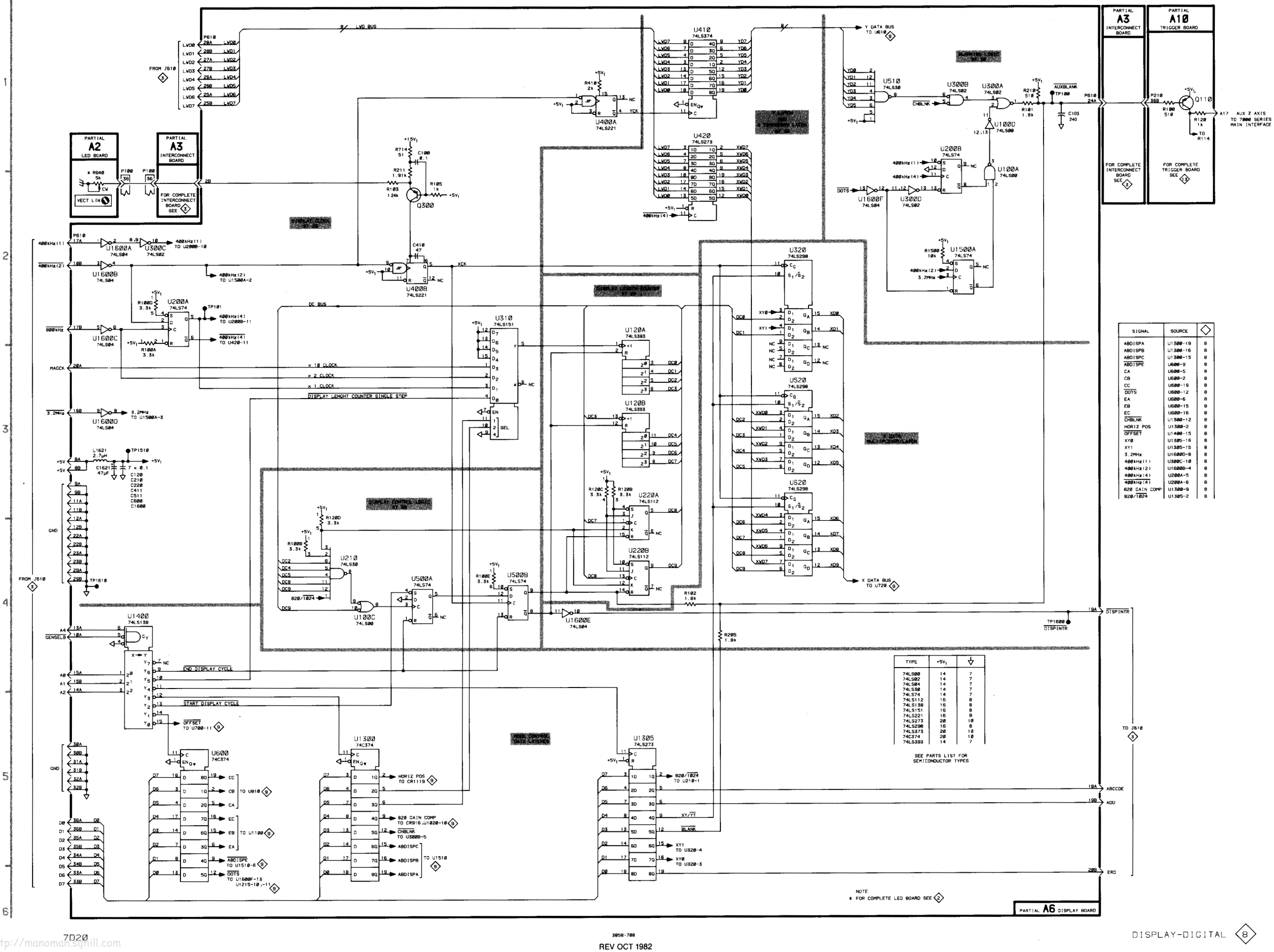

SIGNAL	SOURCE	◇
ABDISPA	U1300-19	8
ABDISPB	U1300-16	8
ABDISPC	U1300-15	8
ABDISPE	U600-9	8
CA	U600-5	8
CB	U600-2	8
CC	U600-19	8
DOTS	U600-12	8
EA	U600-6	8
EB	U600-15	8
EC	U600-16	8
CHBLNK	U1300-12	8
HORIZ POS	U1300-2	8
OFFSET	U1400-15	8
XY0	U1305-16	8
XY1	U1305-15	8
3.2MHz	U1600-8	8
400kHz(1)	U300C-10	8
400kHz(2)	U1600B-4	8
400kHz(4)	U200A-5	8
400kHz(4)	U200A-6	8
820 GAIN COMP	U1300-9	9
820/1024	U1305-2	8

TYPE	+5V$_1$	⏚
74LS00	14	7
74LS02	14	7
74LS04	14	7
74LS30	14	7
74LS74	14	7
74LS112	16	8
74LS138	16	8
74LS151	16	8
74LS221	16	8
74LS273	20	10
74LS298	16	8
74LS373	20	10
74C374	20	10
74LS393	14	7

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

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DISPLAY - ANALOG DIAGRAM 9

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
R440	A2	E4	R630	A4	E4	R840	A5	G4
R540	A3	E4	R740	A4	F4			

Partial A2 also shown on diagrams 2, 5, 7 and 8.

ASSEMBLY A4

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C241	H2	B4	R230	H2	B4	R251	G2	B5
C250	G2	B5	R240	H2	B4	R255	H2	B5
			R241	G2	B4			
P830	G2	M3	R242	H2	B4	U240A	G2	B4
			R250	G2	B5	U240B	G2	B4

Partial A4 also shown on diagrams 4 and 5.

ASSEMBLY A6

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C711	F2	D4	R801	C2	E3	R1220	E2	G5
C712	F1	D4	R802	D2	E3	R1221	F3	H4
C801	C2	E3	R820	B4	E5	R1222	E2	H4
C810	F1	E4	R821	E4	E5	R1223	B4	H5
C811	F1	E4	R822	E4	E5	R1310	F2	H4
C820	E4	E5	R900	C2	E2	R1315	E3	H4
C920	B4	G5	R903	C1	F3	R1323	B4	H5
C1011	B2	F4	R904	C2	F3	R1324	B4	H5
C1020	B4	F5	R905	C2	F3	R1325	D5	H5
C1210	E2	G4	R906	D2	F3	R1410	F4	J3
C1211	E2	H4	R907	E2	E3	R1411	F4	J3
C1220	E3	G5	R908	E2	E3	R1412	F4	J3
C1221	E3	H5	R909	E3	E4	R1413	F4	J4
C1315	E3	H4	R910	E3	E4	R1414	E4	J4
C1316	F1	H4	R911	B1	E4	R1415	F2	J4
C1317	F2	H4	R912	B1	E4	R1416	F4	J4
C1325	D5	H5	R913	B1	E4	R1417	F4	J4
C1420	F2	J4	R914	B1	E4	R1418	F3	J4
C1520	F1	J4	R915	B1	E4	R1421*	F3	J5
C1521	F1	K4	R916	B4	E5	TP720	E5	E4
C1620	F1	K4	R917*	B4	F5	TP900	D2	E2
			R918	B4	E5	TP1220	F1	G4
CR916	B4	E5	R920	B4	G5	TP1221	F1	H5
CR920	B4	E5	R921	B4	E5	TP1420	F2	J5
CR1119	B4	G4	R1000	D1	F2	TP1421	F3	J5
CR1322	B4	H5	R1001	E2	F2	U610	C1	D3
			R1002	D2	F2	U700	C2	D2
L1210	E2	G3	R1005	E2	F3	U720	C3	D5
L1220	E2	G5	R1006	E1	F3	U800	D2	E2
L1420	F2	J5	R1007	E1	F3	U810	B1	E3
L1520	F1	J5	R1120	E2	G4	U820	E5	E5
L1521	F1	K5	R1121	B2	F4	U905	C2	F2
L1620	F1	K5	R1122	B4	G4	U1010	E2	F4
			R1200	D2	G2	U1020	B4	F5
Q1001	E2	F3	R1201	D2	G2	U1100	D1	G2
Q1015	E1	G4	R1202	D2	G2	U1215	F2	G4
			R1203	D2	G2	U1315	F2	H3
R710	C2	D3	R1204	D2	G3	U1325A	F3	H5
R711	B2	D3	R1205	D2	G3	U1325B	B4	H5
R712	B2	D4	R1207	D2	G3	U1510	F4	J3
R715	C3	D4	R1210	E2	G3			

Partial A6 also shown on diagram 8.

***See Parts List for serial number ranges.**

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C130	H3	C4	R134	H3	B4	U230A	G3	C4
C231	G3	D4	R135	H3	B5	U230B	G3	C4
			R220	H3	C4			
R131	H3	C4	R230	G3	D4	W231*	G3	D5
R132	G3	C4	R231*	G3	D5			

Partial A10 also shown on diagrams 8 and 13.

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VOLTAGE CONDITIONS

Use a digital voltmeter with a 10 MΩ input impedance such as the TEKTRONIX DM 501A Digital Multimeter installed in a TM 500-or TM 5000-series power module, or a TEKTRONIX 7D13A Digital Multimeter in a readout-equipped Tektronix 7000-series oscilloscope mainframe. Connect the voltmeter ground lead to A6TP1220.

Setup the 7D20 as follows:

Turn off power to oscilloscope mainframe. Remove A6 Display Board and place it on the 067-1050-00 extender board. Refer to the A6 Display Board removal procedure in the Maintenance section of this manual. Turn on oscilloscope mainframe power when A6 has been extended.

To horizontally center the display, rotate the HORIZ POSITION control fully clockwise into the switch detent.

Initialize the 7D20 control settings as follows:

a. Press MENU (pushbutton will light).

b. If MASTER MENU is not displayed, press MEMORY DISPLAY pushbutton number 6.

c. From displayed MASTER MENU list select UTILITIES by pressing MEMORY DISPLAY pushbutton number 4.

d. From displayed UTILITIES List select INIT FRONT PANEL by pressing MEMORY DISPLAY pushbutton number 5.

e. To return to MASTER MENU, press MEMORY DISPLAY pushbutton number 6. To turn off MASTER MENU display, press MENU.

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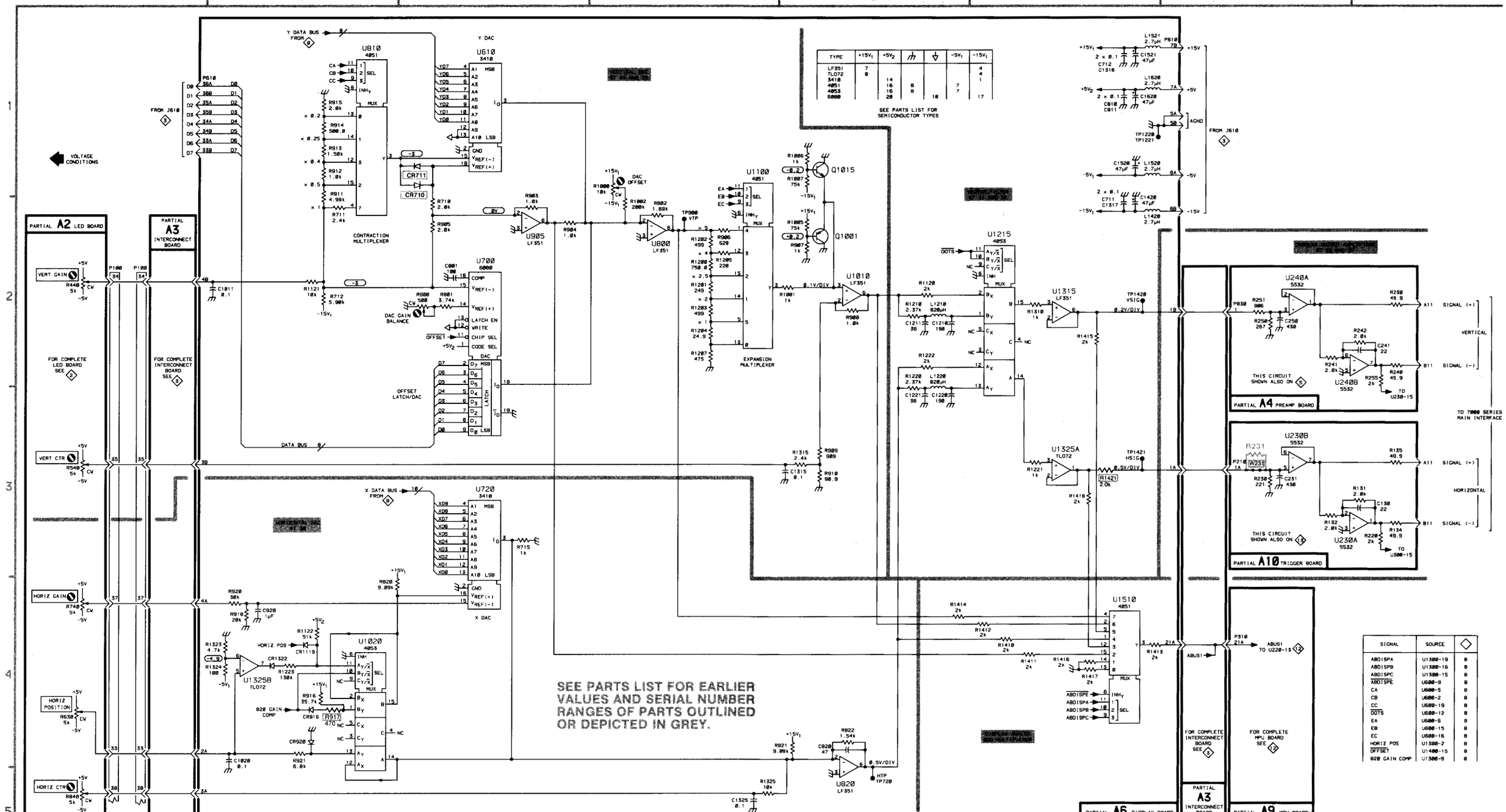

SIGNAL	SOURCE	◇
ABDISPA	U1300-19	9
ABDISPB	U1300-15	9
ABDISPC	U1300-15	9
ABDISPE	U600-9	9
CA	U600-5	9
CB	U600-2	9
CC	U600-19	9
DOTS	U600-12	9
EA	U600-6	9
EB	U600-15	9
EC	U600-16	9
HORIZ POS	U1300-2	9
OFFSET	U1400-15	9
820 GAIN COMP	U1300-9	9

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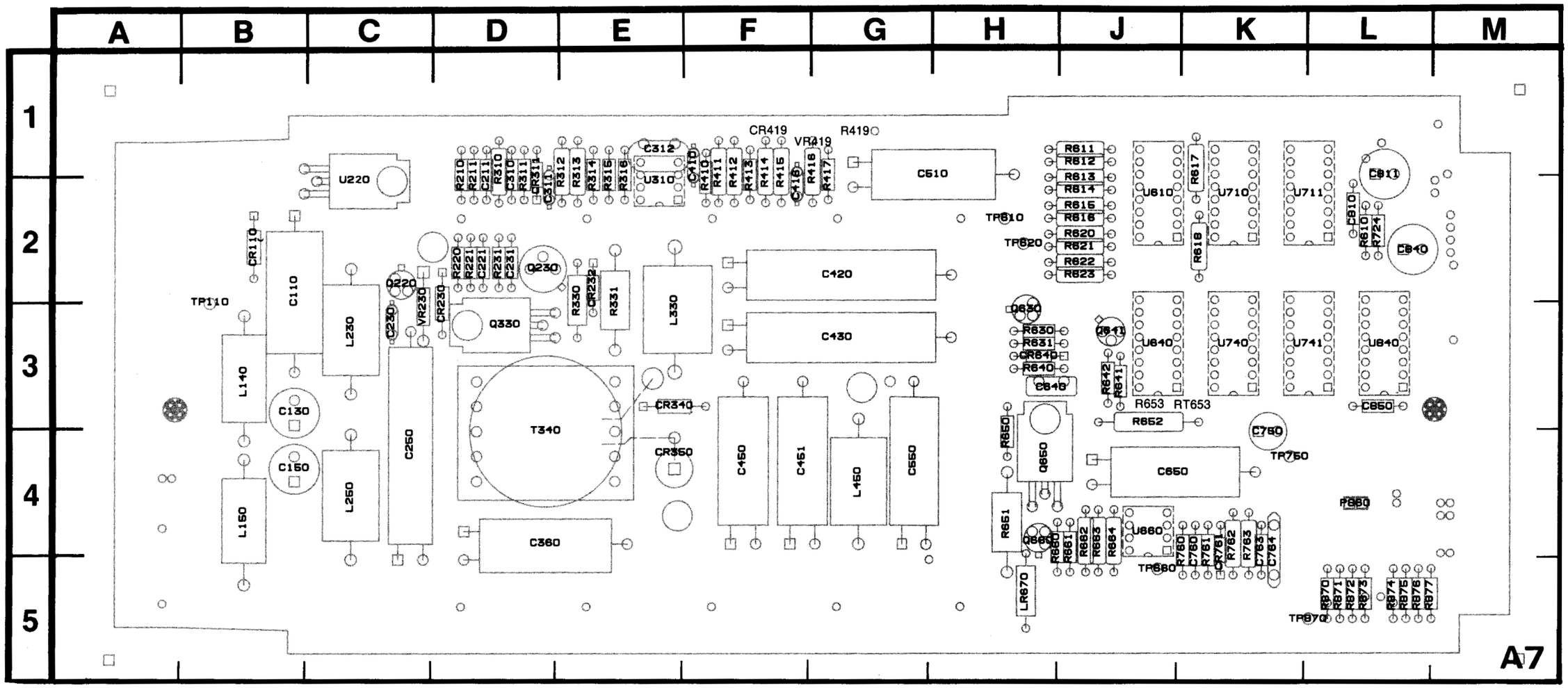

Figure 7-9. A7—Power Supply circuit board assembly.

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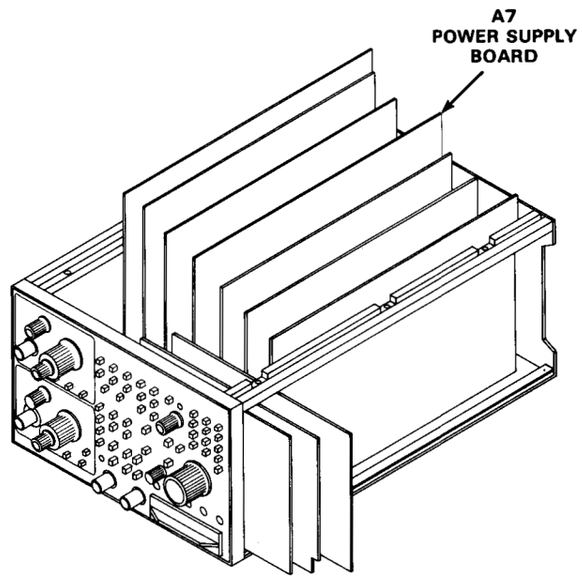

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POWER SUPPLY BOARD DIAGRAM 10

ASSEMBLY A7

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C110	B1	B2
C130	A4	B3
C150	B3	B4
C211	C5	D1
C221	B5	D2
C230	B3	C3
C231	C5	D2
C250	B3	C4
C310	C5	D1
C311	D5	D2
C312	D5	E1
C360	B3	D4
C410	E5	F1
C416	E5	F2
C420	C3	G2
C430	C3	G3
C450	B4	F4
C451	C4	F4
C510	C3	H1
C550	C4	G4
C640	F4	H3
C650	E3	J4
C750	D3	K3
C760	D3	K4
C763	C3	K4
C764	B4	K4
C810	E3	L2
C811	D2	L1
C840	D3	L2
C850	E3	L3
CR110	B1	B2
CR230	B4	D2
CR232	B5	E2
CR311	D5	D1
CR340	C4	E3
CR350	C3	E4
CR419	E5	F1
CR640	F4	H3
CR761	D4	K4
L140	A4	B3
L150	A3	B4
L230	B4	C3
L250	B3	C4
L330	C3	E3
L450	C4	G4
LR670	A4	H5
P860	F3	L4
Q220	B6	C2
Q230	B5	D2
Q330	B5	D3
Q630	F4	H3
Q641	E2	J3
Q650	D3	H4
Q660	D3	H4
R210	B5	D1
R211	C5	D1
R220	B5	D2
R221	B5	D2
R231	C5	D2
R310	D5	D1
R311	C5	D1
R312	C5	E1
R313	C4	E1
R314	D5	E1
R315	D5	E1
R316	D5	E1
R330	B5	E2
R331	B5	E2
R410	E5	F1
R411	E5	F1
R412	E5	F1
R413	E5	F1
R414	E5	F1
R415	F5	F1
R416	E5	G1
R417	B6	G1
R419	E5	G1
R610	D1	L2
R611	C1	J1
R612	C2	J1
R613	C2	J2
R614	C2	J2
R615	C1	J2
R616	C1	J2
R617	B1	K1
R618	B1	K2
R620	C1	J2
R621	C1	J2
R622	C1	J2
R623	C1	J2
R630	F4	H3
R631	F4	H3
R640	F4	H3
R641	E1	J3
R642	E2	J3
R650	E4	H3
R651	E4	H4
R652	E1	J3
R653	E1	J3
R660	D4	J4
R661	D3	J4
R662	D4	J4
R663	D4	J4
R664	D4	J4
R724	D1	L2
R760	D4	K4
R761	D4	K4
R762	C4	K4
R763	C3	K4
R870	F2	L5
R871	F2	L5
R872	F3	L5
R873	F3	L5
R874	F2	L5
R875	F2	L5
R876	F2	L5
R877	F2	L5
RT653	E1	J3
T340	C3	D4
TP610	E3	H2
TP620	C4	H2
TP660	E3	J5
TP750	F4	K4
TP870	F4	L5
U220	B1	C2
U310A	E5	E2
U310B	D5	E2
U610	C1	J2
U640	F2	J3
U660A	D4	J4
U660B	D4	J4
U710	B2	K2
U711	D2	K2
U740A	E2	K3
U740B	E2	K3
U741	F1	K3
U840	B1	L3
VR230	B3	C3
VR419	E5	F1

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VOLTAGE CONDITIONS

Use a digital voltmeter with a 10 MΩ input impedance such as the TEKTRONIX DM 501A Digitial Multimeter installed in a TM 500- or TM 5000-series power module, or a TEKTRONIX 7D13A Digital Multimeter in a readout-equipped Tektronix 7000-series oscilloscope mainframe. Connect the voltmeter ground lead to A7TP620.

Setup the 7D20 as follows:

Turn off power to the oscilloscope mainframe. Remove A7 Power Supply Board and place it on the 067-1050-00 extender board. Refer to the A7 Power Supply Board removal procedure in the Maintenance section of this manual. Turn on oscilloscope mainframe power when A7 has been extended.

Set the CH 1 and CH 2 POSITION controls to midrange.

To horizontally center the display, rotate the HORIZ POSITION control fully clockwise into the switch detent.

Initialize the 7D20 control settings as follows:

a. Press MENU (pushbutton will light).

b. If MASTER MENU is not displayed, press MEMORY DISPLAY pushbutton number 6.

c. From displayed MASTER MENU list select UTILITIES by pressing MEMORY DISPLAY pushbutton number 4.

d. From displayed UTILITIES list select INIT FRONT PANEL by pressing MEMORY DISPLAY pushbutton number 5.

e. To return to MASTER MENU, press MEMORY DISPLAY pushbutton number 6. To turn off MASTER MENU display, press MENU.

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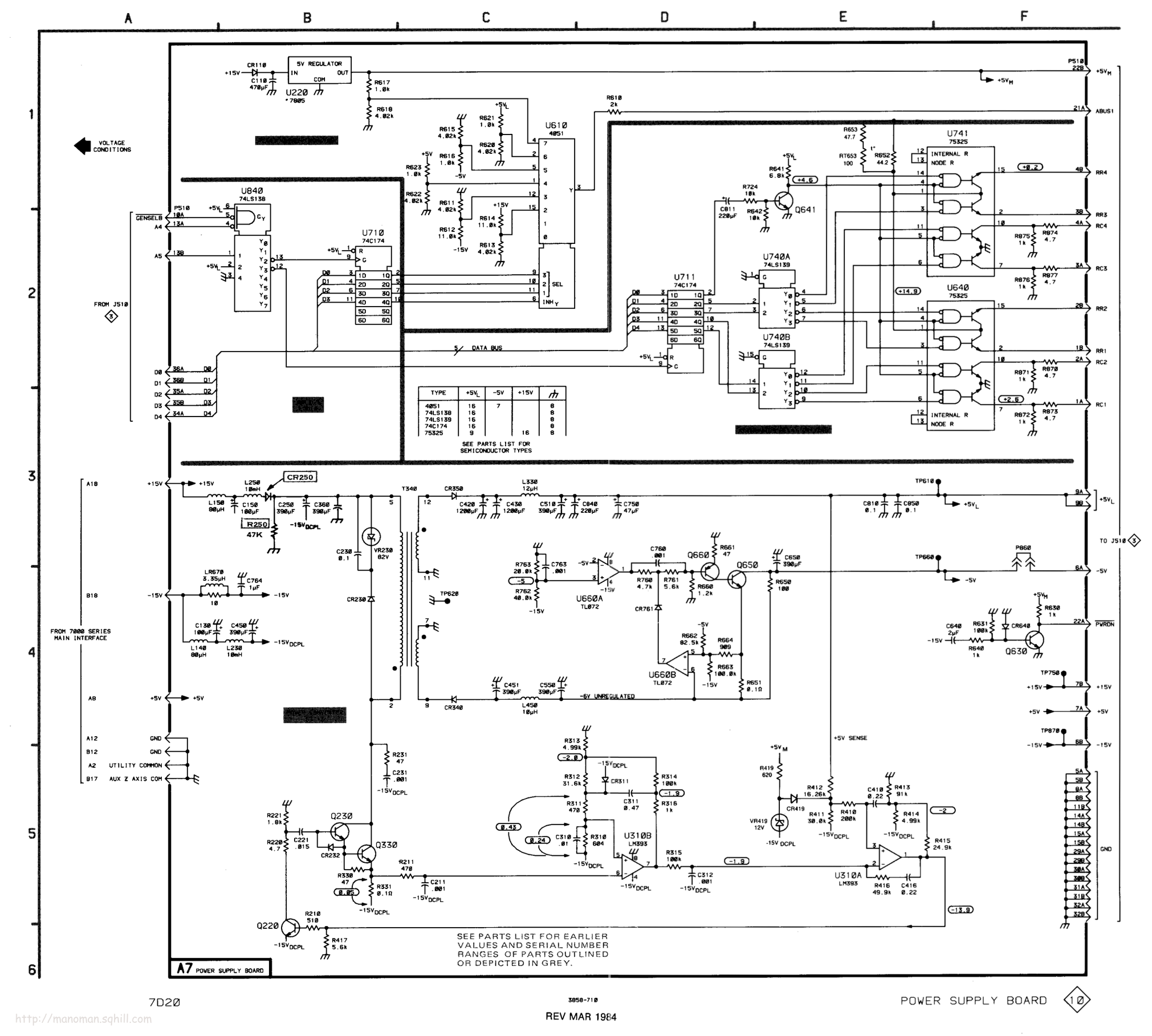

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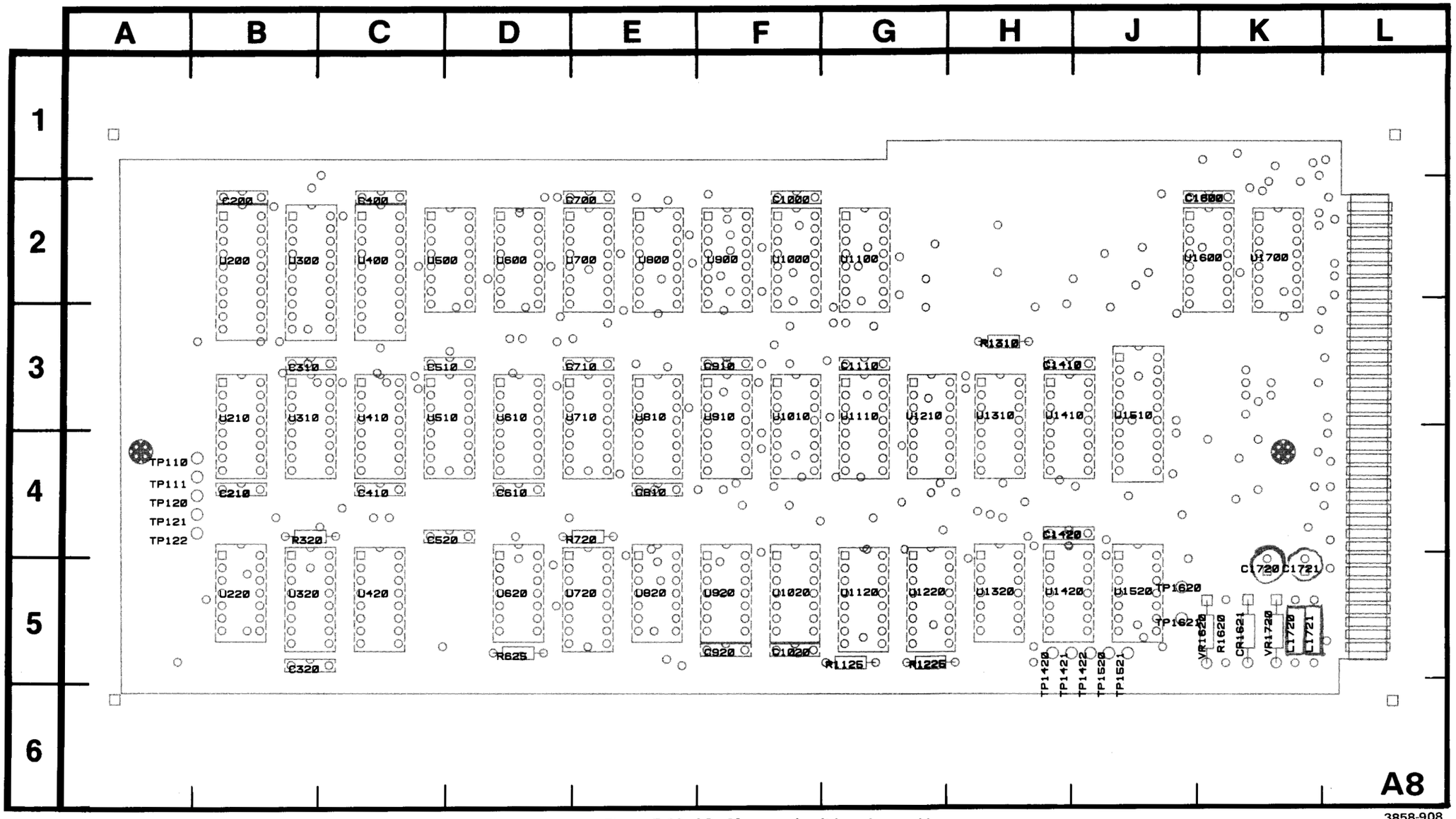

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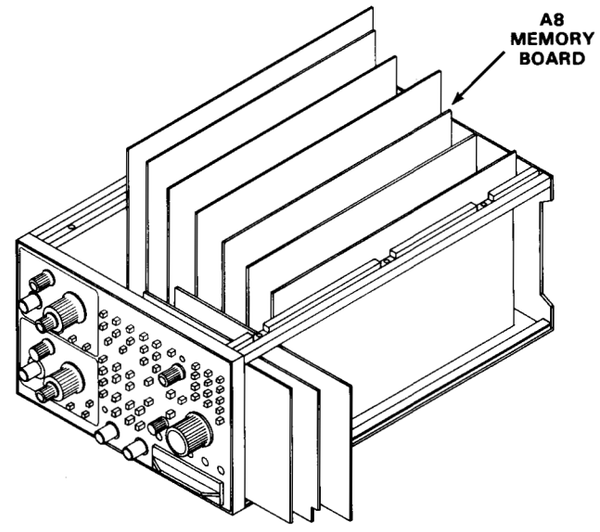
Figure 7-10. A8—Memory circuit board assembly.



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MEMORY BOARD DIAGRAM 11

ASSEMBLY A8

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C200	A5	B2
C210	A3	B4
C310	A2	B3
C320	A5	B5
C400	A5	C2
C410	A3	C4
C510	A2	C3
C520	A5	C4
C610	A3	D4
C700	A5	E2
C710	A2	E3
C810	A3	E4
C910	A2	F3
C920	A5	F5
C1000	A5	F2
C1020	A5	F5
C1110	A5	G3
C1410	A5	H3
C1420	A5	H4
C1600	A5	K2
C1720	A2	K5
C1721	A5	K5
CR1621	A2	K5
L1720	A2	K5
L1721	A5	K5
R320	B3	B4
R625	B5	D5
R720	B5	E4
R1125	C4	G5
R1225	B2	G5
R1310	E3	H3
R1620	A2	K5
TP110	D1	A4
TP111	C3	A4
TP120	C4	A4
TP121	C4	A4
TP122	C3	A4
TP1420	A3	H4
TP1421	A3	H4
TP1422	A3	J5
TP1520	B4	J5
TP1620	A5	J5
TP1621	A3	J5
U200	H5	B2
U210	G5	B3
U220	B4	B5
U300	H3	B2
U310	G4	B3
U320	B3	B5
U400	H2	C2
U410	G4	C3
U420	B1	C5
U500	D2	C2
U510	G3	C3
U600	D2	D2
U610	G2	D3
U620A	D3	D5
U620B	C3	D5
U620C	H2	D5
U620D	D1	D5
U700	D1	E2
U710	G2	E3
U720A	C1	E5
U800	E5	E2
U810	G1	E3
U820A	D1	E5
U820B	B4	E5
U900	D3	F2
U910	G1	F3
U920A	E5	F5
U920B	C1	F5
U920C	C2	F5
U920D	E3	F5
U1000	D4	F2
U1010	E4	F3
U1020A	C5	F5
U1020B	C5	F5
U1020C	B3	F5
U1100	D4	G2
U1110	E4	G3
U1120	C3	G5
U1210	E3	G3
U1220	B2	G5
U1310	E2	H3
U1320A	A4	H4
U1320B	C2	H4
U1320C	C3	H4
U1320D	A3	H4
U1410	E1	H3
U1420A	B4	H4
U1420B	C1	H4
U1420C	B4	H4
U1420D	A3	H4
U1510	H1	J3
U1520A	B4	J5
U1520B	C1	J5
U1520C	A4	J5
U1520E	A3	J5
U1600	F1	K2
U1700	F2	K2
VR1620	A2	K5
VR1720	A2	K5

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MEMORY CONTROL

WAVEFORM MEMORY SELECT ST.12

DISPLAY ADDRESS GENERATOR ST.15 AND 16

DATA MULTIPLEXER ST.17

MICROPROCESSOR ADDRESS MULTIPLEXER ST.18

DISPLAY/ACQUIRE ADDRESS MULTIPLEXER

ACQUIRE ADDRESS GENERATOR ST.19

BLOCK REGISTER ST.27

MEMORY TIMING AND SYNCHRONIZATION

DISPLAY OUTPUT LATCH ST.23

WAVEFORM DATA LATCH

SELF TEST LATCHES ST.14 AND 17

WAVEFORM MEMORY (16PK) ST.19-26

TYPE	+5V$_L$	⏚	+12V	-5V
4116	9	16	8	1
74LS00	14	7		
74LS02	14	7		
74LS04	14	7		
74LS10	14	7		
74LS32	14	7		
74LS54	14	7		
74LS74	14	7		
74LS85	16	8		
74LS86	14	7		
74LS109	16	8		
74LS138	16	8		
74LS175	16	8		
74LS191	16	8		
74LS257	16	8		
74LS259	16	8		
74LS373	20	10		
74LS374	20	10		
74LS670	16	8		

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

SIGNAL	SOURCE
AACSS	U420-13
AACSSE	U1220-10
ACQ	U320-11
ASA	U420-9
AV	U1020-9
AWCK	P410-18A
A0	A BUS
A1	A BUS
BLOCK	U420-7
CA	U320-15
DISPINTR	P410-19B
D0	D BUS
ENDACQ	P410-30B
GSA	U620B-6
LATCK	U1120-6
MEA	U1000-7
PRWS	U1220-11
RA	U320-14
RAS	U1320D-13
RMA	U420-15
RMD	U420-14
R/W	U220-6
WMEMSEL	P410-21B
WMS	U820A-6
WMS	U820A-5
W/R	P410-19A
1.6MHzM	U1420C-11
400kHz(3)	U320-7
800kHz	P410-17B
800kHzM	U1520A-2

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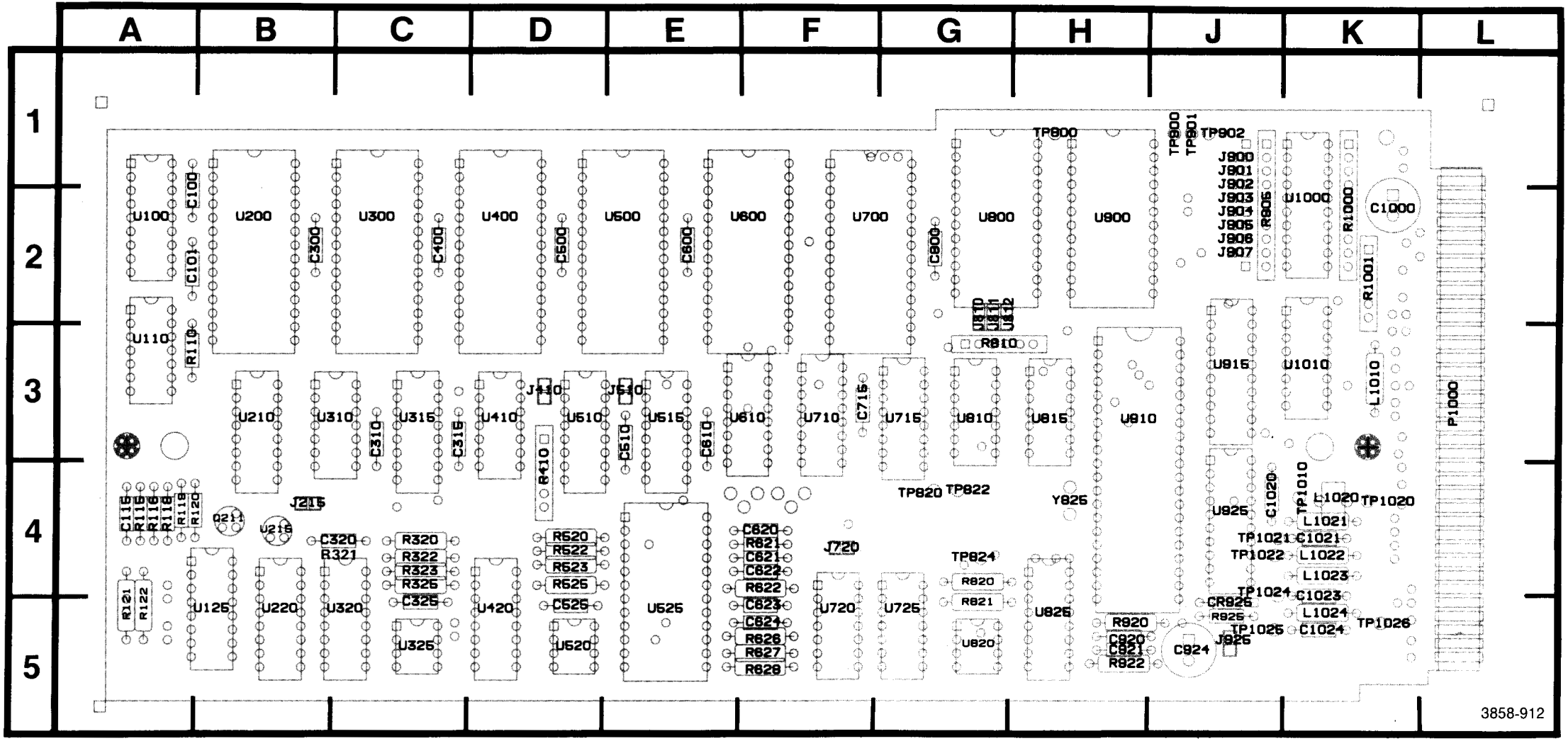

3858-912

Fig. 7-11A. A9—MPU circuit board assembly (SN B061870 & up).

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MPU CONTROL DIAGRAM (SN B061870 & UP) 12

ASSEMBLY A9

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	A5	A2
C101	A5	A2
C300	A5	B2
C310	A5	C3
C315	A5	C3
C320	A5	C4
C325	A6	C4
C400	A5	C2
C500	A5	D2
C510	A5	E3
C525	A5	D4
C600	A5	E2
C610	B5	E3
C621	A5	F4
C622	A5	F4
C623	G4	F5
C624	G3	F5
C715	B5	F3
C800	B5	G2
C920	B3	H5
C921	B3	H5
C924	B4	J5
C1000	A5	K1
C1020	A5	K1
C1021	A5	K4
C1023	A5	K4
C1024	A6	K5
CR925	B4	J5
J215	H5	B4
J410	H4	D3
J510	H3	E3
J720	A2	F4
J810	A4	G2
J811	A4	G2
J812	B4	G2
J900	C2	J1
J901	C1	J1
J902	C1	J1
J903	C1	J2
J904	C2	J2
J905	C1	J2
J906	C1	J2
J907	C2	J2
J925	B4	J5
L1010	A5	K3
L1020	A5	K4
L1021	A5	K4
L1022	A6	K4
L1023	A5	K4
L1024	A5	K5
P310	A1	L3
P310	F3	L3
P310	I1	L3
Q211	G6	B4
R110	G5	A2
R115	G6	A4
R116	G6	A4
R118	G6	A4
R119	G5	A4
R120	H5	A4
R121	G5	A5
R122	G5	A5
R320	F4	C4
R321	G3	C4
R322	F4	C4
R323	E4	C4
R325	E4	C4
R410A	H3	D3
R410B	H3	D3
R410E	B3	D3
R520	E5	D4
R522	F5	D4
R523	F5	D4
R525	E5	D4
R621	G4	F4
R622	G3	F4
R626	G4	F4
R627	G4	F5
R628	G3	F5
R810A	B4	G3
R810B	B4	G3
R810D	A4	G3
R820	A4	G4
R821	A4	G5
R905A	B3	J2
R905B	B2	J2
R905C	B1	J2
R905D	B1	J2
R905E	B1	J2
R905F	B2	J2
R905G	B1	J2
R905H	B1	J2
R905J	B2	J2
R920	B3	H4
R922	B3	H5
R925	B4	J5
R1000A	B2	K2
R1000B	A1	K2
R1000C	A1	K2
R1000D	A1	K2
R1000E	A2	K2
R1000F	A1	K2
R1000G	A1	K2
R1000H	A2	K2
R1000J	A2	K2
R1001A	H5	K2
R1001B	H5	K2
R1001	I1	K2
TP800	A3	H1
TP820	C3	G4
TP822	C2	G4
TP824	C3	G4
TP900	E5	J1
TP901	E5	J1
TP902	B4	J1
TP1010	A5	K4
TP1020	A3	K4
TP1021	A4	J4
TP1022	A6	J4
TP1024	A5	J4
TP1025	A6	J5
TP1026	A5	K5
U100	H1	A2
U110A	G5	A3
U100B	G5	A3
U110C	H5	A3
U125	G4	B4
U200	F1	B2
U210	E3	B3
U215	G5	B4
U220	G3	B4
U300	F1	C2
U310	E4	C3
U315	E4	C3
U320	F4	C3
U325A	F6	C5
U325B	F4	C5
U400	E1	D2
U410	E5	D3
U420	F5	D4
U500	G1	E2
U510	H3	D3
U515	H2	E3
U520	B5	D5
U525	G3	E5
U600	E2	F2
U610	D3	F3
U700	G2	F2
U710	D1	F3
U720A	D3	F4
U720B	D3	F4
U720C	B4	F4
U720D	B4	F4
U725A	D2	G5
U725B	D2	G5
U725C	A2	G5
U725D	A2	G5
U800	F2	G2
U810A	D1	G3
U810B	C2	G3
U810C	A3	G3
U810D	D2	G3
U815A	B3	H3
U815B	A3	H3
U815C	B3	H3
U820	B4	G5
U825A	B3	H5
U825B	B3	H5
U900	E2	H2
U910	C4	H3
U915	H5	J4
U1000	BI	K1
U1010	H1	K3
Y825	B5	H4

Partial A9 also shown on diagrams 5 and 9.

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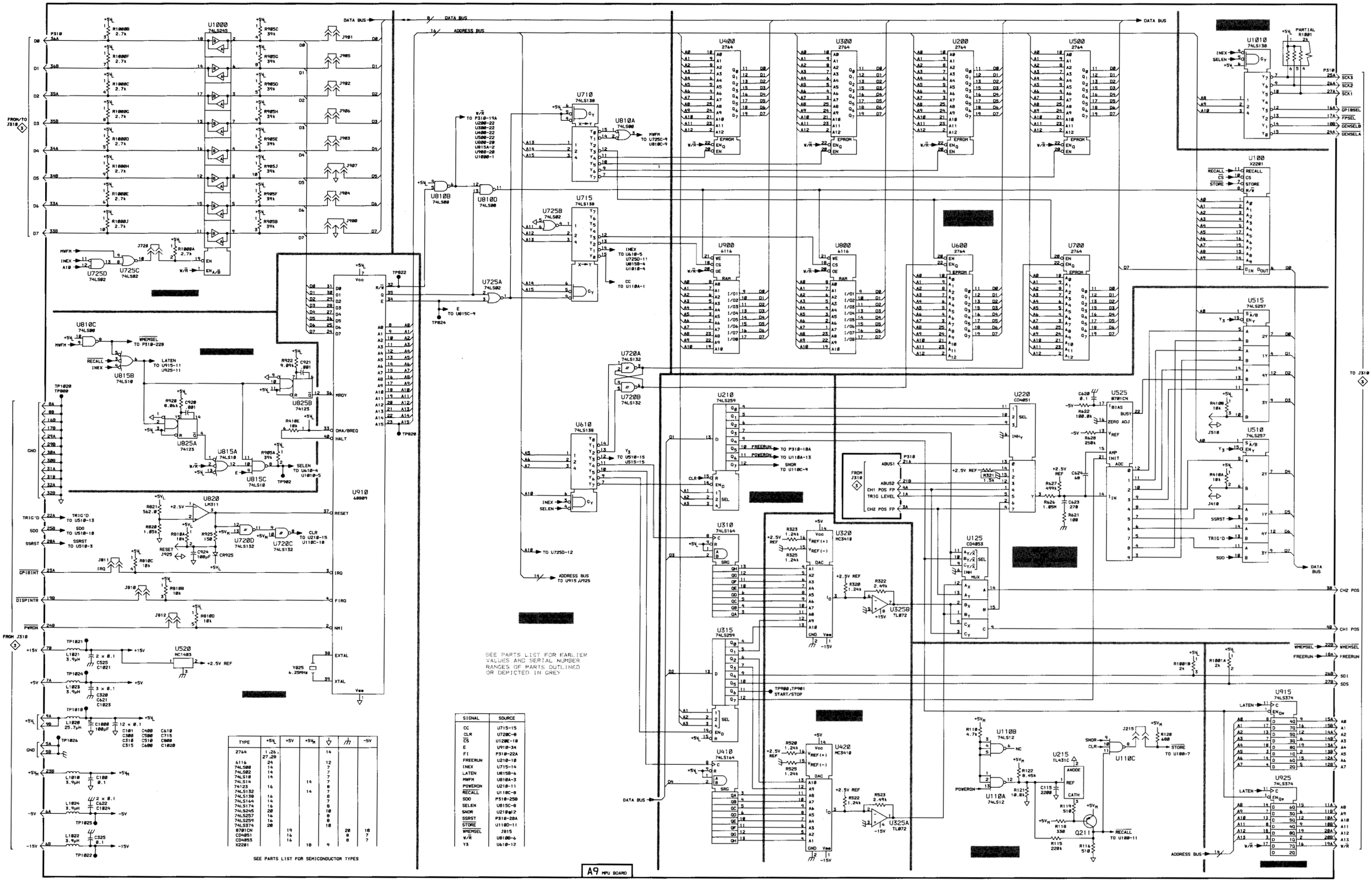

SIGNAL	SOURCE
CC	U715-15
CLR	U720C-8
CS	U129E-18
E	U910-34
F1	P310-22A
FREERUN	U210-10
INEX	U715-14
LATEN	U815B-4
MWFH	U810A-3
POWERON	U210-11
RECALL	U118C-8
SDO	P310-25B
SELEN	U815C-6
SNOR	U210@12
SSRST	P310-28A
STORE	U110D-11
WHEMSEL	J815
W/R	U810B-6
Y3	U610-12

TYPE	+5VL	+5V	+5VH	-5V
2764	1,26, 27,28		14	
6116	24		12	
74LS00	14		7	
74LS02	14		7	
74LS10	14		7	
74LS14		14	7	
74123	16		8	
74LS132		14	7	
74LS138	16		8	
74LS164	14		7	
74LS174	16		8	
74LS245	20		10	
74LS257	16		8	
74LS259	16		8	
74LS374	20		10	
87101CN		19		20 18
CD4051		16	8	7
CD4053		16	8	7
X2201			9	

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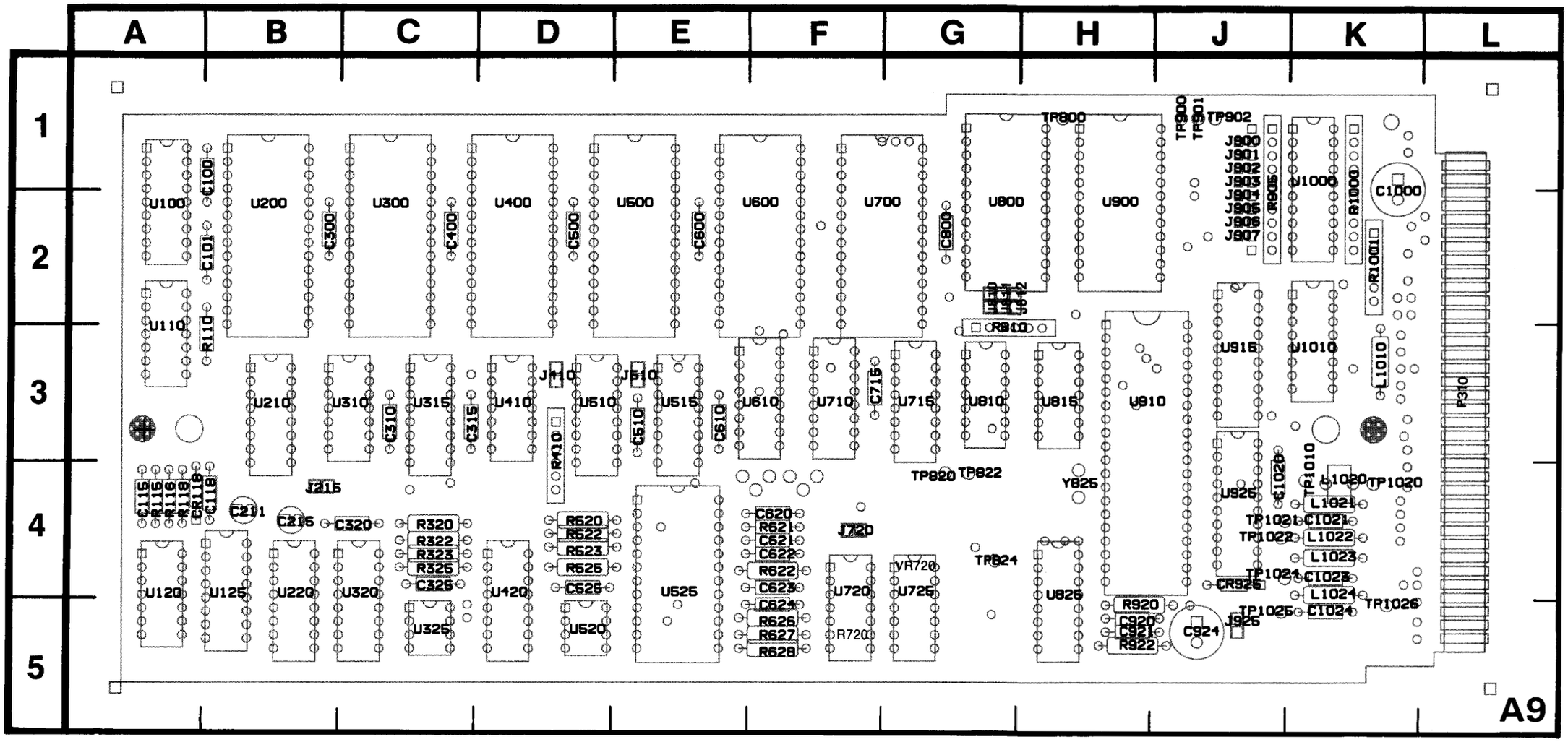
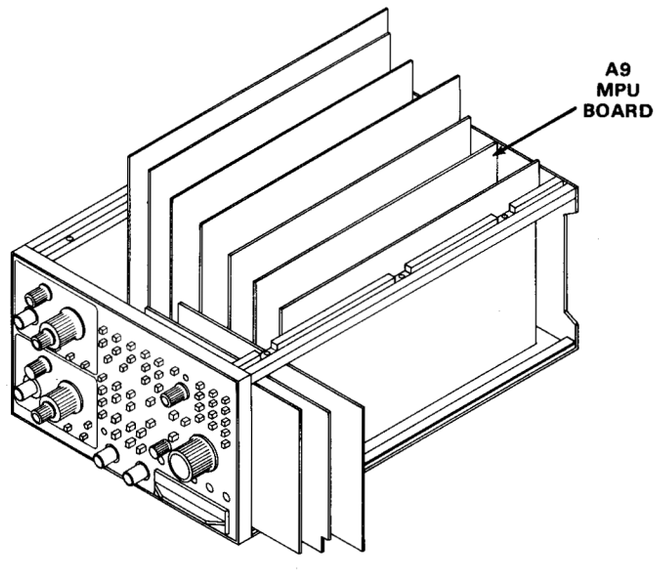


3858-909B

Fig. 7-11B. A9—MPU circuit board assembly (SN B061869 & below).



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MPU CONTROL DIAGRAM (SN B061869 & BELOW) 12

ASSEMBLY A9

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	A5	B1
C101	A5	B2
C115	G5	A4
C118	G5	B4
C211	G5	B4
C215	G6	B4
C300	A5	B2
C310	A5	C3
C315	A5	C3
C320	A5	C4
C325	A6	C4
C400	A5	C2
C500	A5	D2
C510	A5	E3
C525	A5	D4
C600	A5	E2
C610	B5	E3
C620	G3	F4
C621	A5	F4
C622	A5	F4
C623	G4	F4
C624	G3	F5
C715	B5	F3
C800	B5	G2
C920	B3	H5
C921	B3	H5
C924	B4	J5
C1000	A5	K1
C1020	B5	J4
C1021	A5	K4
C1023	A5	K4
C1024	A6	K5
CR118	G5	A4
CR925	B4	J4
J215	E3	B4
J410	H4	D3
J510	H3	E3
J810	A4	G2
J811	A4	G2
J812	B4	G2
J900	C2	J1
J901	C1	J1
J902	C1	J1
J903	C1	J1
J904	C2	J2
J905	C1	J2
J906	C1	J2
J907	C2	J2
J925	A4	J5
L1010	A5	K3
L1020	A5	K4
L1021	A5	K4
L1022	A6	K4
L1023	A5	K4
L1024	A5	K4
P310	A1	L3
P310	F3	L3
P310	I1	L3
R110	G5	B3
R115	G5	A4
R116	G6	A4
R118	G5	A4
R320	F4	C4
R322	F4	C4
R323	E4	C4
R325	E4	C4
R410A	H3	D3
R410B	H3	D3
R410E	A3	D3
R520	E5	D4
R522	F5	D4
R523	F5	D4
R525	E5	D4
R621	G4	F4
R622	G3	F4
R626	G4	F5
R627	G4	F5
R628	G3	F5
R720	B4	F5
R810A	B4	G3
R810B	B4	G3
R810C	A4	G3
R810D	B4	G3
R905A	B3	J2
R905B	B2	J2
R905C	B1	J2
R905D	B1	J2
R905E	B1	J2
R905F	B2	J2
R905G	B1	J2
R905H	B1	J2
R905J	B2	J2
R920	B3	H4
R922	B3	H5
R1000A	B2	K1
R1000B	A1	K1
R1000C	A1	K1
R1000D	A1	K1
R1000E	A2	K1
R1000F	A1	K1
R1000G	A1	K1
R1000H	A2	K1
R1000J	A2	K1
R1001A	H5	K2
R1001B	H5	K2
R1001	I1	K2
TP800	A3	H1
TP820	C3	G4
TP822	C2	G4
TP824	C3	G4
TP902	B4	J1
TP1010	A5	K4
TP1020	A3	K4
TP1021	A4	J4
TP1022	A6	J4
TP1024	A5	J4
TP1025	A6	J5
TP1026	A5	K5
U100	H1	A2
U110A	G5	A3
U110B	G5	A3
U110C	H5	A3
U110D	H5	A3
U120A	G5	A4
U120B	G5	A4
U120C	G5	A4
U120D	G6	A4
U120E	H5	A4
U120F	G6	A4
U125	G4	B4
U200	F1	B2
U210	E3	B3
U220	G3	B4
U300	F1	C2
U310	E4	C3
U315	E4	C3
U320	F4	C4
U325A	F6	C5
U325B	F4	C5
U400	E1	D2
U410	E5	D3
U420	F5	D4
U500	G1	E2
U510	H3	D3
U515	H2	E3
U520	B5	D5
U525	G3	E4
U600	F2	F2
U610	D3	F3
U700	G2	G2
U710	D1	F3
U715	D2	G3
U720A	D3	F4
U720B	D3	F4
U720C	B4	F4
U720D	B4	F4
U725A	D2	G4
U725B	D2	G4
U725C	A2	G4
U725D	A2	G4
U800	F2	G2
U810A	D1	G3
U810B	C2	G3
U810C	A3	G3
U810D	D2	G3
U815A	B3	H3
U815B	A3	H3
U815C	B3	H3
U825A	B3	H4
U825B	B3	H4
U900	E2	H2
U910	C4	H3
U915	H5	J3
U925	H5	J4
U1000	B1	K1
U1010	H1	K3
VR720	B4	G4
Y825	B5	H4

Partial A9 also shown on diagrams 5 and 9.

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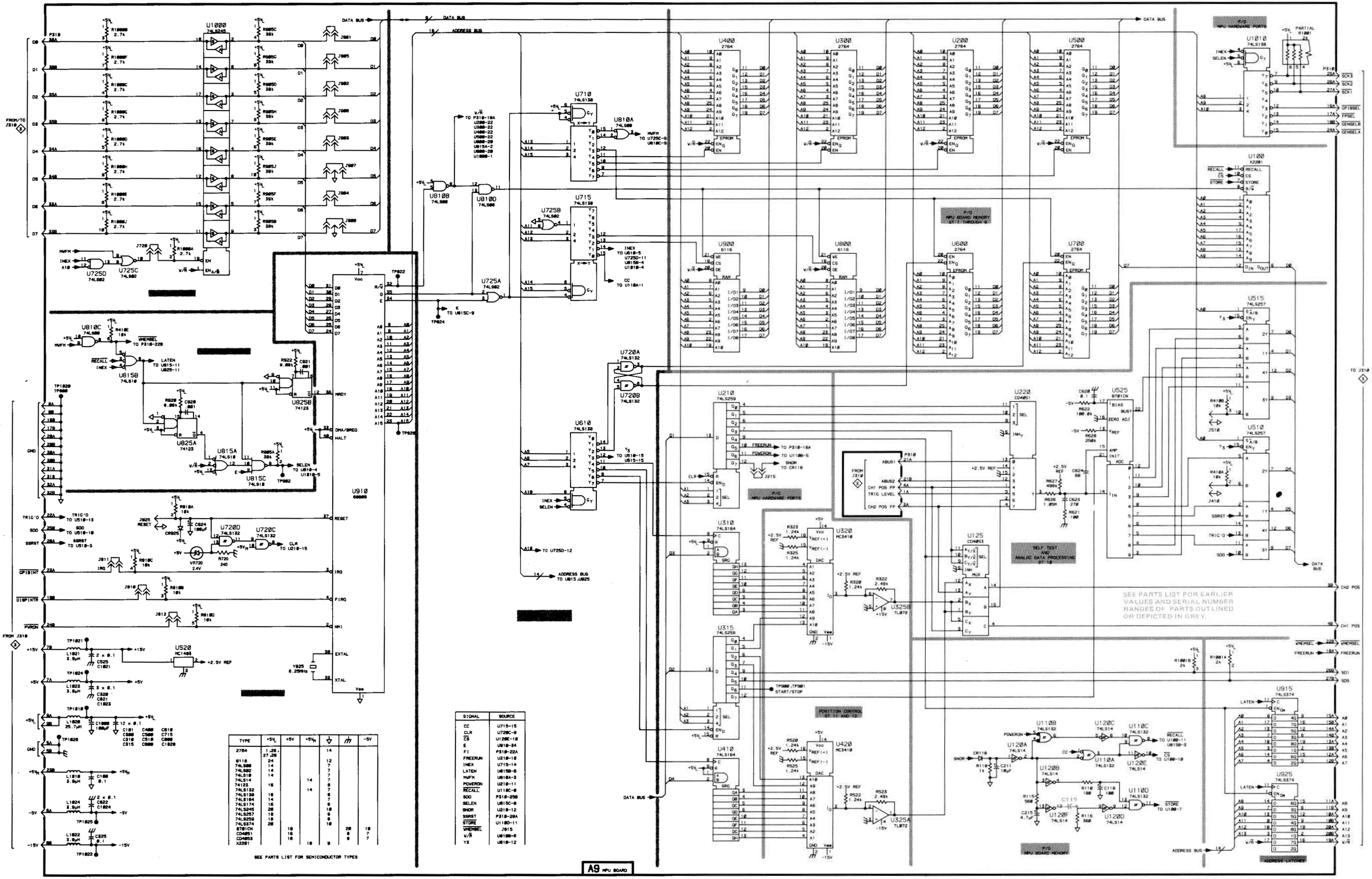

SIGNAL	SOURCE
CC	U715-15
CLR	U720C-8
CS	U120E-10
E	U810-34
FI	P310-22A
FREERUN	U210-10
INEX	U715-14
LATEN	U815B-6
MWFH	U810A-3
POWERON	U210-11
RECALL	U110C-8
SOD	P310-25B
SELEN	U815C-8
SNOR	U210-12
SSRST	P310-28A
STORE	U110D-11
WMEMSEL	J815
V/R	U810B-6
YS	U610-12

TYPE	+5V	+5V	+5VH			-5V
2764	1,26, 27,28			14		
6116	24			12		
74LS08	14			7		
74LS02	14			7		
74LS10	14			7		
74LS14			14	7		
74123	16			8		
74LS132			14	7		
74LS138	16			8		
74LS164	14			7		
74LS174	16			8		
74LS245	20			10		
74LS257	16			8		
74LS259	16			8		
74LS374	20			10		
8701CN		19			20	19
CD4051		16			8	7
CD4053		16			8	7
X2201			18	9		

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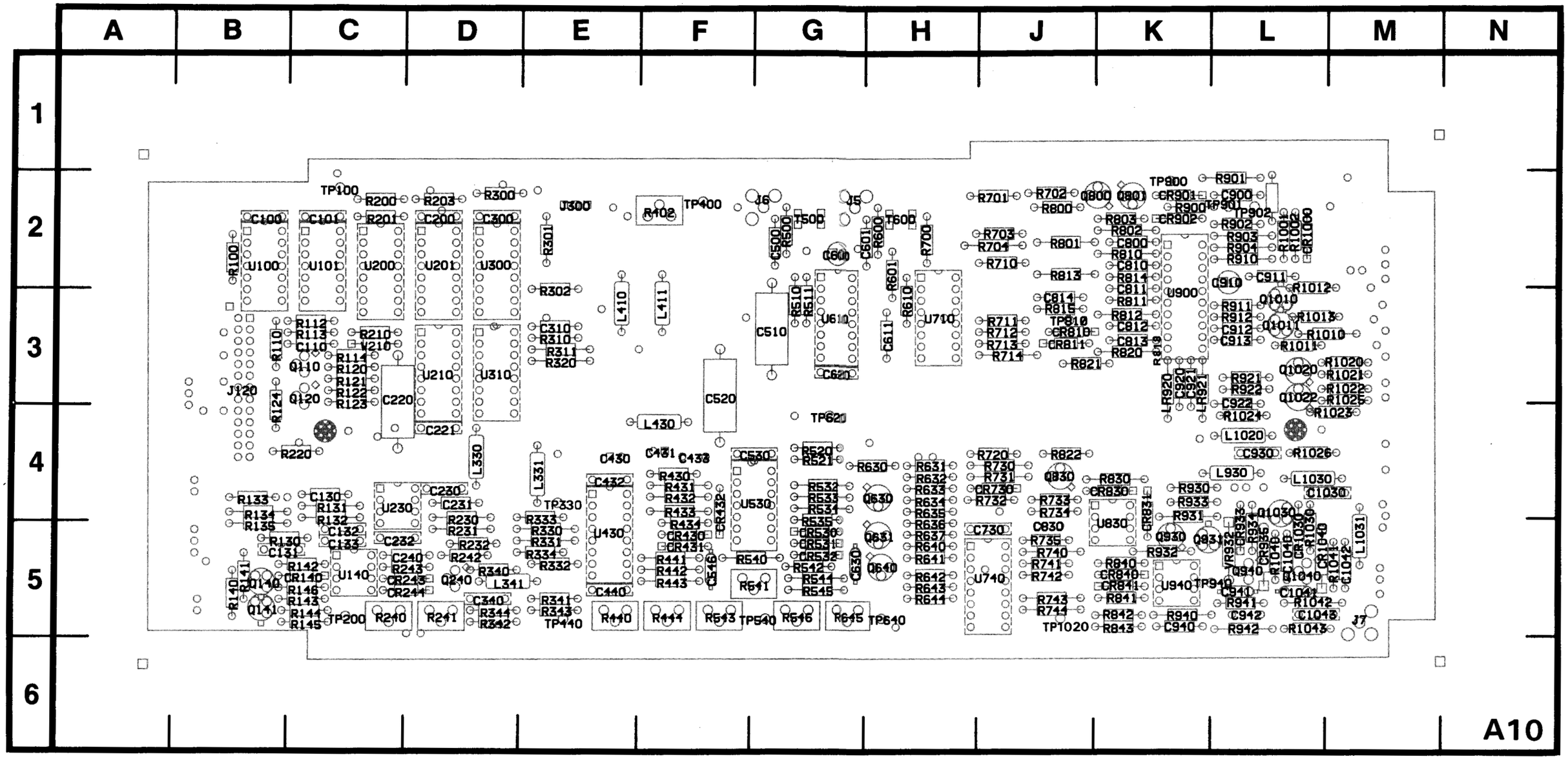
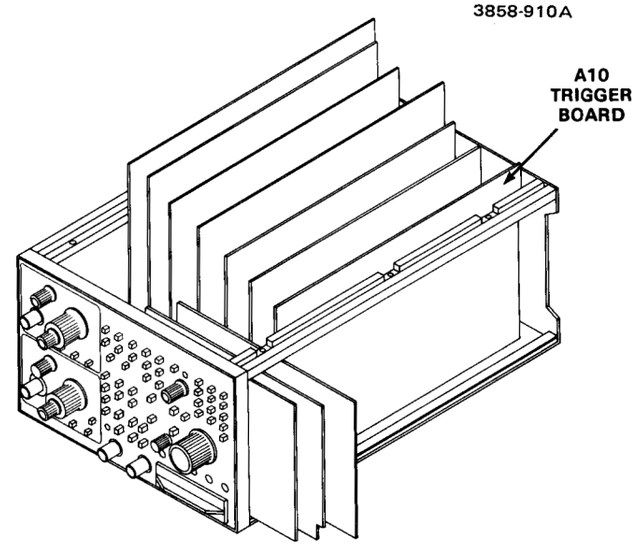


Figure 7-12. A10—Trigger circuit board assembly.

3858-910A



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TRIGGER DIAGRAM 13

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	A2	B2
C101	A2	C2
C110	D2	C3
C130	C1	C4
C131	G1	B5
C132	H3	C5
C133	A2	C5
C200	A2	D2
C220	A2	C3
C221	A2	D4
C230	A2	D4
C231	C1	D4
C232	A3	C5
C240	H1	D5
C300	A2	D2
C310	B2	E3
C340	G1	D5
C430	A3	E4
C431	A2	F4
C432	A2	E4
C433	D3	F4
C440	H3	E5
C500	A3	G1
C510	H3	G2
C520	A2	F3
C530	A2	G4
C546	G4	F5
C600	D4	G1
C601	A3	H2
C611	B4	H3
C620	H3	G2
C630	G3	G5
C730	A2	J5
C800	D3	K2
C810	D3	K2
C811	E4	K2
C812	D5	K3
C813	E3	K3
C814	E6	J3
C830	B5	J5
C900	E3	L2
C910	F3	L2
C911	E6	L2
C912	E5	L3
C913	E6	L3
C920	F4	K3
C921	F3	K3
C922	C6	L3
C930	A2	L4
C940	A4	K5
C941	A4	L5
C942	A4	L5
C1030	A3	M4
C1040	A2	L5
C1041	A4	L5
C1042	C4	M5
C1043	A4	L5
CR140	H1	C5
CR243	H1	D5
CR244	G1	D5
CR430	F4	F5
CR431	G4	F5
CR432	G4	F4
CR530	G3	G5
CR531	G3	G5
CR532	F3	G5
CR730	F3	J4
CR810	C4	J3
CR811	C4	J3
CR830	C4	K4
CR831	C4	K4
CR840	A5	K5
CR841	A5	K5
CR901	F3	K2
CR902	F3	K2
CR933	C4	L5
CR935	B4	L5
CR1000	E5	L2
CR1030	C4	L5
CR1040	B4	L5
J5	A3	G1
J6	A3	G1
J7	A4	M5
J7	A4	M5
L330	A2	D4
L331	A2	E4
L341	G1	D5
L410	A2	E3
L411	A1	F3
L430	A2	F4
L930	A2	L4
L1020	A2	L4
L1030	A1	L4
L1031	H3	M5
LR920	F4	K3
LR921	F3	K3
Q110	D1	C3
Q120	G2	C3
Q140	H1	B5
Q141	H1	B5
Q240	G1	D5
Q630	C4	H4
Q631	B4	H5
Q640	A5	H5
Q800	D6	K2
Q801	D6	K2
Q830	C5	J4
Q930	B5	K5
Q931	C4	K5
Q940	C4	L5
Q1010	F5	L3
Q1011	F4	L3
Q1020	C6	L3
Q1022	C6	L3
Q1030	C4	L4
Q1040	C4	L5
R100	D1	B2
R110	F1	B3
R112	B1	C3
R113	F2	C3
R114	D1	C3
R120	D1	C3
R121	G2	C3
R122	G2	C3
R123	G2	C3
R124	G2	B4
R130	H1	B5
R131	C1	C4
R132	C1	C4
R133	B3	B4
R134	D1	B4
R135	D1	B5
R140	H1	B5
R141	H1	B5
R142	H1	C5
R143	H1	C5
R144	H1	C5
R145	H1	C5
R146	H1	C5
R200	B1	C2
R201	B1	C2
R203	B2	D2
R210	H1	C3
R220	D1	C4
R230	B1	D4
R231	B1	D5
R232	G1	D5
R240	A5	C5
R241	B5	D5
R242	H1	D5
R243	G1	D5
R300	E2	D2
R301	E3	E2
R302	C2	E3
R310	C2	E3
R311	C2	E3
R320	C2	E3
R330	G4	E5
R331	G4	E5
R332	E5	E5
R333	A2	E4
R334	G1	E5
R340	G1	D5
R341	G3	E5
R342	H3	D5
R343	G4	E5
R344	G1	D5
R402	B2	F2
R430	D2	F4
R431	G4	F4
R432	G4	F4
R433	G3	F4
R434	G4	F5
R440	E6	E5
R441	G4	F5
R442	F4	F5
R443	F4	F5
R444	E5	F5
R500	A3	G1
R510	D4	G2
R511	D4	G2
R520	D3	G4
R521	F4	G4
R532	C3	G4
R533	D3	G4
R534	C3	G4
R535	D3	G5
R540	F3	G5
R541	D3	G5
R542	G3	G5
R543	E3	F5
R544	G3	G5
R545	F3	G5
R546	F4	G5
R600	A3	H2
R601	C3	H2
R610	B3	H3
R630	F3	H4
R631	B4	H4
R632	B4	H4
R633	B4	H4
R634	C4	H4
R635	B4	H4
R636	B4	H5
R637	B4	H5
R640	B4	H5
R641	B4	H5
R642	A5	H5
R643	A5	H5
R644	A5	H5
R645	F3	G5
R700	C3	H2
R701	D6	J2
R702	D6	J2
R703	E4	J2
R704	D5	J2
R710	E4	J2
R711	D4	J3
R712	D4	J3
R713	E3	J3
R714	D5	J3
R720	C5	J4
R730	F3	J4
R731	F3	J4
R732	F3	J4
R733	C5	J4
R734	B5	J4
R735	B5	J5
R740	B5	J5
R741	C5	J5
R742	B5	J5
R743	B5	J5
R744	B5	J5
R800	D6	J2
R801	B3	J2
R802	E4	K2
R803	D6	K2
R810	E4	K2
R811	E4	K3
R812	D4	K3
R813	B3	J2
R814	D6	K2
R815	E6	J3
R818*	E3	K3
R820	E3	K3
R821	D4	J3
R822	C5	J4
R830	F3	K4
R840	A5	K5
R841	A5	K5
R842	B5	K5
R843	A4	K5
R900	E3	K2
R901	E3	L2
R902	F3	L2
R903	E3	L2
R904	E3	L2
R910	E3	L2
R911	F5	L3
R912	F4	L3
R921	E6	L3
R922	A6	L3
R930	C5	K4
R931	B5	K4
R932	B5	K5
R933	C4	K4
R934	C5	L5
R940	A5	K5
R941	A4	L5
R942	A4	L5
R1001	F3	L2
R1002	E5	L2
R1010	F5	L3
R1011	F4	L3
R1012	F5	L2
R1013	F5	L3
R1020	C6	M3
R1021	C6	M3
R1022	C6	M3
R1023	D6	M4
R1024	D6	L4
R1025	C6	M3
R1026	G1	L4
R1030	C4	L5
R1040	C4	L5
R1041	C4	M5
R1042	A4	L5
R1043	A4	L5
T500	A3	G1
T600	A3	H2
TP100	H3	C2
TP200	H3	C5
TP400	C2	F2
TP440	D3	E5
TP540	G4	G5
TP620	H3	G4
TP640	G3	H5
TP810	C4	J3
TP900	H3	K2
TP901	E3	L2
TP902	E3	L2
TP940	H3	L5
U100A	G2	B2
U101B	F2	C2
U101C	G2	C2
U101D	B1	C2
U140	G1	C5
U200	D3	C2
U200	E2	C2
U201	C2	D2
U210	B1	D3
U230A	C1	C4
U230B	C1	C4
U300	E2	D2
U310	C2	D3
U430A	D2	E5
U430B	G4	E5
U430C	G3	E5
U430	G3	E5
U530A	H4	G4
U530B	F4	G4
U530C	G3	G4
U530D	D3	G4
U610A	D4	G2
U610B	D4	G2
U610C	D4	G2
U610	G3	G2
U710	D3	H3
U740A	B5	J5
U740B	B5	J5
U740	G3	J5
U830A	C5	K5
U830B	F3	K5
U900	E4	K3
U940	B5	K5
VR932	C4	L5
W210	D2	C3

Partial A10 also shown on diagrams 8 and 9.

***See Parts List for serial number ranges.**

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VOLTAGE CONDITIONS

Use a digital voltmeter with a 10 MΩ input impedance such as the TEKTRONIX DM 501A Digitial Multimeter installed in a TM 500- or TM 5000-series power module, or a TEKTRONIX 7D13A Digital Multimeter in a readout-equipped Tektronix 7000-series oscilloscope mainframe. Connect the voltmeter ground lead to A10TP900.

Setup the 7D20 as follows:

Turn off power to the oscilloscope mainframe. Remove A10 Trigger Board and place it on the 067-1050-00 extender board. Refer to the A10 Trigger Board removal procedure in the Maintenance section of this manual. Turn on oscilloscope mainframe power when A10 has been extended.

Set the TRIGGERING LEVEL control to midrange.

Initialize the 7D20 control settings as follows:

a. Press MENU (pushbutton will light).

b. If MASTER MENU is not displayed, press MEMORY DISPLAY pushbutton number 6.

c. From displayed MASTER MENU list select UTILITIES by pressing MEMORY DISPLAY pushbutton number 4.

d. From displayed UTILITIES list select INIT FRONT PANEL by pressing MEMORY DISPLAY pushbutton number 5.

e. To return to MASTER MENU, press MEMORY DISPLAY pushbutton number 6. To turn off MASTER MENU display, press MENU.

Selectable Electrical Parts Table
For Diagram 13

Component Number	Reason For Selection	Component Value (See Replaceable Electrical Parts)
A10R730	To obtain peak-to-peak trigger offset parameters.	226 kΩ 232 kΩ 237 kΩ

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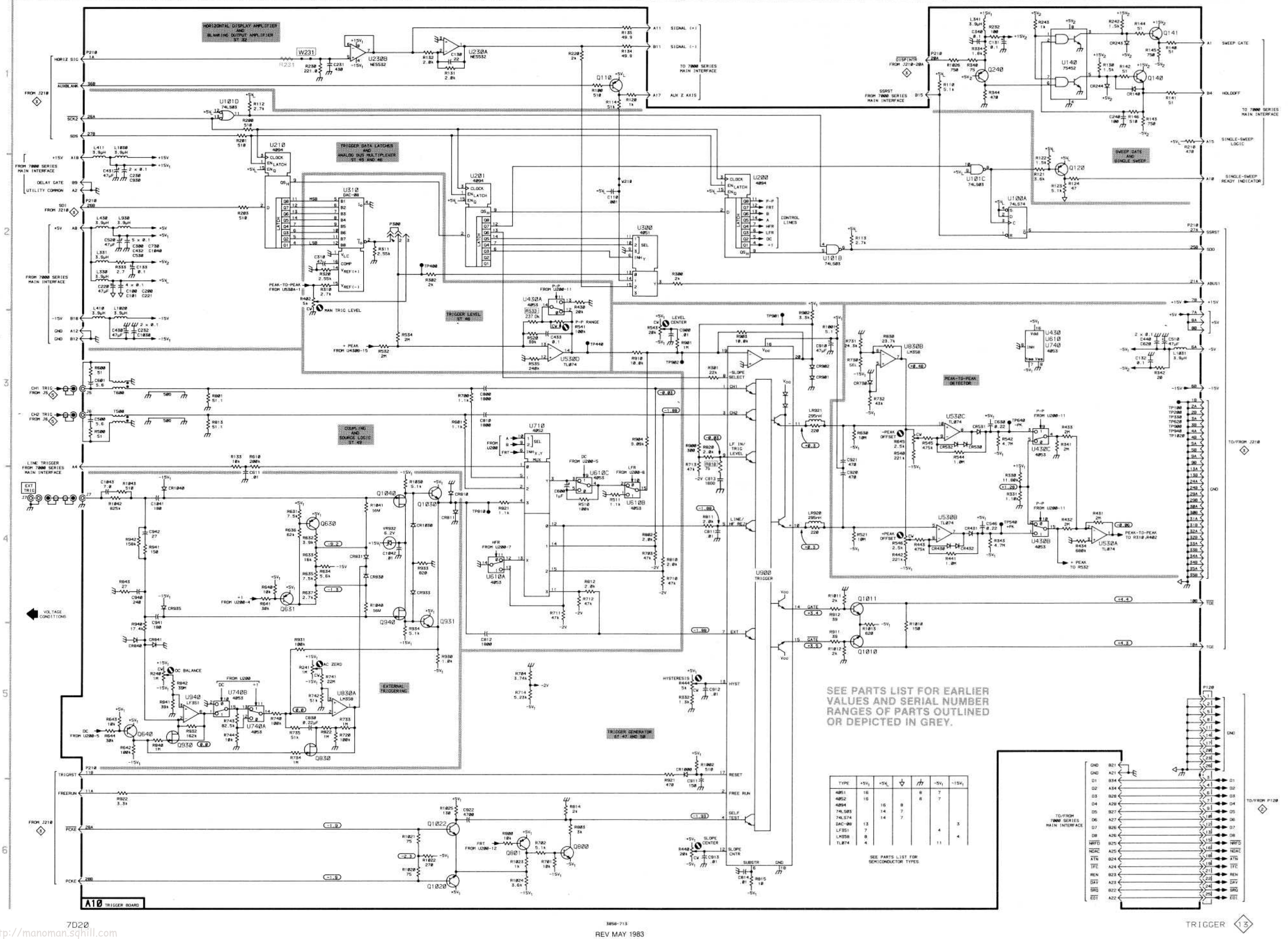

TYPE	+5V2	+5VL	⏚	⫫	-5V1	-15V1
4051	16			8	7	
4052	16			8	7	
4094		16	8			
74LS03		14	7			
74LS74		14	7			
DAC-08	13					3
LF351	7				4	
LM358	8					4
TL074	4				11	

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

3858-713
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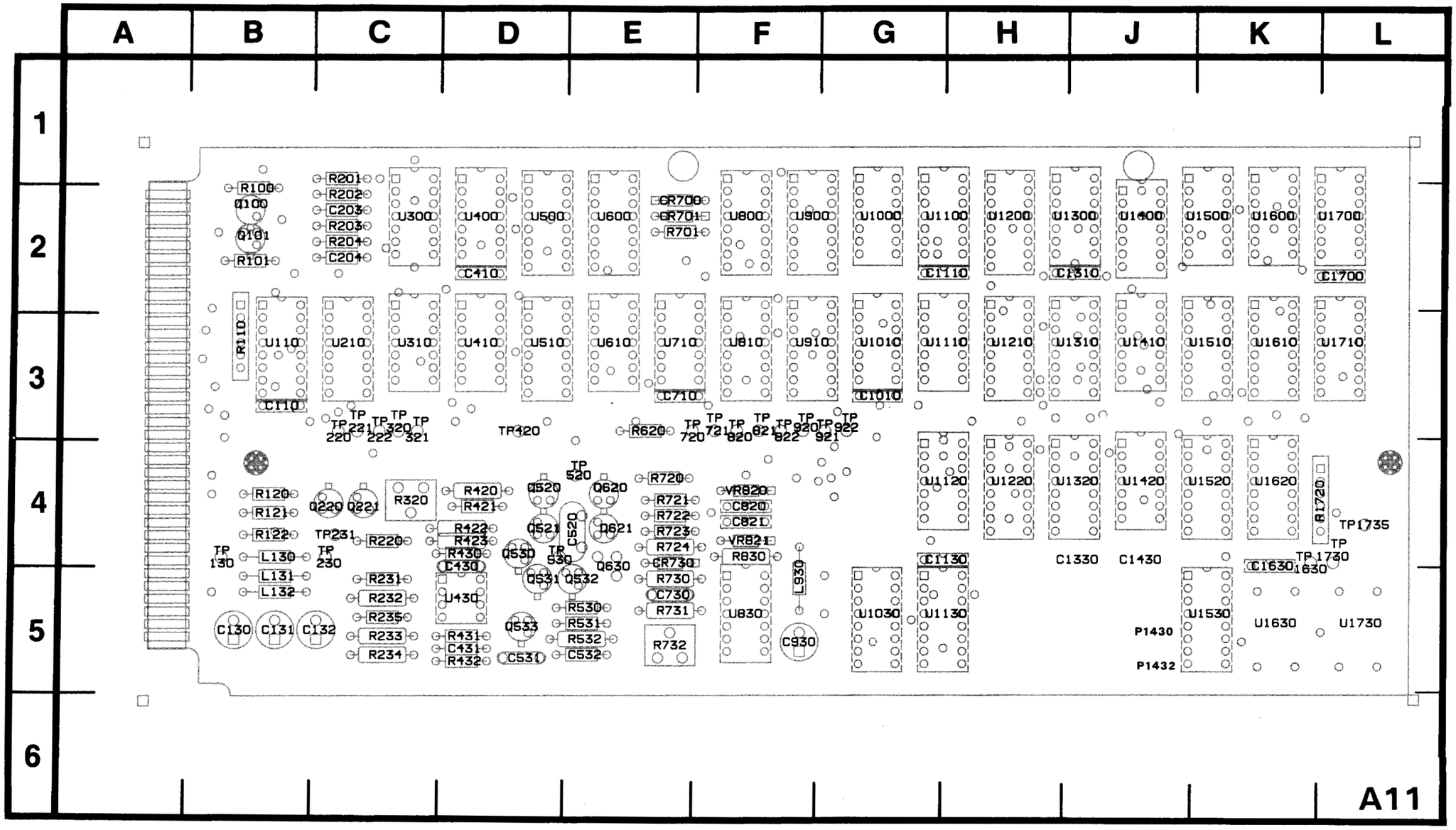
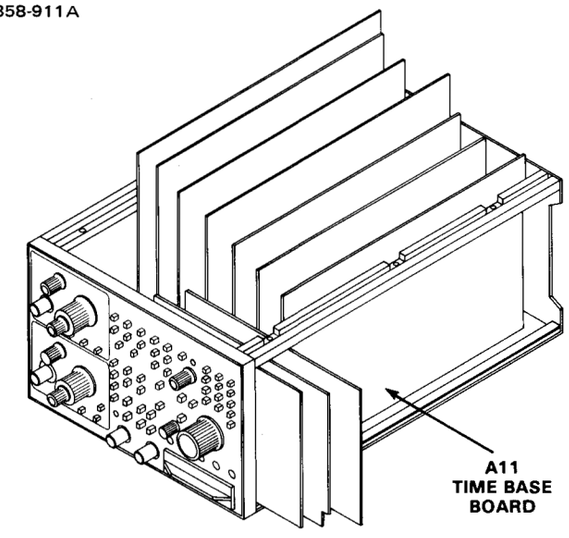


Figure 7-13. A11—Timebase circuit board assembly.

3858-911A



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CLOCK GENERATOR DIAGRAM 14

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C203	G1	C2	R620	G5	E3	U410D	B3	D3
C204	G1	C2	R701	D5	E2	U500A	D4	D2
			R1720B	E1	L4	U500B	E4	D2
CR700	D5	E2	R1720C	E1	L4	U510	B2	D3
CR701	D5	E2				U600A	E4	E2
P1430 *	B1	J5	TP220	C3	C3	U600B	F5	E2
P1432 *	A1	J5	TP221	C3	C3	U610A	G2	E3
Q100	H1	B2	TP222	C3	C3	U610B	H3	E3
Q101	H1	B2	TP320	C3	C3	U710A	G2	E3
R100	D5	B2	TP321	B2	C3	U710B	F3	E3
R101	G1	B2	TP921	E1	G3	U710D	B2	E3
R110A	A4	B3	TP922	H3	G3	U800	F3	F2
R110B	A4	B3	TP1630	A1	K4	U810	B5	F3
R110C	C5	B3	TP1730	B1	L4	U900	D3	F2
R110E	C5	B3	TP1735	A1	L4	U1000B	E1	G2
R201	G1	C1				U1100D	D1	G2
R202	G1	C2	U210B	C5	C3	U1220A	E1	H4
R203	G1	C2	U300A	B4	C2	U1420A	F2	J4
R204	G1	C2	U300B	C4	C2	U1420B	D1	J4
R620	A2	E3	U400A	E5	D2	U1520A	B1	K4
R620	B2	E3	U400B	C5	D2	U1520B	B1	K4
R620	G3	E3	U400C	A3	D2	U1530	C1	K5
R620	G3	E3	U410A	E5	D3	U1630	A1	K5
R620	G6	E3	U410B	B3	D3	U1730	B1	L5

Partial A11 also shown on diagrams 15 and 16.

***See Parts List for serial number ranges.**

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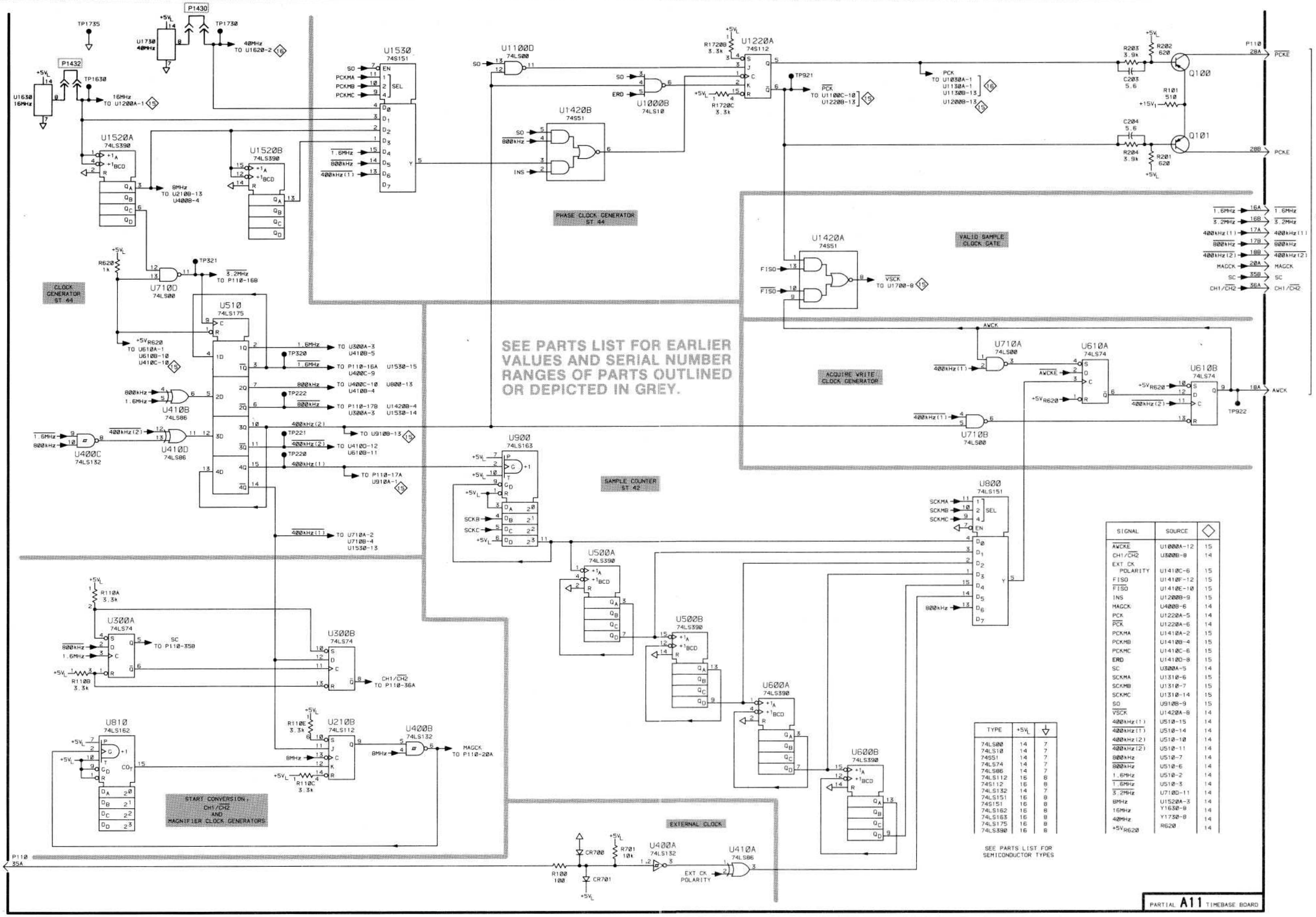

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ACQUIRE CONTROL DIAGRAM 15

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C110	A3	B3
C130	A3	B5
C410	A3	D2
C710	A3	E3
C1010	A3	G3
C1110	A3	G2
C1130	A3	H4
C1310	B3	J2
C1330	B3	J4
C1430	B3	J4
C1630	B3	K4
C1700	B3	L2
L130	A3	B4
R620	A5	E3
R620	B5	E3
R620	D5	E3
R1720A	E3	L4
R1720D	D2	L4
TP230	A3	C4
TP720	E5	F3
TP721	E2	F3
TP820	F3	F3
TP821	G4	F3
TP822	F1	F3
TP920	G3	F3
U110A	G2	B3
U110B	E5	B3
U310D	F4	C3
U410C	D5	D3
U710C	E5	E3
U910A	G3	F3
U910B	F4	F3
U1000A	F1	G2
U1000C	F1	G2
U1010A	F3	G3
U1010D	E5	G3
U1100A	G3	G2
U1100B	E1	G2
U1100C	E1	G2
U1120A	E2	H4
U1200A	E2	H2
U1200B	E3	H2
U1210	D5	H3
U1220B	E1	H4
U1300	D3	J2
U1310	C3	J3
U1320	D4	J4
U1400	D2	J2
U1410D	C2	J3
U1410E	F3	J3
U1410F	F3	J3
U1410	D4	J3
U1500	C2	K2
U1510	C3	K3
U1600	C1	K2
U1610	B2	K3
U1700	B1	L2
U1710	B1	L3

Partial A11 also shown on diagrams 14 and 16.

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POST-TRIGGER COUNTER ST 43 AND 42

ACQUIRE WAVEFORM CLOCK ENABLE

SERIAL DATA LATCHES ST 39

END ACQUIRE ST 41

FAST-IN,SLOW-OUT LOGIC

SIGNAL	SOURCE	◇
$\overline{AWCKE}$	U1000A-12	15
A4	P110-13A	15
$\overline{EORD}$	U1610-11	15
EHO	U1200A-5	15
$\overline{ENDACQ}$	U910A-6	15
EXT CK POLARITY	U1410C-6	15
FISO	U1410F-12	15
$\overline{FISO}$	U1410E-10	15
$\overline{FISOUB}$	U1610-12	15
$\overline{GENSELA}$	P110-24A	15
$\overline{INIT}$	U1010D-11	15
INS	U1200B-7	15
$\overline{LOAD}$	U1120A-3	15
MEA	P110-33A	15
PCK	U1220A-5	14
$\overline{PCK}$	U1220A-6	14
PCKMA	U1410A-2	15
PCKMB	U1410B-4	15
PCKMC	U1410C-6	15
	U1410D-8	15
SCKB	U1310-4	15
SCKC	U1310-5	15
SCKMA	U1310-6	15
SCKMB	U1310-7	15
SCKMC	U1310-14	15
SCK3	P110-25A	15
SDS	P110-27B	15
SO	U910B-9	15
$\overline{STC}$	U1130A-7	16
TGP	U1010C-8	16
TRIGRST	U1200A-6	15
$\overline{VSCK}$	U1410A-8	14
400kHz(1)	U510-15	14
400kHz(2)	U510-10	14
16MHz	U1630-8	14
$+5V_{R620}$	R620	14

TYPE	$+5V_L$	⏚
4094	16	8
74LS00	14	7
74LS02	14	7
74LS04	14	7
74S08	14	7
74LS86	14	7
74S112	16	8
74LS165	16	8
74LS197	14	7
74LS368	16	8

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

PARTIAL **A11** TIMEBASE BOARD

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FAST RAMP INTERPOLATOR DIAGRAM 16

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C131	A4	B5
C132	A4	C5
C430	A4	D4
C431	B3	D5
C520	C3	E4
C531	A4	D5
C532	A3	E5
C730	A4	E5
C820	C4	F4
C821	C4	F4
C930	B4	F5
CR730	C3	E4
L131	A4	B5
L132	A4	B5
L930	B4	F5
Q220	B1	C4
Q221	B1	C4
Q520	B2	D4
Q521	C2	D4
Q530	B3	D4
Q531	B3	D5
Q532	C3	E5
Q533	A3	D5
Q620	B1	E4
Q621	C2	E4
Q630	C3	E4
R120	A1	B4
R121	A2	B4
R122	A1	B4
R220	B1	C4
R231	B3	C5
R232	B3	C5
R233	B3	C5
R234	B3	C5
R235	A3	C5
R320	A3	C4
R420	B2	D4
R421	A2	D4
R422	C2	D4
R423	C2	D4
R430	B2	D4
R431	B3	D5
R432	B3	D5
R530	B3	E5
R531	E2	E5
R532	A3	E5
R720	A1	E4
R721	B1	E4
R722	C2	E4
R723	B2	E4
R724	C3	E4
R730	A3	E5
R731	D3	E5
R732	D3	E5
R830	D3	F4
R1720B	C1	L4
R1720E	D1	L4
TP130	G1	B4
TP231	B1	C4
TP420	G1	D3
TP520	C3	E4
TP530	C3	D4
U430A	B3	D5
U430B	B3	D5
U830	D3	F5
U830	D4	F5
U1010B	D1	G3
U1010C	C1	G3
U1030A	D1	G5
U1110A	F2	G3
U1110B	G3	G3
U1120B	D3	H4
U1120C	E2	H4
U1120D	D1	H4
U1130A	C1	G5
U1130B	E2	G5
U1620	F2	K4
VR820	D4	F4
VR821	D4	F4

Partial A11 also shown on diagrams 14 and 15.

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VOLTAGE CONDITIONS

Use a digital voltmeter with a 10 MΩ input impedance such as the TEKTRONIX DM 501A Digital Multimeter installed in a TM 500- or TM 5000-series power module, or a TEKTRONIX 7D13A Digita Multimeter in a readout-equipped Tektronix 7000-series oscilloscope mainframe. Connect the voltmeter ground lead to A11TP520.

There is no special 7D20 setup required.

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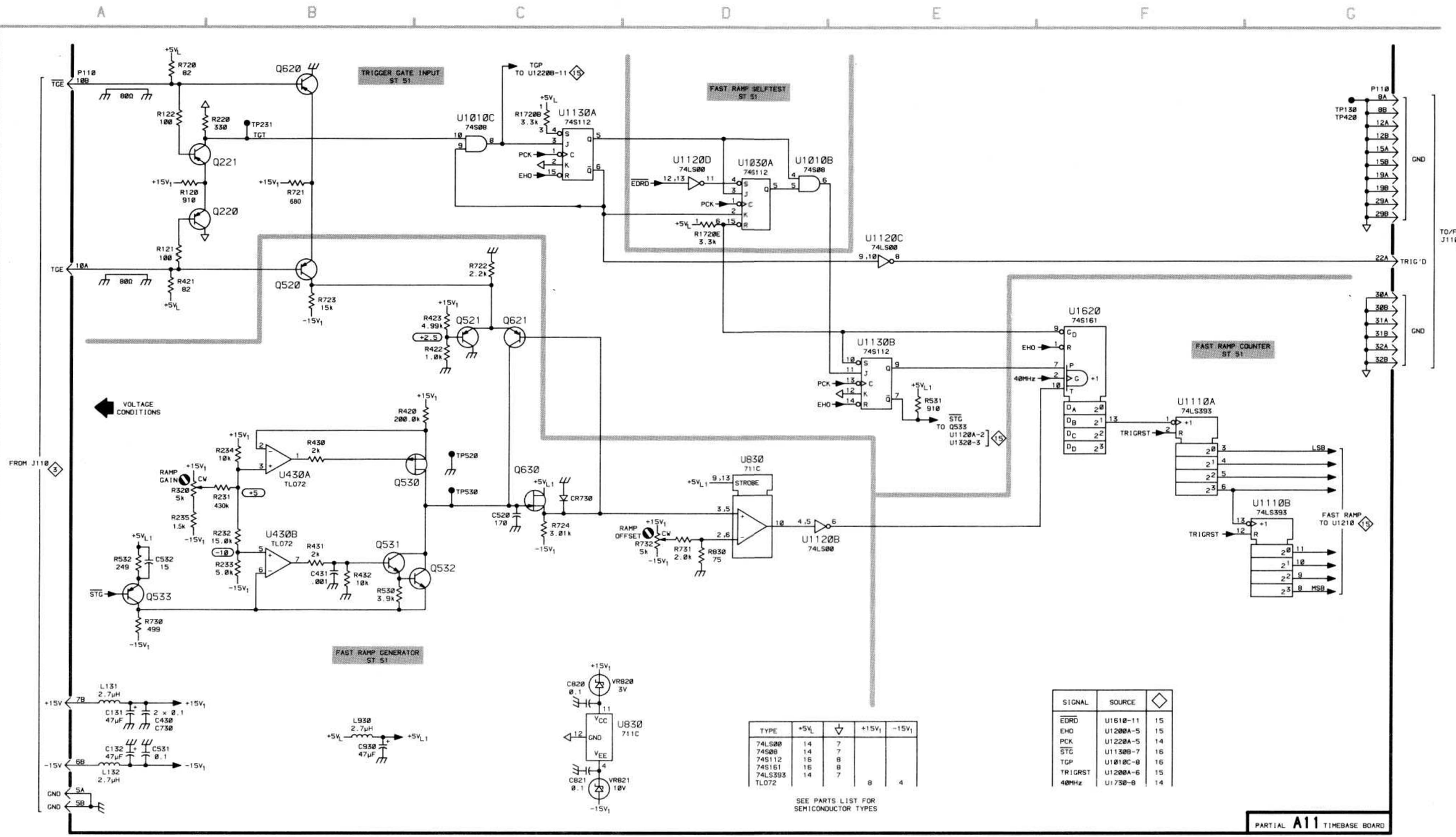

TYPE	+5V$_L$	⏚	+15V$_I$	-15V$_I$
74LS00	14	7		
74S00	14	7		
74S112	16	8		
74S161	16	8		
74LS393	14	7		
TL072			8	4

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

SIGNAL	SOURCE	◇
$\overline{\text{EDRD}}$	U1610-11	15
EHO	U1200A-5	15
PCK	U1220A-5	14
$\overline{\text{STG}}$	U1130B-7	16
TCP	U1010C-8	16
TRIGRST	U1200A-6	15
40MHz	U1730-8	14

PARTIAL A11 TIMEBASE BOARD

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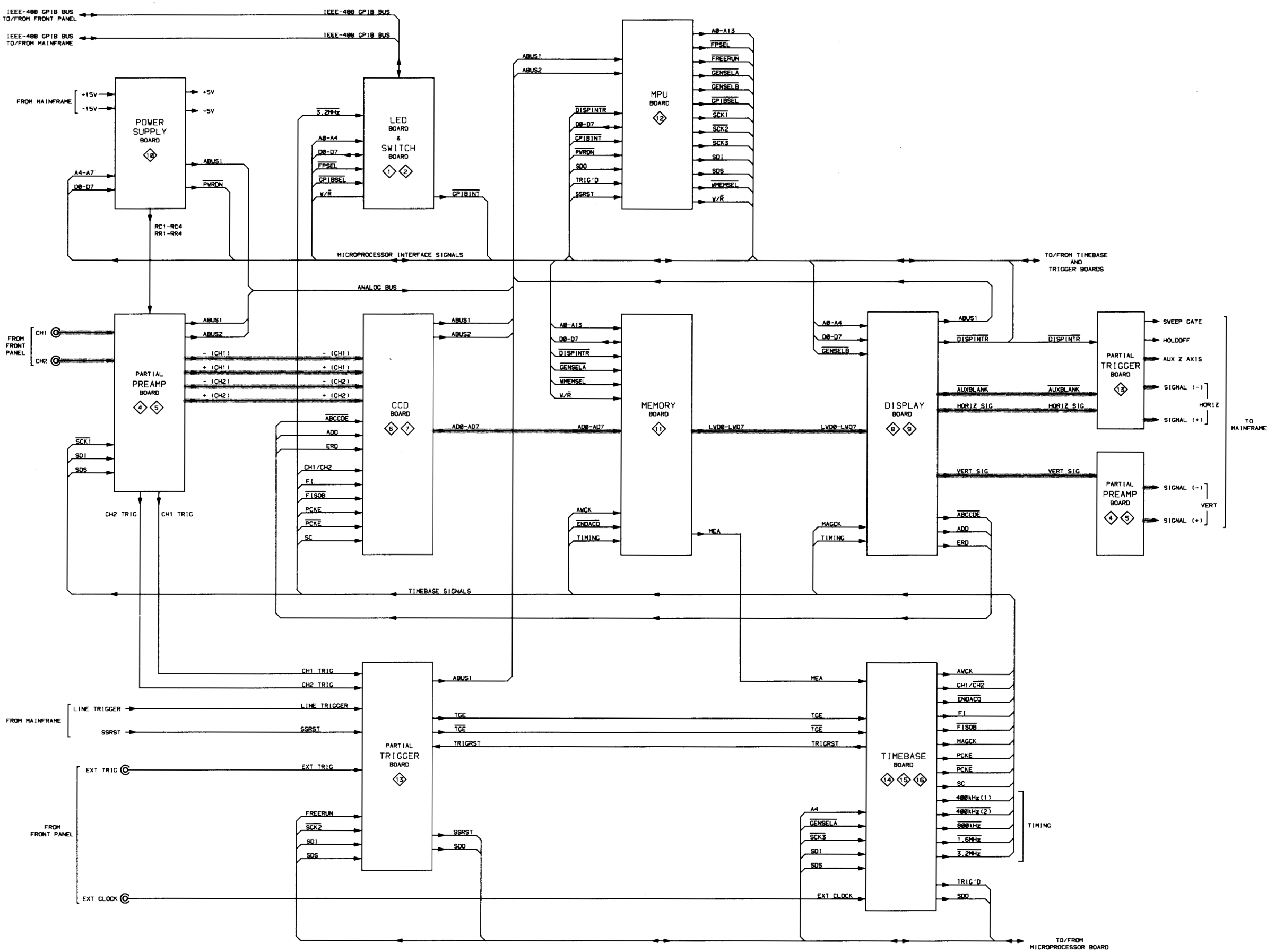

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SIGNATURE ANALYSIS TABLES

NOTE

Signature Tables are individually tabbed according to firmware version. These version numbers correspond to the firmware version information displayed on the crt. For further firmware version information refer to the 7D20 Operators Manual as follows:

1. Operating Instructions section for front-panel ID information.
2. GPIB section for GPIB Mode Terminator, and Address Selection information.

The "Firmware Version to Circuit Board Cross Reference" Table 7-1, which follows, should be referenced each time a 7D20 is serviced.

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TABLE 7-1
Firmware Version To Circuit Board Cross-Reference

Assembly Number & Board Name	Version 1.00	Version 1.01	Version 1.02	Version 1.03
A1 Switch Board	670-7315-00	670-7315-00	670-7315-00	670-7315-00
A2 LED Board	670-7316-00	670-7316-00	670-7316-00	670-7316-00
A3 Interconnect Board	670-7317-00	670-7317-00	670-7317-00	670-7317-00
A4 Preamplifier Board	670-7318-00	670-7318-00	670-7318-00	670-7318-00
A5 CCD Board	670-7319-00	670-7319-00	670-7319-00	670-7319-00
A6 Display Board	670-7320-00	670-7320-00	670-7320-00	670-7320-00
A7 Power Supply Board	670-7321-00	670-7321-00	670-7321-00	670-7321-00
A8 Memory Board	670-7322-00	670-7322-00	670-7322-00	670-7322-00
A9 MPU Board	670-7323-00	670-7323-00	670-7323-01	670-7323-01
A10 Trigger Board	670-7324-00	670-7324-00	670-7324-00	670-7324-00
A11 Timebase Board	670-7325-00	670-7325-00	670-7325-00	670-7325-00
A12 CH 1 Attenuator	119-1444-00	119-1444-00	119-1444-00	119-1444-00
A13 CH 2 Attenuator	119-1444-00	119-1444-00	119-1444-00	119-1444-00

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SIGNATURE ANALYSIS TABLES
FIRMWARE VERSION 1.00 & 1.03

FIRMWARE VERSION 1.00 & 1.03 CROSS REFERENCE

(Use in conjunction with Table 7-1
at the beginning of the Signature Analysis Tables).

Circuit Number	1.00 IC Part Number	1.03 IC Part Number
A9U200	160-1164-00	160-1164-02
A9U300	160-1165-00	160-1165-02
A9U400	160-1163-00	160-1163-02
A9U500	160-1162-00	160-1162-03
A9U600	160-1676-00	160-1676-02
A9U700	160-1757-00	160-1757-03

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7D20 SIGNATURE TABLE 1.0

Firmware Version: 1.00

Diagnostic Invoked: None (freerun)

For Testing: Address and Control

On Assembly: A9 MPU

Board Version: 670-7323-00

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-820	_	0001
Stop	TP-820	_	0001
Clock	TP-824	_	0003

Configuration:

MPU Board on extender

Remove P215 P720 P901 P902 P903 P904 P905 P906 P810 P811 P812

Test Position P900 P907

Jumper U110-5 to U110-14

+5 Volt Signature: 0003

Ground Signature: 0000

A9 U200		A9 U300		A9 U400		A9 U500		A9 U600	
pin 1	0003	pin 1	0003	pin 1	0003	pin 1	0003	pin 1	0003
pin 2	4FCA	pin 2	4FCA	pin 2	4FCA	pin 2	4FCA	pin 2	4FCA
pin 3	6F9A	pin 3	6F9A	pin 3	6F9A	pin 3	6F9A	pin 3	6F9A
pin 4	U759	pin 4	U759	pin 4	U759	pin 4	U759	pin 4	U759
pin 5	0356	pin 5	0356	pin 5	0356	pin 5	0356	pin 5	0356
pin 6	1U5P	pin 6	1U5P	pin 6	1U5P	pin 6	1U5P	pin 6	1U5P
pin 7	P763	pin 7	P763	pin 7	P763	pin 7	P763	pin 7	P763
pin 8	8484	pin 8	8484	pin 8	8484	pin 8	8484	pin 8	8484
pin 9	FFFF	pin 9	FFFF	pin 9	FFFF	pin 9	FFFF	pin 9	FFFF
pin 10	UUUU	pin 10	UUUU	pin 10	UUUU	pin 10	UUUU	pin 10	UUUU
pin 20	64HF	pin 20	29A4	pin 20	5FUA	pin 20	1183	pin 20	2302
pin 21	37C5	pin 21	37C5	pin 21	37C5	pin 21	37C5	pin 21	37C5
pin 22	0000	pin 22	0000	pin 22	0000	pin 22	0000	pin 22	6081
pin 23	6U28	pin 23	6U28	pin 23	6U28	pin 23	6U28	pin 23	6U28
pin 24	6321	pin 24	6321	pin 24	6321	pin 24	6321	pin 24	6321
pin 25	7791	pin 25	7791	pin 25	7791	pin 25	7791	pin 25	7791
pin 26	0003	pin 26	0003	pin 26	0003	pin 26	0003	pin 26	0003
pin 27	0003	pin 27	0003	pin 27	0003	pin 27	0003	pin 27	0003
pin 28	0003	pin 28	0003	pin 28	0003	pin 28	0003	pin 28	0003

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7D2Ø SIGNATURE TABLE 1.Ø

A9 U7ØØ		A9 U8ØØ		A9 U9ØØ		A9 U1ØØ		A9 U21Ø	
pin 1	ØØØ3	pin 1	6F9A	pin 1	6F9A	pin 1	UUUU	pin 1	FFFF
pin 2	4FCA	pin 2	U759	pin 2	U759	pin 2	FFFF	pin 2	8484
pin 3	6F9A	pin 3	Ø356	pin 3	Ø356	pin 3	8484	pin 3	P763
pin 4	U759	pin 4	1U5P	pin 4	1U5P	pin 4	P763	pin 8	ØØØØ
pin 5	Ø356	pin 5	P763	pin 5	P763	pin 5	1U5P	pin 14	HH69
pin 6	1U5P	pin 6	8484	pin 6	8484	pin 7	ØØØ3	pin 15	ØØØ3
pin 7	P763	pin 7	FFFF	pin 7	FFFF	pin 8	ØØØ3	pin 16	ØØØ3
pin 8	8484	pin 8	UUUU	pin 8	UUUU	pin 9	ØØØØ		
pin 9	FFFF	pin 12	ØØØØ	pin 12	ØØØØ	pin 1Ø	APC2		
pin 1Ø	UUUU	pin 18	47UA	pin 18	54H4	pin 11	APC2		
pin 2Ø	23Ø2	pin 19	37C5	pin 19	37C5	pin 13	7791		
pin 21	37C5	pin 2Ø	ØØØØ	pin 2Ø	ØØØØ	pin 14	6321		
pin 22	6Ø82	pin 21	ØØØ3	pin 21	ØØØ3	pin 15	6F9A		
pin 23	6U28	pin 22	6321	pin 22	6321	pin 16	U759		
pin 24	6321	pin 23	7791	pin 23	7791	pin 17	Ø356		
pin 25	7791	pin 24	ØØØ3	pin 24	ØØØ3	pin 18	ØØØ3		
pin 26	ØØØ3								
pin 27	ØØØ3								
pin 28	ØØØ3								

A9 U31Ø		A9 U315		A9 U41Ø		A9 U61Ø		A9 U71Ø	
pin 1	ØØØ3	pin 1	FFFF	pin 1	ØØØ3	pin 1	Ø356	pin 1	4868
pin 8	2246	pin 2	8484	pin 8	8F75	pin 2	U759	pin 2	9UP1
pin 9	ØØØ3	pin 3	P763			pin 3	6F9A	pin 3	ØØØ1
		pin 14	3FF4			pin 4	3Ø2P	pin 6	ØØØ3
		pin 15	ØØØ3			pin 5	7423	pin 7	1183
						pin 6	37C5	pin 8	ØØØØ
						pin 7	HH69	pin 9	64HF
						pin 8	ØØØØ	pin 1Ø	29A4
						pin 9	3FF4	pin 11	5FUA
						pin 1Ø	8F75	pin 12	23Ø2
						pin 11	2246	pin 13	F9CF
						pin 12	H3P5	pin 14	534H
						pin 13	8317	pin 15	C9U1
						pin 14	6Ø81	pin 16	ØØØ3
						pin 15	76C6		
						pin 16	ØØØ3		

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7D2Ø SIGNATURE TABLE 1.Ø

A9 U715		A9 U72Ø		A9 U725		A9 U81Ø		A9 U815	
pin	1 6U2C	pin	1 6Ø81	pin	2 ØØØØ	pin	1 C9U1	pin	1 ØØØ3
pin	2 4FCA	pin	2 6Ø81	pin	3 ØØØ3	pin	2 534H	pin	2 ØØØØ
pin	3 4868	pin	3 6Ø82	pin	4 6U2C	pin	3 PACF	pin	3 APC2
pin	5 ØØØ1	pin	4 6Ø82	pin	5 ØØØØ	pin	4 ØØØ3	pin	4 7423
pin	6 9UP1	pin	5 8317	pin	6 6U28	pin	5 ØØØ3	pin	5 PACU
pin	7 FØ77	pin	6 6Ø81	pin	7 ØØØØ	pin	6 ØØØØ	pin	6 3Ø2H
pin	8 ØØØØ	pin	7 ØØØØ	pin	8 7H7C	pin	7 ØØØØ	pin	7 ØØØØ
pin	9 Ø4HU	pin	8 ØØØ3	pin	9 PACF	pin	8 PACU	pin	8 3Ø2P
pin	1Ø 4P23	pin	9 ØØØØ	pin	1Ø 97F4	pin	9 PACF	pin	9 ØØØ3
pin	11 A98A	pin	1Ø ØØØ3	pin	11 7423	pin	1Ø ØØØ3	pin	1Ø ØØØ3
pin	12 47UA	pin	11 ØØØØ	pin	12 37C5	pin	11 ØØØ3	pin	11 3Ø2H
pin	13 54H4	pin	12 ØØØ3	pin	13 7H7C	pin	12 ØØØØ	pin	12 ØØØ3
pin	14 7423	pin	13 ØØØ3	pin	14 ØØØ3	pin	13 ØØØØ	pin	13 ØØØ3
pin	15 APC2	pin	14 ØØØ3			pin	14 ØØØ3	pin	14 ØØØ3
pin	16 ØØØ3								

A9 U825		A9 U91Ø		A9 U915		A9 U925		A9 U1Ø1Ø	
pin	1 ØØØØ	pin	1 ØØØØ	pin	1 ØØØ3	pin	1 ØØØ3	pin	1 7791
pin	2 3Ø2H	pin	2 ØØØ3	pin	3 Ø356	pin	3 4868	pin	2 6321
pin	3 ØØØ3	pin	3 ØØØ3	pin	4 6F9A	pin	7 6321	pin	3 37C5
pin	4 ØØØ3	pin	4 ØØØ3	pin	7 P763	pin	8 6U28	pin	4 7423
pin	5 ØØØØ	pin	8 UUUU	pin	8 UUUU	pin	1Ø ØØØØ	pin	5 3Ø2P
pin	8 ØØØØ	pin	9 FFFF	pin	1Ø ØØØØ	pin	11 3Ø2H	pin	6 ØØØ3
pin	9 ØØØØ	pin	1Ø 8484	pin	11 3Ø2H	pin	13 37C5	pin	7 95AØ
pin	1Ø 3Ø2H	pin	11 P763	pin	13 8484	pin	14 7791	pin	8 ØØØØ
pin	11 ØØØ3	pin	12 1U5P	pin	14 U759	pin	17 ØØØØ	pin	9 9C6A
pin	12 ØØØ3	pin	13 Ø356	pin	17 FFFF	pin	18 4FCA	pin	1Ø FU07
pin	13 ØØØØ	pin	14 U759	pin	18 1U5P	pin	2Ø ØØØ3	pin	11 F896
pin	16 ØØØ3	pin	15 6F9A	pin	2Ø ØØØ3			pin	12 H996
		pin	16 7791					pin	13 3205
		pin	17 6321					pin	14 72P9
		pin	18 37C5					pin	15 P4Ø1
		pin	19 6U28					pin	16 ØØØ3
		pin	2Ø 4FCA						
		pin	21 4868						
		pin	22 9UP1						
		pin	23 ØØØ1						
		pin	32 ØØØ3						

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7D20 SIGNATURE TABLE 1.1

Firmware Version: 1.00

Diagnostic Invoked: None (freerun)

For Testing: U400 data

On Assembly: A9 MPU

Board Version: 670-7323-00

Signature Analyzer Setup:

	connect	edge	signature
Start	U400-20	_	0000
Stop	U710-11	_/	0000
Clock	TP-824	_	1180

Configuration:

MPU Board on extender

Remove P215 P720 P901 P902 P903 P904 P905 P906 P810 P811 P812

Test Position P900 P907

+5 Volt Signature: 1180

Ground Signature: 0000

A9 U400
pin 11 7F1U
pin 12 F205
pin 13 045A
pin 15 2895
pin 16 U2C7
pin 17 0808
pin 18 U01C
pin 19 33H0

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7D2Ø SIGNATURE TABLE 1.2

Firmware Version: 1.ØØ

Diagnostic Invoked: None (freerun)

For Testing: U3ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	U3ØØ-2Ø	_	ØØØØ
Stop	U71Ø-1Ø	_/	ØØØØ
Clock	TP-824	_	118Ø

Configuration:

MPU Board on extender

Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812

Test Position P9ØØ P9Ø7

+5 Volt Signature: 118Ø

Ground Signature: ØØØØ

A9 U3ØØ
pin 11 2U19
pin 12 2U28
pin 13 2FP4
pin 15 55PØ
pin 16 2C81
pin 17 82Ø9
pin 18 1PA9
pin 19 376C

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7D20 SIGNATURE TABLE 1.3

Firmware Version: 1.00

Diagnostic Invoked: None (freerun)

For Testing: U200 data

On Assembly: A9 MPU

Board Version: 670-7323-00

Signature Analyzer Setup:

	connect	edge	signature
Start	U200-20	_	0000
Stop	U710-9	_/	0000
Clock	TP-824	_	1180

Configuration:

MPU Board on extender

Remove P215 P720 P901 P902 P903 P904 P905 P906 P810 P811 P812

Test Position P900 P907

+5 Volt Signature: 1180

Ground Signature: 0000

A9 U200
pin 11 6PU0
pin 12 PF42
pin 13 14U1
pin 15 H68P
pin 16 5158
pin 17 C514
pin 18 HPC4
pin 19 7298

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7D2Ø SIGNATURE TABLE 1.4

Firmware Version: 1.00, 1.03

Diagnostic Invoked: None (freerun)

Signature Analyzer Setup:

For Testing: U5ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

	connect	edge	signature
Start	U5ØØ-2Ø	_	ØØØØ
Stop	U71Ø-7	_/	ØØØØ
Clock	TP-824	_	118Ø

Configuration:

MPU Board on extender

Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812

Test Position P9ØØ P9Ø7

+5 Volt Signature: 118Ø

Ground Signature: ØØØØ

1.00	1.03
A9 U500	A9 U500
pin 11 HH1F pin 12 0F41 pin 13 133U pin 15 1F1P pin 16 C829 pin 17 FPF8 pin 18 020C pin 19 A112	pin 11 7FF0 pin 12 0U55 pin 13 067H pin 15 542C pin 16 F355 pin 17 H3AF pin 18 FA7P pin 19 4CC6

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7D20 SIGNATURE TABLE 1.5

Firmware Version: 1.00, 1.03

Diagnostic Invoked: None (freerun)

For Testing: U700 data

On Assembly: A9 MPU

Board Version: 670-7323-00, 03

Signature Analyzer Setup:

	connect	edge	signature
Start	U700-20	_	0000
Stop	U710-12	_/	0000
Clock	TP-824	_	1180

Configuration:

MPU Board on extender

Remove P215 P720 P901 P902 P903 P904 P905 P906 P810 P811 P812

Test Position P900 P907

Jumper U720-1 to U720-14

+5 Volt Signature: 1180

Ground Signature: 0000

1.00	1.03
A9 U500	A9 U500
pin 11 FC59 pin 12 FH65 pin 13 P21A pin 15 PA67 pin 16 9HFP pin 17 6P9F pin 18 C83C pin 19 70A6	pin 11 3A1H pin 12 9HF7 pin 13 F2A9 pin 15 PC8A pin 16 7CA9 pin 17 APC8 pin 18 A5H3 pin 19 4AHC

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7D2Ø SIGNATURE TABLE 1.6

Firmware Version: 1.ØØ

Diagnostic Invoked: None (freerun)

For Testing: U6ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	U6ØØ-2Ø	_	ØØØØ
Stop	U71Ø-12	_/	ØØØØ
Clock	TP-824	_	118Ø

Configuration:

MPU Board on extender

Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812

Test Position P9ØØ P9Ø7

Jumper U72Ø-5 to U72Ø-14

+5 Volt Signature: 118Ø

Ground Signature: ØØØØ

A9 U6ØØ
pin 11 PA84
pin 12 P29Ø
pin 13 5P23
pin 15 9115
pin 16 3CFH
pin 17 A256
pin 18 33H8
pin 19 C6CØ

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7D20 SIGNATURE TABLE 2.0

Firmware Version: 1.00

Diagnostic Invoked: External Bus Exerciser

For Testing: External Bus (data, address)

On Assembly: A9 MPU, A2 LED, A1 Switch

Board Version: 670-7323-00
670-7316-00
670-7315-00

Configuration:
MPU Board on extender
Frontpanel connected by cabling only
Remove P215 P510

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-900*	_/	FU6C
Stop	TP-901*	_	FU6C
Clock	TP-902*	_/	0000

* on A9 MPU

+5 Volt Signature: FU6C
Ground Signature: 0000

A9 U915		A9 U925		A9 U1000		A9 U1010		A2 U100	
pin 1	0000	pin 1	0000	pin 1	FU14	pin 1	809P	pin 1	CH33
pin 2	02H0	pin 2	AA25	pin 2	F7U2	pin 2	3HHA	pin 2	FU6C
pin 3	02H0	pin 3	AA25	pin 3	CH33	pin 3	795U	pin 7	0000
pin 4	2C65	pin 6	3HHA	pin 4	5735	pin 4	FFC6	pin 8	F22P
pin 5	2C65	pin 7	3HHA	pin 5	UU2F	pin 5	0000	pin 9	FU6C
pin 6	496P	pin 8	5AU6	pin 6	U607	pin 6	FU6C	pin 14	FU6C
pin 7	496P	pin 9	5AU6	pin 7	0304	pin 7	FU6C		
pin 8	A293	pin 10	0000	pin 8	H708	pin 8	0000		
pin 9	A293	pin 11	FU6C	pin 9	873A	pin 9	FU6C		
pin 10	0000	pin 12	795U	pin 10	0000	pin 10	FU6C		
pin 11	FU6C	pin 13	795U	pin 11	873A	pin 11	P7C5		
pin 12	0419	pin 14	809P	pin 12	H708	pin 12	43AC		
pin 13	0419	pin 15	809P	pin 13	0304	pin 13	3253		
pin 14	U70H	pin 16	FU14	pin 14	U607	pin 14	FU6C		
pin 15	U70H	pin 17	FU14	pin 15	UU2F	pin 15	9590		
pin 16	9P24	pin 18	PCUA	pin 16	5735	pin 16	FU6C		
pin 17	9P24	pin 19	PCUA	pin 17	CH33				
pin 18	P38F	pin 20	FU6C	pin 18	F7U2				
pin 19	P38F			pin 19	28HP				
pin 20	FU6C			pin 20	FU6C				

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A2 U110	A2 U120	A2 U130	A2 U140	A2 U310
pin 1 Ø3Ø4	pin 1 5735	pin 1 H7Ø8	pin 1 F7U2	pin 1 UU2F
pin 2 FU6C	pin 2 FU6C	pin 2 FU6C	pin 2 FU6C	pin 2 FU6C
pin 7 ØØØØ	pin 7 ØØØØ	pin 7 ØØØØ	pin 7 ØØØØ	pin 7 ØØØØ
pin 8 F22P	pin 8 F22P	pin 8 F22P	pin 8 F22P	pin 8 F22P
pin 9 FU6C	pin 9 FU6C	pin 9 FU6C	pin 9 FU6C	pin 9 FU6C
pin 14 FU6C	pin 14 FU6C	pin 14 FU6C	pin 14 FU6C	pin 14 FU6C

A2 U335	A2 U43Ø	A2 U5ØØ	A2 U72Ø	A1 U31Ø
pin 1 FU6C	pin 1 FU14	pin 1 U6Ø7	pin 2 FU6C	pin 1 496P
pin 2 43AC	pin 2 CH33	pin 2 FU6C	pin 3 43AC	pin 4 5735
pin 3 FU14	pin 3 U6Ø7	pin 7 ØØØØ	pin 4 96ØU	pin 6 ØØØØ
pin 4 1AFU	pin 4 Ø3Ø4	pin 8 F22P	pin 5 96ØU	pin 7 H7Ø8
pin 5 96ØU	pin 5 5735	pin 9 FU6C	pin 6 A293	pin 8 ØØØØ
pin 6 FU6C	pin 6 H7Ø8	pin 14 FU6C	pin 7 9P24	pin 9 UU2F
pin 7 FU6C	pin 7 873A		pin 8 Ø419	pin 1Ø ØØØØ
pin 8 ØØØØ	pin 8 UU2F		pin 9 FU6C	pin 12 873A
pin 9 FU6C	pin 9 F7U2		pin 19 3U69	pin 13 ØØØØ
pin 1Ø FU14	pin 1Ø ØØØØ		pin 2Ø ØØØØ	pin 15 FU6C
pin 11 3U69	pin 19 43AC		pin 4Ø FU6C	pin 16 FU6C
pin 12 F22P	pin 2Ø FU6C			
pin 13 P38F				
pin 14 ØØØØ				
pin 15 3253				
pin 16 FU6C				

A1 U32Ø	A1 U33Ø	A1 U42Ø
pin 1 Ø419	pin 1 FU14	pin 1 496P
pin 2 FU14	pin 2 FU6C	pin 4 F7U2
pin 3 9P24	pin 3 5735	pin 7 U6Ø7
pin 4 ØØØØ	pin 4 FU6C	pin 8 ØØØØ
pin 5 ØØØØ	pin 5 873A	pin 9 CH33
pin 6 ØØØØ	pin 6 FU6C	pin 12 Ø3Ø4
pin 7 ØØØØ	pin 7 CH33	pin 15 FU6C
pin 8 ØØØØ	pin 8 FU6C	pin 16 FU6C
pin 9 ØØØØ	pin 9 U6Ø7	
pin 1Ø ØØØØ	pin 1Ø ØØØØ	
pin 11 ØØØØ	pin 11 F7U2	
pin 12 ØØØØ	pin 12 FU6C	
pin 13 A293	pin 13 UU2F	
pin 14 FU14	pin 14 FU6C	
pin 15 Ø419	pin 15 H7Ø8	
pin 16 FU6C	pin 16 FU6C	
	pin 17 Ø3Ø4	
	pin 18 FU6C	
	pin 19 FU14	
	pin 2Ø FU6C	

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7D2Ø SIGNATURE TABLE 3.Ø

Firmware Version: 1.ØØ

Diagnostic Invoked: Circuit
Exerciser 432

For Testing: Address Bus &
Last Address Latch

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	7ACC
Stop	TP-9Ø1*	_	7ACC
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 7ACC
Ground Signature: ØØØØ

A8 U2ØØ	A8 U42Ø	A8 U112Ø	A8 U122Ø	A8 U131Ø
pin 1 9616	pin 1 P532	pin 1 ØØØØ	pin 1 7CHC	pin 2 U887
pin 1Ø ØØØØ	pin 2 8C17	pin 8 ØØØØ	pin 2 7UAA	pin 3 5634
pin 2Ø 7ACC	pin 3 9616	pin 9 7ACC	pin 3 71CC	pin 5 P532
	pin 4 U887	pin 11 7ACC	pin 4 7ACC	pin 6 PHA2
	pin 5 1PCF	pin 14 C9C1	pin 5 7ACC	pin 8 ØØØØ
	pin 6 7ACC	pin 16 7ACC	pin 6 C9C1	pin 1Ø H9H9
	pin 7 7ACC		pin 7 ØØØØ	pin 11 8C17
	pin 8 ØØØØ		pin 8 ØØØØ	pin 14 7ACC
	pin 9 7ACC		pin 11 ØØØØ	pin 16 7ACC
	pin 1Ø U211		pin 13 PF7A	
	pin 11 7ACC		pin 14 U211	
	pin 12 7ACC		pin 15 7ACC	
	pin 13 7ACC		pin 16 7ACC	
	pin 14 7ACC			
	pin 15 9616			
	pin 16 7ACC			

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A8 U141Ø	
pin 2	7CHC
pin 3	CH82
pin 5	7UAA
pin 6	2FH6
pin 8	ØØØØ
pin 1Ø	7A75
pin 11	71CC
pin 13	UU96
pin 14	F83A
pin 16	7ACC

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7D2Ø SIGNATURE TABLE 3.1

Firmware Version: 1.ØØ

Diagnostic Invoked: Circuit
Exerciser 432

For Testing: Memory Address Bus
Memory Data Bus

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	3395
Stop	TP-9Ø1*	_	3395
Clock	U112Ø-6	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 3395
Ground Signature: ØØØØ

A8 U2ØØ	A8 U21Ø	A8 U31Ø	A8 U41Ø	A8 U51Ø
pin 3 1H8	pin 2 Ø3PP	pin 2 U27A	pin 2 342A	pin 2 2H6A
pin 4 7832	pin 3 22P6	pin 3 22P6	pin 3 22P6	pin 3 22P6
pin 7 36CC	pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ
pin 8 89P3	pin 5 89P3	pin 5 89P3	pin 5 89P3	pin 5 89P3
pin 11 ØØØØ	pin 6 7832	pin 6 7832	pin 6 7832	pin 6 7832
pin 13 617F	pin 7 1H8	pin 7 1H8	pin 7 1H8	pin 7 1H8
pin 14 272U	pin 9 3395	pin 9 3395	pin 9 3395	pin 9 3395
pin 17 C2HP	pin 1Ø 36CC	pin 1Ø 36CC	pin 1Ø 36CC	pin 1Ø 36CC
pin 18 22P6	pin 11 272U	pin 11 272U	pin 11 272U	pin 11 272U
	pin 12 617F	pin 12 617F	pin 12 617F	pin 12 617F
	pin 13 C2HP	pin 13 C2HP	pin 13 C2HP	pin 13 C2HP
	pin 16 ØØØØ	pin 16 ØØØØ	pin 16 ØØØØ	pin 16 ØØØØ

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A8 U61Ø	A8 U71Ø	A8 U81Ø	A8 U91Ø	A8 U8ØØ
pin 2 4868	pin 2 HF62	pin 2 8F49	pin 2 FFP5	pin 6 C2HP
pin 3 22P6	pin 3 22P6	pin 3 22P6	pin 3 22P6	pin 7 36CC
pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ	pin 9 272U
pin 5 89P3	pin 5 89P3	pin 5 89P3	pin 5 89P3	pin 1Ø 617F
pin 6 7832	pin 6 7832	pin 6 7832	pin 6 7832	
pin 7 1HØ8	pin 7 1HØ8	pin 7 1HØ8	pin 7 1HØ8	
pin 9 3395	pin 9 3395	pin 9 3395	pin 9 3395	
pin 1Ø 36CC	pin 1Ø 36CC	pin 1Ø 36CC	pin 1Ø 36CC	
pin 11 272U	pin 11 272U	pin 11 272U	pin 11 272U	
pin 12 617F	pin 12 617F	pin 12 617F	pin 12 617F	
pin 13 C2HP	pin 13 C2HP	pin 13 C2HP	pin 13 C2HP	
pin 16 ØØØØ	pin 16 ØØØØ	pin 16 ØØØØ	pin 16 ØØØØ	

A8 U1Ø1Ø	A8 U111Ø	A8 U121Ø	A8 U131Ø	A8 U141Ø
pin 4 89P3	pin 4 272U	pin 4 89P3	pin 4 272U	pin 4 89P3
pin 7 1HØ8	pin 7 36CC	pin 7 1HØ8	pin 7 36CC	pin 7 1HØ8
pin 9 7832	pin 9 C2HP	pin 9 7832	pin 9 C2HP	pin 9 7832
pin 12 22P6	pin 12 22P6	pin 12 617F	pin 12 22P6	pin 12 617F

A8 U16ØØ	A8 U17ØØ
pin 4 FFP5	pin 4 2H6A
pin 7 8F49	pin 7 342A
pin 9 HF62	pin 9 U27A
pin 12 4868	pin 12 Ø3PP

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7D2Ø SIGNATURE TABLE 3.2

Firmware Version: 1.ØØ

Diagnostic Invoked: Circuit Exerciser 432

For Testing: Data Bus

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	3395
Stop	TP-9Ø1*	_	3395
Clock	J41Ø-21B	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 3395
Ground Signature: ØØØØ

A8 U5ØØ	A8 U6ØØ	A8 U7ØØ	A8 U9ØØ	A8 U1ØØØ
pin 1 8F49	pin 1 342A	pin 1 8F49	pin 1 3395	pin 1 U27A
pin 15 FFP5	pin 9 Ø3PP	pin 9 4868	pin 9 FFP5	pin 9 ØØØØ
	pin 1Ø U27A	pin 1Ø HF62	pin 1Ø 3395	pin 1Ø Ø3PP
	pin 15 2H6A	pin 15 FFP5	pin 15 3395	pin 15 342A

A8 U11ØØ	A8 U8ØØ	A8 U16ØØ	A8 U17ØØ	A8 U2ØØ
pin 1 HF62	pin 1 8F49	pin 3 FFP5	pin 3 2H6A	pin 2 8F49
pin 9 2H6A	pin 2 HF62	pin 6 8F49	pin 6 342A	pin 5 HF62
pin 1Ø 4868	pin 3 4868	pin 1Ø HF62	pin 1Ø U27A	pin 6 342A
pin 15 8F49	pin 15 FFP5	pin 13 4868	pin 13 Ø3PP	pin 9 FFP5
				pin 12 4868
				pin 15 2H6A
				pin 16 U27A
				pin 19 Ø3PP

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7D20 SIGNATURE TABLE 3.2

A8 U300		A8 U400	
pin	2 8F49	pin	2 8F49
pin	5 HF62	pin	5 HF62
pin	6 342A	pin	6 342A
pin	9 FFP5	pin	9 FFP5
pin	12 4868	pin	12 4868
pin	15 2H6A	pin	15 2H6A
pin	16 U27A	pin	16 U27A
pin	19 Ø3PP	pin	19 Ø3PP

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7D2Ø SIGNATURE TABLE 4.Ø

Firmware Version: 1.ØØ

Diagnostic Invoked: Circuit
Exerciser 4321

For Testing: Display Address
Generator

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	6PCP
Stop	TP-9Ø1*	_	6PCP
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 6PCP
Ground Signature: ØØØØ

A8 U5ØØ	A8 U6ØØ	A8 U7ØØ	A8 U42Ø	A8 U62Ø
pin 2 1UFP	pin 2 3H46	pin 2 ØP45	pin 1 HCPH	pin 1 C679
pin 3 H32C	pin 3 H8U8	pin 3 1C84	pin 2 H98U	pin 2 6UH8
pin 4 6PCP	pin 4 6PCP	pin 4 6PCP	pin 3 Ø3Ø4	pin 3 6U05
pin 5 ØØØØ	pin 5 ØØØØ	pin 5 ØØØØ	pin 4 ØØØØ	pin 7 ØØØØ
pin 8 ØØØØ	pin 6 6589	pin 6 C5UØ	pin 5 H98U	pin 14 6PCP
pin 11 6U05	pin 7 98C3	pin 7 1C55	pin 6 6PCP	
pin 13 6PCP	pin 8 ØØØØ	pin 8 ØØØØ	pin 7 6PCP	
pin 14 ØØØØ	pin 11 6UH8	pin 11 6UH8	pin 8 ØØØØ	
pin 16 6PCP	pin 12 ØØØØ	pin 12 ØØØØ	pin 9 6PCP	
	pin 13 6PCP	pin 13 6PCP	pin 1Ø C553	
	pin 14 ØØØØ	pin 14 ØØØØ	pin 11 6UH8	
	pin 16 6PCP	pin 16 6PCP	pin 12 6PCP	
			pin 13 6PCP	
			pin 14 6PCP	
			pin 15 Ø3Ø4	
			pin 16 6PCP	

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A8 U920		A8 U1010		A8 U1110		A8 U1210		A8 U1220	
pin	4 6PCP	pin	2 98C3	pin	2 H8U8	pin	2 1C84	pin	1 C679
pin	5 6PCP	pin	5 H32C	pin	5 3H46	pin	5 0P45	pin	2 6H9F
pin	6 0000	pin	11 1UFP	pin	11 6589	pin	11 C5U0	pin	3 H98U
pin	7 0000					pin	14 1C55	pin	4 6PCP
pin	8 6PCP							pin	5 0000
pin	10 0000							pin	6 4A0P
pin	14 6PCP							pin	7 6PCP
								pin	8 0000
								pin	9 0000
								pin	12 0000
								pin	13 CC1C
								pin	14 C553
								pin	15 6PCP
								pin	16 6PCP

A8 U1320	
pin	4 6PCP
pin	5 0000
pin	6 0000
pin	7 0000
pin	14 6PCP

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7D2Ø SIGNATURE TABLE 5.Ø

Firmware Version: 1.ØØ

Diagnostic Invoked: Circuit Exerciser 64

For Testing: Acquire Address Generator

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	6F6P
Stop	TP-9Ø1*	_	6F6P
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 6F6P
Ground Signature: ØØØØ

A8 U42Ø	A8 U122Ø	A8 U9ØØ	A8 U1ØØØ	A8 U11ØØ
pin 1 1F46	pin 1 U43H	pin 1 6F6P	pin 2 491P	pin 2 P16C
pin 2 6884	pin 2 53PC	pin 2 98A7	pin 3 66FU	pin 3 H9ØA
pin 3 C891	pin 3 3F7Ø	pin 3 98A7	pin 4 AA2A	pin 4 U4F9
pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ	pin 5 ØØØØ	pin 5 ØØØØ
pin 5 3F7Ø	pin 5 6F6P	pin 5 ØØØØ	pin 6 7F47	pin 6 8P1A
pin 6 6F6P	pin 6 2U4H	pin 6 98A7	pin 7 ØØØØ	pin 7 55P9
pin 7 6F6P	pin 7 6F6P	pin 7 99P4	pin 8 ØØØØ	pin 8 ØØØØ
pin 8 ØØØØ	pin 8 ØØØØ	pin 8 ØØØØ	pin 11 U4F9	pin 11 U4F9
pin 9 U4F9	pin 1Ø ØØØØ	pin 1Ø 6F6P	pin 13 6F6P	pin 13 AA2A
pin 1Ø 7Ø28	pin 13 HUPA	pin 11 U4F9	pin 14 FF53	pin 14 FF53
pin 11 6F6P	pin 14 7Ø28	pin 13 U4F9	pin 16 6F6P	pin 16 6F6P
pin 12 6F6P	pin 15 6F6P	pin 14 FF53		
pin 13 AØ3H	pin 16 6F6P	pin 15 6F6P		
pin 14 6F6P		pin 16 6F6P		
pin 15 74F2				
pin 16 6F6P				

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A8 U1Ø1Ø		A8 U1Ø2Ø		A8 U111Ø		A8 U121Ø	
pin 3	55P9	pin 1	AØ3H	pin 3	H9ØA	pin 3	98A7
pin 6	66FU	pin 2	6F6P	pin 6	P16C	pin 6	98A7
pin 8	ØØØØ	pin 5	ØØØØ	pin 8	ØØØØ	pin 8	ØØØØ
pin 1Ø	491P	pin 6	6F6P	pin 1Ø	8P1A	pin 1Ø	98A7
pin 14	ØØØØ	pin 7	ØØØØ	pin 16	6F6P	pin 13	99P4
pin 16	6F6P	pin 12	FF53			pin 16	6F6P
		pin 13	6F6P				
		pin 14	6F6P				

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7D20 SIGNATURE TABLE 6.0

Firmware Version: 1.00

Diagnostic Invoked: Circuit
Exerciser 6321

For Testing: Time Base
Data Registers

On Assembly: A11 Time Base

Board Version: 670-7325-00

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-900*	_/	3H18
Stop	TP-901*	_	3H18
Clock	TP-902*	_/	0000

* on A9 MPU Board

+5 Volt Signature: 3H18
Ground Signature: 0000

A11 U110	A11 U1210	A11 U1310	A11 U1320	A11 U1410
pin 8 0000	pin 1 H130	pin 1 CU0U	pin 1 H130	pin 1 55F3
pin 15 ACF1	pin 2 ACF1	pin 2 C018	pin 2 ACF1	pin 2 68HC
pin 16 3H18	pin 8 0000	pin 3 ACF1	pin 8 0000	pin 3 4C40
	pin 15 0000	pin 4 H5U5	pin 10 4186	pin 4 7658
	pin 16 3H18	pin 5 F16A	pin 15 0000	pin 5 5UHU
		pin 6 HUP9	pin 16 3H18	pin 6 62F7
		pin 7 FC76		pin 7 0000
		pin 8 0000		pin 8 HUP9
		pin 9 4186		pin 9 P2U1
		pin 11 5UHU		pin 10 7F44
		pin 12 4C40		pin 11 415F
		pin 13 55F3		pin 12 415F
		pin 14 415F		pin 13 7F44
		pin 15 3H18		pin 14 3H18
		pin 16 3H18		

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7D2Ø SIGNATURE TABLE 6.Ø

A11 U151Ø		A11 U161Ø		A11 U171Ø		A11 U13ØØ		A11 U14ØØ	
pin	1 CUØU	pin	1 CUØU	pin	1 CUØU	pin	3 H8C8	pin	3 2987
pin	2 59P5	pin	2 FCF3	pin	2 3494	pin	4 5519	pin	4 4C4Ø
pin	3 ACF1	pin	3 ACF1	pin	3 ACF1	pin	7 ØØØØ	pin	7 ØØØØ
pin	4 P8PH	pin	4 H5U5	pin	4 P8PH	pin	1Ø 19H2	pin	1Ø P8PH
pin	5 2987	pin	5 UF72	pin	5 149U	pin	11 ØØØØ	pin	11 9473
pin	6 9473	pin	6 FC76	pin	6 5519	pin	14 3H18	pin	14 3H18
pin	7 5519	pin	7 P2U1	pin	7 A96C				
pin	8 ØØØØ	pin	8 ØØØØ	pin	8 ØØØØ				
pin	9 CØ18	pin	9 59P5	pin	9 FCF3				
pin	11 A426	pin	11 55F3	pin	11 H8C8				
pin	12 654F	pin	12 7F44	pin	12 24FA				
pin	13 H8C8	pin	13 4C4Ø	pin	13 654F				
pin	14 19H2	pin	14 62F7	pin	14 993P				
pin	15 3H18	pin	15 3H18	pin	15 3H18				
pin	16 3H18	pin	16 3H18	pin	16 3H18				

A11 U15ØØ		A11 U16ØØ		A11 U17ØØ	
pin	3 FC76	pin	3 24FA	pin	3 5519
pin	4 H5U5	pin	4 993P	pin	4 P8PH
pin	7 ØØØØ	pin	7 ØØØØ	pin	7 ØØØØ
pin	1Ø UF72	pin	1Ø 654F	pin	1Ø 149U
pin	11 62F7	pin	11 H8C8	pin	11 A96C
pin	14 3H18	pin	14 3H18	pin	14 3H18

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7D2Ø SIGNATURE TABLE 7.Ø

Firmware Version: 1.ØØ

Diagnostic Invoked: Circuit Exerciser 641

For Testing: INS, SO, EOA (flip-flops)

On Assembly: A11 Time Base

Board Version: 67Ø-7325-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	99FA
Stop	TP-9Ø1*	_	99FA
Clock	U132Ø-1	_/	ØØØØ

* on A9 MPU Board

+5 Volt Signature: 99FA
Ground Signature: ØØØØ

A11 U31Ø	A11 U41Ø	A11 U71Ø	A11 U91Ø	A11 U1Ø1Ø
pin 7 ØØØØ	pin 7 ØØØØ	pin 7 ØØØØ	pin 2 ØØØØ	pin 1 Ø7U3
pin 11 3172	pin 8 99FA	pin 8 A5UA	pin 3 Ø43H	pin 2 3172
pin 12 Ø7U3	pin 9 ØØØØ	pin 9 99FA	pin 4 6Ø4A	pin 3 Ø43H
pin 13 AC76	pin 1Ø 99FA	pin 1Ø 3F3Ø	pin 5 A892	pin 7 ØØØØ
pin 14 99FA	pin 14 99FA	pin 14 99FA	pin 6 3158	pin 11 A5UA
			pin 7 A97C	pin 12 A5UA
			pin 8 ØØØØ	pin 13 A5UA
			pin 9 32CF	pin 14 99FA
			pin 1Ø 9P39	
			pin 11 3172	
			pin 12 ØØØØ	
			pin 14 A5UA	
			pin 15 A5UA	
			pin 16 99FA	

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7D2Ø SIGNATURE TABLE 8.Ø

Firmware Version: 1.ØØ

Diagnostic Invoked: Circuit Exerciser 6431

For Testing: Preamplifier Data Registers

On Assembly: A4 Preamplifier

Board Version: 67Ø-7318-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	3H18
Stop	TP-9Ø1*	_	3H18
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

+5 Volt Signature: 3H18
Ground Signature: ØØØØ

A4 U3ØØ	A4 U123Ø	A4 U34Ø	A4 U91Ø	A4 U93Ø
pin 1 CUØU	pin 1 CUØU	pin 9 H8C8	pin 3 F16A	pin 3 FC76
pin 2 46A2	pin 2 3494	pin 1Ø A426	pin 5 H5U5	pin 5 HUP9
pin 3 8HF9	pin 3 8HF9	pin 11 5854		
pin 4 P8PH	pin 4 H5U5			
pin 5 149U	pin 5 F16A			
pin 6 68Ø1	pin 6 HUP9			
pin 7 9473	pin 7 FC76			
pin 8 ØØØØ	pin 8 ØØØØ			
pin 9 8C29	pin 9 46A2			
pin 11 24FA	pin 11 5UHU			
pin 12 H8C8	pin 12 4C4Ø			
pin 13 A426	pin 13 55F3			
pin 14 5854	pin 14 415F			
pin 15 3H18	pin 15 3H18			
pin 16 3H18	pin 16 3H18			

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7D2Ø SIGNATURE TABLE 9.Ø

Firmware Version: 1.ØØ

Diagnostic Invoked: Circuit Exerciser 6431

For Testing: Trigger Data Registers

On Assembly: A1Ø Trigger

Board Version: 67Ø-7324-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	3H18
Stop	TP-9Ø1*	_	3H18
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:
Trigger Board on extender

+5 Volt Signature: 3H18
Ground Signature: ØØØØ

A1Ø U1Ø1	A1Ø U2ØØ	A1Ø U2Ø1	A1Ø U21Ø	A1Ø U3ØØ
pin 4 HCP7	pin 1 CU ØU	pin 1 CU ØU	pin 1 CU ØU	pin 6 A96C
pin 5 F13A	pin 2 3944	pin 2 32C4	pin 2 3494	pin 8 ØØØØ
pin 7 ØØØØ	pin 3 P6UU	pin 3 P6UU	pin 3 P6UU	pin 9 ØØØØ
pin 8 993P	pin 4 H5U5	pin 4 P8PH	pin 4 H5U5	pin 1Ø 68Ø1
pin 9 3H18	pin 5 F16A	pin 5 2987	pin 5 UF72	pin 11 P5AØ
pin 1Ø A426	pin 6 P2U1	pin 6 A96C	pin 6 U66P	pin 15 ØØØØ
pin 11 HCP7	pin 7 U66P	pin 7 68Ø1	pin 7 HUP9	pin 16 3H18
pin 12 3H18	pin 8 ØØØØ	pin 8 ØØØØ	pin 8 ØØØØ	
pin 13 P6UU	pin 9 F13A	pin 9 3944	pin 9 32C4	
pin 14 3H18	pin 11 4C4Ø	pin 1Ø P1AU	pin 11 7F44	
	pin 12 5UHU	pin 11 654F	pin 12 55F3	
	pin 13 7F44	pin 12 A426	pin 13 5UHU	
	pin 14 68HC	pin 13 24FA	pin 14 7658	
	pin 15 3H18	pin 14 P5AØ	pin 15 3H18	
	pin 16 3H18	pin 15 3H18	pin 16 3H18	
		pin 16 3H18		

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A1Ø U31Ø	
pin 5	7F44
pin 6	55F3
pin 7	5UHU
pin 8	7658
pin 9	HUP9
pin 1Ø	U66P
pin 11	UF72
pin 12	H5U5

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SIGNATURE ANALYSIS TABLES
FIRMWARE VERSION 1.01

FIRMWARE VERSION 1.01 CROSS REFERENCE
(Use in conjunction with Table 7-1
at the beginning of the Signature Analysis Tables).

Circuit Number	IC Part Number
A9U200	160-1164-01
A9U300	160-1165-01
A9U400	160-1163-01
A9U500	160-1162-01
A9U600	160-1676-01
A9U700	160-1757-01

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7D2Ø SIGNATURE TABLE 1.Ø

Firmware Version: 1.Ø1

Diagnostic Invoked: None (freerun)

For Testing: Address and Control

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Configuration:
MPU Board on extender
Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812
Test Position P9ØØ P9Ø7
Jumper U11Ø-5 to U11Ø-14

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-82Ø	_	ØØØ1
Stop	TP-82Ø	_	ØØØ1
Clock	TP-824	_	ØØØ3

+5 Volt Signature: ØØØ3
Ground Signature: ØØØØ

A9 U2ØØ	A9 U3ØØ	A9 U4ØØ	A9 U5ØØ	A9 U6ØØ
pin 1 ØØØ3	pin 1 ØØØ3	pin 1 ØØØ3	pin 1 ØØØ3	pin 1 ØØØ3
pin 2 4FCA	pin 2 4FCA	pin 2 4FCA	pin 2 4FCA	pin 2 4FCA
pin 3 6F9A	pin 3 6F9A	pin 3 6F9A	pin 3 6F9A	pin 3 6F9A
pin 4 U759	pin 4 U759	pin 4 U759	pin 4 U759	pin 4 U759
pin 5 Ø356	pin 5 Ø356	pin 5 Ø356	pin 5 Ø356	pin 5 Ø356
pin 6 1U5P	pin 6 1U5P	pin 6 1U5P	pin 6 1U5P	pin 6 1U5P
pin 7 P763	pin 7 P763	pin 7 P763	pin 7 P763	pin 7 P763
pin 8 8484	pin 8 8484	pin 8 8484	pin 8 8484	pin 8 8484
pin 9 FFFF	pin 9 FFFF	pin 9 FFFF	pin 9 FFFF	pin 9 FFFF
pin 1Ø UUUU	pin 1Ø UUUU	pin 1Ø UUUU	pin 1Ø UUUU	pin 1Ø UUUU
pin 2Ø 64HF	pin 2Ø 29A4	pin 2Ø 5FUA	pin 2Ø 1183	pin 2Ø 2302
pin 21 37C5	pin 21 37C5	pin 21 37C5	pin 21 37C5	pin 21 37C5
pin 22 ØØØØ	pin 22 ØØØØ	pin 22 ØØØØ	pin 22 ØØØØ	pin 22 6Ø81
pin 23 6U28	pin 23 6U28	pin 23 6U28	pin 23 6U28	pin 23 6U28
pin 24 6321	pin 24 6321	pin 24 6321	pin 24 6321	pin 24 6321
pin 25 7791	pin 25 7791	pin 25 7791	pin 25 7791	pin 25 7791
pin 26 ØØØ3	pin 26 ØØØ3	pin 26 ØØØ3	pin 26 ØØØ3	pin 26 ØØØ3
pin 27 ØØØ3	pin 27 ØØØ3	pin 27 ØØØ3	pin 27 ØØØ3	pin 27 ØØØ3
pin 28 ØØØ3	pin 28 ØØØ3	pin 28 ØØØ3	pin 28 ØØØ3	pin 28 ØØØ3

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7D20 SIGNATURE TABLE 1.0

A9 U700		A9 U800		A9 U900		A9 U100		A9 U210	
pin 1	0003	pin 1	6F9A	pin 1	6F9A	pin 1	UUUU	pin 1	FFFF
pin 2	4FCA	pin 2	U759	pin 2	U759	pin 2	FFFF	pin 2	8484
pin 3	6F9A	pin 3	0356	pin 3	0356	pin 3	8484	pin 3	P763
pin 4	U759	pin 4	1U5P	pin 4	1U5P	pin 4	P763	pin 8	0000
pin 5	0356	pin 5	P763	pin 5	P763	pin 5	1U5P	pin 14	HH69
pin 6	1U5P	pin 6	8484	pin 6	8484	pin 7	0003	pin 15	0003
pin 7	P763	pin 7	FFFF	pin 7	FFFF	pin 8	0003	pin 16	0003
pin 8	8484	pin 8	UUUU	pin 8	UUUU	pin 9	0000		
pin 9	FFFF	pin 12	0000	pin 12	0000	pin 10	APC2		
pin 10	UUUU	pin 18	47UA	pin 18	54H4	pin 11	APC2		
pin 20	2302	pin 19	37C5	pin 19	37C5	pin 13	7791		
pin 21	37C5	pin 20	0000	pin 20	0000	pin 14	6321		
pin 22	6082	pin 21	0003	pin 21	0003	pin 15	6F9A		
pin 23	6U28	pin 22	6321	pin 22	6321	pin 16	U759		
pin 24	6321	pin 23	7791	pin 23	7791	pin 17	0356		
pin 25	7791	pin 24	0003	pin 24	0003	pin 18	0003		
pin 26	0003								
pin 27	0003								
pin 28	0003								

A9 U310		A9 U315		A9 U410		A9 U610		A9 U710	
pin 1	0003	pin 1	FFFF	pin 1	0003	pin 1	0356	pin 1	4868
pin 8	2246	pin 2	8484	pin 8	8F75	pin 2	U759	pin 2	9UP1
pin 9	0003	pin 3	P763			pin 3	6F9A	pin 3	0001
		pin 14	3FF4			pin 4	302P	pin 6	0003
		pin 15	0003			pin 5	7423	pin 7	1183
						pin 6	37C5	pin 8	0000
						pin 7	HH69	pin 9	64HF
						pin 8	0000	pin 10	29A4
						pin 9	3FF4	pin 11	5FUA
						pin 10	8F75	pin 12	2302
						pin 11	2246	pin 13	F9CF
						pin 12	H3P5	pin 14	534H
						pin 13	8317	pin 15	C9U1
						pin 14	6081	pin 16	0003
						pin 15	76C6		
						pin 16	0003		

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7D2Ø SIGNATURE TABLE 1.Ø

A9 U715		A9 U72Ø		A9 U725		A9 U81Ø		A9 U815	
pin	1 6U2C	pin	1 6Ø81	pin	2 ØØØØ	pin	1 C9U1	pin	1 ØØØ3
pin	2 4FCA	pin	2 6Ø81	pin	3 ØØØ3	pin	2 534H	pin	2 ØØØØ
pin	3 4868	pin	3 6Ø82	pin	4 6U2C	pin	3 PACF	pin	3 APC2
pin	5 ØØØ1	pin	4 6Ø82	pin	5 ØØØØ	pin	4 ØØØ3	pin	4 7423
pin	6 9UP1	pin	5 8317	pin	6 6U28	pin	5 ØØØ3	pin	5 PACU
pin	7 FØ77	pin	6 6Ø81	pin	7 ØØØØ	pin	6 ØØØØ	pin	6 3Ø2H
pin	8 ØØØØ	pin	7 ØØØØ	pin	8 7H7C	pin	7 ØØØØ	pin	7 ØØØØ
pin	9 Ø4HU	pin	8 ØØØ3	pin	9 PACF	pin	8 PACU	pin	8 3Ø2P
pin	1Ø 4P23	pin	9 ØØØØ	pin	1Ø 97F4	pin	9 PACF	pin	9 ØØØ3
pin	11 A98A	pin	1Ø ØØØ3	pin	11 7423	pin	1Ø ØØØ3	pin	1Ø ØØØ3
pin	12 47UA	pin	11 ØØØØ	pin	12 37C5	pin	11 ØØØ3	pin	11 3Ø2H
pin	13 54H4	pin	12 ØØØ3	pin	13 7H7C	pin	12 ØØØØ	pin	12 ØØØ3
pin	14 7423	pin	13 ØØØ3	pin	14 ØØØ3	pin	13 ØØØØ	pin	13 ØØØ3
pin	15 APC2	pin	14 ØØØ3			pin	14 ØØØ3	pin	14 ØØØ3
pin	16 ØØØ3								

A9 U825		A9 U91Ø		A9 U915		A9 U925		A9 U1Ø1Ø	
pin	1 ØØØØ	pin	1 ØØØØ	pin	1 ØØØ3	pin	1 ØØØ3	pin	1 7791
pin	2 3Ø2H	pin	2 ØØØ3	pin	3 Ø356	pin	3 4868	pin	2 6321
pin	3 ØØØ3	pin	3 ØØØ3	pin	4 6F9A	pin	7 6321	pin	3 37C5
pin	4 ØØØ3	pin	4 ØØØ3	pin	7 P763	pin	8 6U28	pin	4 7423
pin	5 ØØØØ	pin	8 UUUU	pin	8 UUUU	pin	1Ø ØØØØ	pin	5 3Ø2P
pin	8 ØØØØ	pin	9 FFFF	pin	1Ø ØØØØ	pin	11 3Ø2H	pin	6 ØØØ3
pin	9 ØØØØ	pin	1Ø 8484	pin	11 3Ø2H	pin	13 37C5	pin	7 95AØ
pin	1Ø 3Ø2H	pin	11 P763	pin	13 8484	pin	14 7791	pin	8 ØØØØ
pin	11 ØØØ3	pin	12 1U5P	pin	14 U759	pin	17 ØØØØ	pin	9 9C6A
pin	12 ØØØ3	pin	13 Ø356	pin	17 FFFF	pin	18 4FCA	pin	1Ø FUØ7
pin	13 ØØØØ	pin	14 U759	pin	18 1U5P	pin	2Ø ØØØ3	pin	11 F896
pin	16 ØØØ3	pin	15 6F9A	pin	2Ø ØØØ3			pin	12 H996
		pin	16 7791					pin	13 32Ø5
		pin	17 6321					pin	14 72P9
		pin	18 37C5					pin	15 P4Ø1
		pin	19 6U28					pin	16 ØØØ3
		pin	2Ø 4FCA						
		pin	21 4868						
		pin	22 9UP1						
		pin	23 ØØØ1						
		pin	32 ØØØ3						

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7D2Ø SIGNATURE TABLE 1.1

Firmware Version: 1.Ø1

Diagnostic Invoked: None (freerun)

For Testing: U4ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	U4ØØ-2Ø	_	ØØØØ
Stop	U71Ø-11	_/	ØØØØ
Clock	TP-824	_	118Ø

Configuration:

MPU Board on extender

Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812

Test Position P9ØØ P9Ø7

+5 Volt Signature: 118Ø

Ground Signature: ØØØØ

A9 U4ØØ
pin 11 79Ø9
pin 12 1CFU
pin 13 6U62
pin 15 P3FU
pin 16 A28H
pin 17 C8FH
pin 18 CØ8U
pin 19 69ØU

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7D2Ø SIGNATURE TABLE 1.2

Firmware Version: 1.Ø1

Diagnostic Invoked: None (freerun)

For Testing: U3ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	U3ØØ-2Ø	_	ØØØØ
Stop	U71Ø-1Ø	_/	ØØØØ
Clock	TP-824	_	118Ø

Configuration:

MPU Board on extender

Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812

Test Position P9ØØ P9Ø7

+5 Volt Signature: 118Ø

Ground Signature: ØØØØ

A9 U3ØØ
pin 11 P0H9
pin 12 PH6A
pin 13 ØØ28
pin 15 6Ø41
pin 16 392Ø
pin 17 U3FC
pin 18 7UAU
pin 19 6395

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7D2Ø SIGNATURE TABLE 1.3

Firmware Version: 1.Ø1

Diagnostic Invoked: None (freerun)

For Testing: U2ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Configuration:
MPU Board on extender
Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812
Test Position P9ØØ P9Ø7

Signature Analyzer Setup:

	connect	edge	signature
Start	U2ØØ-2Ø	_	ØØØØ
Stop	U71Ø-9	_/	ØØØØ
Clock	TP-824	_	118Ø

+5 Volt Signature: 118Ø
Ground Signature: ØØØØ

A9 U2ØØ
pin 11 285A
pin 12 P1ØC
pin 13 9HC2
pin 15 PAØ7
pin 16 4H2H
pin 17 5U42
pin 18 C684
pin 19 6795

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7D2Ø SIGNATURE TABLE 1.4

Firmware Version: 1.Ø1

Diagnostic Invoked: None (freerun)

For Testing: U5ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	U5ØØ-2Ø	_	ØØØØ
Stop	U71Ø-7	_/	ØØØØ
Clock	TP-824	_	118Ø

Configuration:

MPU Board on extender

Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812

Test Position P9ØØ P9Ø7

+5 Volt Signature: 118Ø

Ground Signature: ØØØØ

A9 U5ØØ
pin 11 4460
pin 12 3455
pin 13 539H
pin 15 1U49
pin 16 83FH
pin 17 H3AF
pin 18 8AP6
pin 19 4CC6

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7D2Ø SIGNATURE TABLE 1.5

Firmware Version: 1.Ø1

Diagnostic Invoked: None (freerun)

For Testing: U7ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	U7ØØ-2Ø	_	ØØØØ
Stop	U71Ø-12	_/	ØØØØ
Clock	TP-824	_	118Ø

Configuration:

MPU Board on extender

Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812

Test Position P9ØØ P9Ø7

Jumper U72Ø-1 to U72Ø-14

+5 Volt Signature: 118Ø

Ground Signature: ØØØØ

ADD OCT 1982

A9 U7ØØ
pin 11 Ø2Ø9
pin 12 U1AH
pin 13 83ØC
pin 15 3ØFC
pin 16 P227
pin 17 U91U
pin 18 16A2
pin 19 C932

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7D20 SIGNATURE TABLE 1.6

Firmware Version: 1.01

Diagnostic Invoked: None (freerun)

For Testing: U600 data

On Assembly: A9 MPU

Board Version: 670-7323-00

Signature Analyzer Setup:

	connect	edge	signature
Start	U600-20	_	0000
Stop	U710-12	_/	0000
Clock	TP-824	_	1180

Configuration:

MPU Board on extender

Remove P215 P720 P901 P902 P903 P904 P905 P906 P810 P811 P812

Test Position P900 P907

Jumper U720-5 to U720-14

+5 Volt Signature: 1180

Ground Signature: 0000

A9 U600
pin 11 UAUC
pin 12 38C4
pin 13 2P66
pin 15 5PU1
pin 16 F5P1
pin 17 242F
pin 18 3AF7
pin 19 F055

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7D2Ø SIGNATURE TABLE 2.Ø

Firmware Version: 1.Ø1

Diagnostic Invoked: External Bus Exerciser

For Testing: External Bus (data, address)

On Assembly: A9 MPU, A2 LED, A1 Switch

Board Version: 67Ø-7323-ØØ
67Ø-7316-ØØ
67Ø-7315-ØØ

Configuration:
MPU Board on extender
Frontpanel connected by cabling only
Remove P215 P51Ø

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	FU6C
Stop	TP-9Ø1*	_	FU6C
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU

+5 Volt Signature: FU6C
Ground Signature: ØØØØ

A9 U915		A9 U925		A9 U1ØØØ		A9 U1Ø1Ø		A2 U1ØØ	
pin 1	ØØØØ	pin 1	ØØØØ	pin 1	FU14	pin 1	8Ø9P	pin 1	CH33
pin 2	Ø2HØ	pin 2	AA25	pin 2	F7U2	pin 2	3HHA	pin 2	FU6C
pin 3	Ø2HØ	pin 3	AA25	pin 3	CH33	pin 3	795U	pin 7	ØØØØ
pin 4	2C65	pin 6	3HHA	pin 4	5735	pin 4	FFC6	pin 8	F22P
pin 5	2C65	pin 7	3HHA	pin 5	UU2F	pin 5	ØØØØ	pin 9	FU6C
pin 6	496P	pin 8	5AU6	pin 6	U6Ø7	pin 6	FU6C	pin 14	FU6C
pin 7	496P	pin 9	5AU6	pin 7	Ø3Ø4	pin 7	FU6C		
pin 8	A293	pin 1Ø	ØØØØ	pin 8	H7Ø8	pin 8	ØØØØ		
pin 9	A293	pin 11	FU6C	pin 9	873A	pin 9	FU6C		
pin 1Ø	ØØØØ	pin 12	795U	pin 1Ø	ØØØØ	pin 1Ø	FU6C		
pin 11	FU6C	pin 13	795U	pin 11	873A	pin 11	P7C5		
pin 12	Ø419	pin 14	8Ø9P	pin 12	H7Ø8	pin 12	43AC		
pin 13	Ø419	pin 15	8Ø9P	pin 13	Ø3Ø4	pin 13	3253		
pin 14	U7ØH	pin 16	FU14	pin 14	U6Ø7	pin 14	FU6C		
pin 15	U7ØH	pin 17	FU14	pin 15	UU2F	pin 15	9590		
pin 16	9P24	pin 18	PCUA	pin 16	5735	pin 16	FU6C		
pin 17	9P24	pin 19	PCUA	pin 17	CH33				
pin 18	P38F	pin 2Ø	FU6C	pin 18	F7U2				
pin 19	P38F			pin 19	28HP				
pin 2Ø	FU6C			pin 2Ø	FU6C				

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7D2Ø SIGNATURE TABLE 2.Ø

A2 U11Ø	A2 U12Ø	A2 U13Ø	A2 U14Ø	A2 U31Ø
pin 1 Ø3Ø4	pin 1 5735	pin 1 H7Ø8	pin 1 F7U2	pin 1 UU2F
pin 2 FU6C	pin 2 FU6C	pin 2 FU6C	pin 2 FU6C	pin 2 FU6C
pin 7 ØØØØ	pin 7 ØØØØ	pin 7 ØØØØ	pin 7 ØØØØ	pin 7 ØØØØ
pin 8 F22P	pin 8 F22P	pin 8 F22P	pin 8 F22P	pin 8 F22P
pin 9 FU6C	pin 9 FU6C	pin 9 FU6C	pin 9 FU6C	pin 9 FU6C
pin 14 FU6C	pin 14 FU6C	pin 14 FU6C	pin 14 FU6C	pin 14 FU6C

A2 U335	A2 U43Ø	A2 U5ØØ	A2 U72Ø	A1 U31Ø
pin 1 FU6C	pin 1 FU14	pin 1 U6Ø7	pin 2 FU6C	pin 1 496P
pin 2 43AC	pin 2 CH33	pin 2 FU6C	pin 3 43AC	pin 4 5735
pin 3 FU14	pin 3 U6Ø7	pin 7 ØØØØ	pin 4 96ØU	pin 6 ØØØØ
pin 4 1AFU	pin 4 Ø3Ø4	pin 8 F22P	pin 5 96ØU	pin 7 H7Ø8
pin 5 96ØU	pin 5 5735	pin 9 FU6C	pin 6 A293	pin 8 ØØØØ
pin 6 FU6C	pin 6 H7Ø8	pin 14 FU6C	pin 7 9P24	pin 9 UU2F
pin 7 FU6C	pin 7 873A		pin 8 Ø419	pin 1Ø ØØØØ
pin 8 ØØØØ	pin 8 UU2F		pin 9 FU6C	pin 12 873A
pin 9 FU6C	pin 9 F7U2		pin 19 3U69	pin 13 ØØØØ
pin 1Ø FU14	pin 1Ø ØØØØ		pin 2Ø ØØØØ	pin 15 FU6C
pin 11 3U69	pin 19 43AC		pin 4Ø FU6C	pin 16 FU6C
pin 12 F22P	pin 2Ø FU6C			
pin 13 P38F				
pin 14 ØØØØ				
pin 15 3253				
pin 16 FU6C				

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A1 U320		A1 U330		A1 U420	
pin	1 Ø419	pin	1 FU14	pin	1 496P
pin	2 FU14	pin	2 FU6C	pin	4 F7U2
pin	3 9P24	pin	3 5735	pin	7 U6Ø7
pin	4 ØØØØ	pin	4 FU6C	pin	8 ØØØØ
pin	5 ØØØØ	pin	5 873A	pin	9 CH33
pin	6 ØØØØ	pin	6 FU6C	pin	12 Ø3Ø4
pin	7 ØØØØ	pin	7 CH33	pin	15 FU6C
pin	8 ØØØØ	pin	8 FU6C	pin	16 FU6C
pin	9 ØØØØ	pin	9 U6Ø7		
pin	1Ø ØØØØ	pin	1Ø ØØØØ		
pin	11 ØØØØ	pin	11 F7U2		
pin	12 ØØØØ	pin	12 FU6C		
pin	13 A293	pin	13 UU2F		
pin	14 FU14	pin	14 FU6C		
pin	15 Ø419	pin	15 H7Ø8		
pin	16 FU6C	pin	16 FU6C		
		pin	17 Ø3Ø4		
		pin	18 FU6C		
		pin	19 FU14		
		pin	2Ø FU6C		

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7D2Ø SIGNATURE TABLE 3.Ø

Firmware Version: 1.Ø1

Diagnostic Invoked: Circuit Exerciser 432

For Testing: Address Bus & Last Address Latch

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	7ACC
Stop	TP-9Ø1*	_	7ACC
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 7ACC
Ground Signature: ØØØØ

A8 U2ØØ	A8 U42Ø	A8 U112Ø	A8 U122Ø	A8 U131Ø
pin 1 9616	pin 1 P532	pin 1 ØØØØ	pin 1 7CHC	pin 2 U887
pin 1Ø ØØØØ	pin 2 8C17	pin 8 ØØØØ	pin 2 7UAA	pin 3 5634
pin 2Ø 7ACC	pin 3 9616	pin 9 7ACC	pin 3 71CC	pin 5 P532
	pin 4 U887	pin 11 7ACC	pin 4 7ACC	pin 6 PHA2
	pin 5 1PCF	pin 14 C9C1	pin 5 7ACC	pin 8 ØØØØ
	pin 6 7ACC	pin 16 7ACC	pin 6 C9C1	pin 1Ø H9H9
	pin 7 7ACC		pin 7 ØØØØ	pin 11 8C17
	pin 8 ØØØØ		pin 8 ØØØØ	pin 14 7ACC
	pin 9 7ACC		pin 11 ØØØØ	pin 16 7ACC
	pin 1Ø U211		pin 13 PF7A	
	pin 11 7ACC		pin 14 U211	
	pin 12 7ACC		pin 15 7ACC	
	pin 13 7ACC		pin 16 7ACC	
	pin 14 7ACC			
	pin 15 9616			
	pin 16 7ACC			

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A8 U1410	
pin 2	7CHC
pin 3	CH82
pin 5	7UAA
pin 6	2FH6
pin 8	ØØØØ
pin 10	7A75
pin 11	71CC
pin 13	UU96
pin 14	F83A
pin 16	7ACC

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7D2Ø SIGNATURE TABLE 3.1

Firmware Version: 1.Ø1

Diagnostic Invoked: Circuit
Exerciser 432

For Testing: Memory Address Bus
Memory Data Bus

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	3395
Stop	TP-9Ø1*	_	3395
Clock	U112Ø-6	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 3395
Ground Signature: ØØØØ

A8 U2ØØ	A8 U21Ø	A8 U31Ø	A8 U41Ø	A8 U51Ø
pin 3 1H8	pin 2 Ø3PP	pin 2 U27A	pin 2 342A	pin 2 2H6A
pin 4 7832	pin 3 22P6	pin 3 22P6	pin 3 22P6	pin 3 22P6
pin 7 36CC	pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ
pin 8 89P3	pin 5 89P3	pin 5 89P3	pin 5 89P3	pin 5 89P3
pin 11 ØØØØ	pin 6 7832	pin 6 7832	pin 6 7832	pin 6 7832
pin 13 617F	pin 7 1H8	pin 7 1H8	pin 7 1H8	pin 7 1H8
pin 14 272U	pin 9 3395	pin 9 3395	pin 9 3395	pin 9 3395
pin 17 C2HP	pin 1Ø 36CC	pin 1Ø 36CC	pin 1Ø 36CC	pin 1Ø 36CC
pin 18 22P6	pin 11 272U	pin 11 272U	pin 11 272U	pin 11 272U
	pin 12 617F	pin 12 617F	pin 12 617F	pin 12 617F
	pin 13 C2HP	pin 13 C2HP	pin 13 C2HP	pin 13 C2HP
	pin 16 ØØØØ	pin 16 ØØØØ	pin 16 ØØØØ	pin 16 ØØØØ

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7D20 SIGNATURE TABLE 3.1

A8 U61Ø	A8 U71Ø	A8 U81Ø	A8 U91Ø	A8 U8ØØ
pin 2 4868	pin 2 HF62	pin 2 8F49	pin 2 FFP5	pin 6 C2HP
pin 3 22P6	pin 3 22P6	pin 3 22P6	pin 3 22P6	pin 7 36CC
pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ	pin 9 272U
pin 5 89P3	pin 5 89P3	pin 5 89P3	pin 5 89P3	pin 1Ø 617F
pin 6 7832	pin 6 7832	pin 6 7832	pin 6 7832	
pin 7 1HØ8	pin 7 1HØ8	pin 7 1HØ8	pin 7 1HØ8	
pin 9 3395	pin 9 3395	pin 9 3395	pin 9 3395	
pin 1Ø 36CC	pin 1Ø 36CC	pin 1Ø 36CC	pin 1Ø 36CC	
pin 11 272U	pin 11 272U	pin 11 272U	pin 11 272U	
pin 12 617F	pin 12 617F	pin 12 617F	pin 12 617F	
pin 13 C2HP	pin 13 C2HP	pin 13 C2HP	pin 13 C2HP	
pin 16 ØØØØ	pin 16 ØØØØ	pin 16 ØØØØ	pin 16 ØØØØ	

A8 U1Ø1Ø	A8 U111Ø	A8 U121Ø	A8 U131Ø	A8 U141Ø
pin 4 89P3	pin 4 272U	pin 4 89P3	pin 4 272U	pin 4 89P3
pin 7 1HØ8	pin 7 36CC	pin 7 1HØ8	pin 7 36CC	pin 7 1HØ8
pin 9 7832	pin 9 C2HP	pin 9 7832	pin 9 C2HP	pin 9 7832
pin 12 22P6	pin 12 22P6	pin 12 617F	pin 12 22P6	pin 12 617F

A8 U16ØØ	A8 U17ØØ
pin 4 FFP5	pin 4 2H6A
pin 7 8F49	pin 7 342A
pin 9 HF62	pin 9 U27A
pin 12 4868	pin 12 Ø3PP

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7D20 SIGNATURE TABLE 3.2

Firmware Version: 1.01

Diagnostic Invoked: Circuit Exerciser 432

For Testing: Data Bus

On Assembly: A8 Memory

Board Version: 670-7322-00

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-900*	_/	3395
Stop	TP-901*	_	3395
Clock	J410-21B	_/	0000

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 3395
Ground Signature: 0000

A8 U500	A8 U600	A8 U700	A8 U900	A8 U1000
pin 1 8F49	pin 1 342A	pin 1 8F49	pin 1 3395	pin 1 U27A
pin 15 FFP5	pin 9 03PP	pin 9 4868	pin 9 FFP5	pin 9 0000
	pin 10 U27A	pin 10 HF62	pin 10 3395	pin 10 03PP
	pin 15 2H6A	pin 15 FFP5	pin 15 3395	pin 15 342A

A8 U1100	A8 U800	A8 U1600	A8 U1700	A8 U200
pin 1 HF62	pin 1 8F49	pin 3 FFP5	pin 3 2H6A	pin 2 8F49
pin 9 2H6A	pin 2 HF62	pin 6 8F49	pin 6 342A	pin 5 HF62
pin 10 4868	pin 3 4868	pin 10 HF62	pin 10 U27A	pin 6 342A
pin 15 8F49	pin 15 FFP5	pin 13 4868	pin 13 03PP	pin 9 FFP5
				pin 12 4868
				pin 15 2H6A
				pin 16 U27A
				pin 19 03PP

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7D20 SIGNATURE TABLE 3.2

ADD OCT 1982

A8 U300		A8 U400	
pin	2 8F49	pin	2 8F49
pin	5 HF62	pin	5 HF62
pin	6 342A	pin	6 342A
pin	9 FFP5	pin	9 FFP5
pin	12 4868	pin	12 4868
pin	15 2H6A	pin	15 2H6A
pin	16 U27A	pin	16 U27A
pin	19 Ø3PP	pin	19 Ø3PP

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7D2Ø SIGNATURE TABLE 4.Ø

Firmware Version: 1.Ø1

Diagnostic Invoked: Circuit
Exerciser 4321

For Testing: Display Address
Generator

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	6PCP
Stop	TP-9Ø1*	_	6PCP
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 6PCP
Ground Signature: ØØØØ

A8 U5ØØ	A8 U6ØØ	A8 U7ØØ	A8 U42Ø	A8 U62Ø
pin 2 1UFP	pin 2 3H46	pin 2 ØP45	pin 1 HCPH	pin 1 C679
pin 3 H32C	pin 3 H8U8	pin 3 1C84	pin 2 H98U	pin 2 6UH8
pin 4 6PCP	pin 4 6PCP	pin 4 6PCP	pin 3 Ø3Ø4	pin 3 6U05
pin 5 ØØØØ	pin 5 ØØØØ	pin 5 ØØØØ	pin 4 ØØØØ	pin 7 ØØØØ
pin 8 ØØØØ	pin 6 6589	pin 6 C5UØ	pin 5 H98U	pin 14 6PCP
pin 11 6U05	pin 7 98C3	pin 7 1C55	pin 6 6PCP	
pin 13 6PCP	pin 8 ØØØØ	pin 8 ØØØØ	pin 7 6PCP	
pin 14 ØØØØ	pin 11 6UH8	pin 11 6UH8	pin 8 ØØØØ	
pin 16 6PCP	pin 12 ØØØØ	pin 12 ØØØØ	pin 9 6PCP	
	pin 13 6PCP	pin 13 6PCP	pin 1Ø C553	
	pin 14 ØØØØ	pin 14 ØØØØ	pin 11 6UH8	
	pin 16 6PCP	pin 16 6PCP	pin 12 6PCP	
			pin 13 6PCP	
			pin 14 6PCP	
			pin 15 Ø3Ø4	
			pin 16 6PCP	

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7D2Ø SIGNATURE TABLE 4.Ø

A8 U92Ø	A8 U1Ø1Ø	A8 U111Ø	A8 U121Ø	A8 U122Ø
pin 4 6PCP	pin 2 98C3	pin 2 H8U8	pin 2 1C84	pin 1 C679
pin 5 6PCP	pin 5 H32C	pin 5 3H46	pin 5 ØP45	pin 2 6H9F
pin 6 ØØØØ	pin 11 1UFP	pin 11 6589	pin 11 C5UØ	pin 3 H98U
pin 7 ØØØØ			pin 14 1C55	pin 4 6PCP
pin 8 6PCP				pin 5 ØØØØ
pin 1Ø ØØØØ				pin 6 4AØP
pin 14 6PCP				pin 7 6PCP
				pin 8 ØØØØ
				pin 9 ØØØØ
				pin 12 ØØØØ
				pin 13 CC1C
				pin 14 C553
				pin 15 6PCP
				pin 16 6PCP

A8 U132Ø
pin 4 6PCP
pin 5 ØØØØ
pin 6 ØØØØ
pin 7 ØØØØ
pin 14 6PCP

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7D2Ø SIGNATURE TABLE 5.Ø

Firmware Version: 1.Ø1

Diagnostic Invoked: Circuit Exerciser 64

For Testing: Acquire Address Generator

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	6F6P
Stop	TP-9Ø1*	_	6F6P
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 6F6P
Ground Signature: ØØØØ

A8 U42Ø	A8 U122Ø	A8 U9ØØ	A8 U1ØØØ	A8 U11ØØ
pin 1 1F46	pin 1 U43H	pin 1 6F6P	pin 2 491P	pin 2 P16C
pin 2 6884	pin 2 53PC	pin 2 98A7	pin 3 66FU	pin 3 H9ØA
pin 3 C891	pin 3 3F7Ø	pin 3 98A7	pin 4 AA2A	pin 4 U4F9
pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ	pin 5 ØØØØ	pin 5 ØØØØ
pin 5 3F7Ø	pin 5 6F6P	pin 5 ØØØØ	pin 6 7F47	pin 6 8P1A
pin 6 6F6P	pin 6 2U4H	pin 6 98A7	pin 7 ØØØØ	pin 7 55P9
pin 7 6F6P	pin 7 6F6P	pin 7 99P4	pin 8 ØØØØ	pin 8 ØØØØ
pin 8 ØØØØ	pin 8 ØØØØ	pin 8 ØØØØ	pin 11 U4F9	pin 11 U4F9
pin 9 U4F9	pin 1Ø ØØØØ	pin 1Ø 6F6P	pin 13 6F6P	pin 13 AA2A
pin 1Ø 7Ø28	pin 13 HUPA	pin 11 U4F9	pin 14 FF53	pin 14 FF53
pin 11 6F6P	pin 14 7Ø28	pin 13 U4F9	pin 16 6F6P	pin 16 6F6P
pin 12 6F6P	pin 15 6F6P	pin 14 FF53		
pin 13 AØ3H	pin 16 6F6P	pin 15 6F6P		
pin 14 6F6P		pin 16 6F6P		
pin 15 74F2				
pin 16 6F6P				

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7D2Ø SIGNATURE TABLE 5.Ø

A8 U1Ø1Ø		A8 U1Ø2Ø		A8 U111Ø		A8 U121Ø	
pin 3	55P9	pin 1	AØ3H	pin 3	H9ØA	pin 3	98A7
pin 6	66FU	pin 2	6F6P	pin 6	P16C	pin 6	98A7
pin 8	ØØØØ	pin 5	ØØØØ	pin 8	ØØØØ	pin 8	ØØØØ
pin 1Ø	491P	pin 6	6F6P	pin 1Ø	8P1A	pin 1Ø	98A7
pin 14	ØØØØ	pin 7	ØØØØ	pin 16	6F6P	pin 13	99P4
pin 16	6F6P	pin 12	FF53			pin 16	6F6P
		pin 13	6F6P				
		pin 14	6F6P				

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7D2Ø SIGNATURE TABLE 6.Ø

Firmware Version: 1.Ø1

Diagnostic Invoked: Circuit
Exerciser 6321

For Testing: Time Base
Data Registers

On Assembly: A11 Time Base

Board Version: 67Ø-7325-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	3H18
Stop	TP-9Ø1*	_	3H18
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:

+5 Volt Signature: 3H18
Ground Signature: ØØØØ

A11 U11Ø	A11 U121Ø	A11 U131Ø	A11 U132Ø	A11 U141Ø
pin 8 ØØØØ	pin 1 H13Ø	pin 1 CU0U	pin 1 H13Ø	pin 1 55F3
pin 15 ACF1	pin 2 ACF1	pin 2 CØ18	pin 2 ACF1	pin 2 68HC
pin 16 3H18	pin 8 ØØØØ	pin 3 ACF1	pin 8 ØØØØ	pin 3 4C4Ø
	pin 15 ØØØØ	pin 4 H5U5	pin 1Ø 4186	pin 4 7658
	pin 16 3H18	pin 5 F16A	pin 15 ØØØØ	pin 5 5UHU
		pin 6 HUP9	pin 16 3H18	pin 6 62F7
		pin 7 FC76		pin 7 ØØØØ
		pin 8 ØØØØ		pin 8 HUP9
		pin 9 4186		pin 9 P2U1
		pin 11 5UHU		pin 1Ø 7F44
		pin 12 4C4Ø		pin 11 415F
		pin 13 55F3		pin 12 415F
		pin 14 415F		pin 13 7F44
		pin 15 3H18		pin 14 3H18
		pin 16 3H18		

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7D20 SIGNATURE TABLE 6.0

A11 U1510		A11 U1610		A11 U1710		A11 U1300		A11 U1400	
pin	1 CU0U	pin	1 CU0U	pin	1 CU0U	pin	3 H8C8	pin	3 2987
pin	2 59P5	pin	2 FCF3	pin	2 3494	pin	4 5519	pin	4 4C40
pin	3 ACF1	pin	3 ACF1	pin	3 ACF1	pin	7 0000	pin	7 0000
pin	4 P8PH	pin	4 H5U5	pin	4 P8PH	pin	10 19H2	pin	10 P8PH
pin	5 2987	pin	5 UF72	pin	5 149U	pin	11 0000	pin	11 9473
pin	6 9473	pin	6 FC76	pin	6 5519	pin	14 3H18	pin	14 3H18
pin	7 5519	pin	7 P2U1	pin	7 A96C				
pin	8 0000	pin	8 0000	pin	8 0000				
pin	9 C018	pin	9 59P5	pin	9 FCF3				
pin	11 A426	pin	11 55F3	pin	11 H8C8				
pin	12 654F	pin	12 7F44	pin	12 24FA				
pin	13 H8C8	pin	13 4C40	pin	13 654F				
pin	14 19H2	pin	14 62F7	pin	14 993P				
pin	15 3H18	pin	15 3H18	pin	15 3H18				
pin	16 3H18	pin	16 3H18	pin	16 3H18				

A11 U1500		A11 U1600		A11 U1700	
pin	3 FC76	pin	3 24FA	pin	3 5519
pin	4 H5U5	pin	4 993P	pin	4 P8PH
pin	7 0000	pin	7 0000	pin	7 0000
pin	10 UF72	pin	10 654F	pin	10 149U
pin	11 62F7	pin	11 H8C8	pin	11 A96C
pin	14 3H18	pin	14 3H18	pin	14 3H18

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7D2Ø SIGNATURE TABLE 7.Ø

Firmware Version: 1.Ø1

Diagnostic Invoked: Circuit
Exerciser 641

For Testing: INS, SO, EOA
(flip-flops)

On Assembly: A11 Time Base

Board Version: 67Ø-7325-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	99FA
Stop	TP-9Ø1*	_	99FA
Clock	U132Ø-1	_/	ØØØØ

* on A9 MPU Board

Configuration:

+5 Volt Signature: 99FA
Ground Signature: ØØØØ

A11 U31Ø	A11 U41Ø	A11 U71Ø	A11 U91Ø	A11 U1Ø1Ø
pin 7 ØØØØ	pin 7 ØØØØ	pin 7 ØØØØ	pin 2 ØØØØ	pin 1 Ø7U3
pin 11 3172	pin 8 99FA	pin 8 A5UA	pin 3 Ø43H	pin 2 3172
pin 12 Ø7U3	pin 9 ØØØØ	pin 9 99FA	pin 4 6Ø4A	pin 3 Ø43H
pin 13 AC76	pin 1Ø 99FA	pin 1Ø 3F3Ø	pin 5 A892	pin 7 ØØØØ
pin 14 99FA	pin 14 99FA	pin 14 99FA	pin 6 3158	pin 11 A5UA
			pin 7 A97C	pin 12 A5UA
			pin 8 ØØØØ	pin 13 A5UA
			pin 9 32CF	pin 14 99FA
			pin 1Ø 9P39	
			pin 11 3172	
			pin 12 ØØØØ	
			pin 14 A5UA	
			pin 15 A5UA	
			pin 16 99FA	

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7D2Ø SIGNATURE TABLE 7.Ø

A11 U11ØØ	A11 U112Ø	A11 U12ØØ	A11 U141Ø	A11 U13ØØ
pin 1 U98Ø	pin 1 3172	pin 2 ØØØØ	pin 7 ØØØØ	pin 1 99FA
pin 2 9P39	pin 2 A8C8	pin 3 ØØØØ	pin 1Ø Ø7U3	pin 7 ØØØØ
pin 3 6Ø4A	pin 3 99FA	pin 4 99FA	pin 11 9P39	pin 12 3172
pin 7 ØØØØ	pin 7 ØØØØ	pin 5 3172	pin 12 9P39	pin 13 A5UA
pin 14 99FA	pin 14 99FA	pin 6 A8C8	pin 13 Ø7U3	pin 14 99FA
		pin 7 A8C8	pin 14 99FA	
		pin 8 ØØØØ		
		pin 9 3172		
		pin 1Ø 99FA		
		pin 11 3172		
		pin 12 ØØØØ		
		pin 14 A5UA		
		pin 15 A5UA		
		pin 16 99FA		

A11 U14ØØ	A11 U15ØØ	A11 U16ØØ	A11 U17ØØ
pin 1 99FA	pin 1 99FA	pin 1 99FA	pin 1 99FA
pin 7 ØØØØ	pin 7 ØØØØ	pin 7 ØØØØ	pin 7 ØØØØ
pin 13 A5UA	pin 13 A5UA	pin 13 A5UA	pin 13 A5UA
pin 14 99FA	pin 14 99FA	pin 14 99FA	pin 14 99FA

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7D2Ø SIGNATURE TABLE 8.Ø

Firmware Version: 1.Ø1

Diagnostic Invoked: Circuit Exerciser 6431

For Testing: Preamplifier Data Registers

On Assembly: A4 Preamplifier

Board Version: 67Ø-7318-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	3H18
Stop	TP-9Ø1*	_	3H18
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:

+5 Volt Signature: 3H18
Ground Signature: ØØØØ

A4 U3ØØ	A4 U123Ø	A4 U34Ø	A4 U91Ø	A4 U93Ø
pin 1 CU0U	pin 1 CU0U	pin 9 H8C8	pin 3 F16A	pin 3 FC76
pin 2 46A2	pin 2 3494	pin 1Ø A426	pin 5 H5U5	pin 5 HUP9
pin 3 8HF9	pin 3 8HF9	pin 11 5854		
pin 4 P8PH	pin 4 H5U5			
pin 5 149U	pin 5 F16A			
pin 6 68Ø1	pin 6 HUP9			
pin 7 9473	pin 7 FC76			
pin 8 ØØØØ	pin 8 ØØØØ			
pin 9 8C29	pin 9 46A2			
pin 11 24FA	pin 11 5UHU			
pin 12 H8C8	pin 12 4C4Ø			
pin 13 A426	pin 13 55F3			
pin 14 5854	pin 14 415F			
pin 15 3H18	pin 15 3H18			
pin 16 3H18	pin 16 3H18			

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7D2Ø SIGNATURE TABLE 9.Ø

Firmware Version: 1.Ø1

Diagnostic Invoked: Circuit Exerciser 6431

For Testing: Trigger Data Registers

On Assembly: A1Ø Trigger

Board Version: 67Ø-7324-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	3H18
Stop	TP-9Ø1*	_	3H18
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:
Trigger Board on extender

+5 Volt Signature: 3H18
Ground Signature: ØØØØ

A1Ø U1Ø1		A1Ø U2ØØ		A1Ø U2Ø1		A1Ø U21Ø		A1Ø U3ØØ	
pin 4	HCP7	pin 1	CUØU	pin 1	CUØU	pin 1	CUØU	pin 6	A96C
pin 5	F13A	pin 2	3944	pin 2	32C4	pin 2	3494	pin 8	ØØØØ
pin 7	ØØØØ	pin 3	P6UU	pin 3	P6UU	pin 3	P6UU	pin 9	ØØØØ
pin 8	993P	pin 4	H5U5	pin 4	P8PH	pin 4	H5U5	pin 1Ø	68Ø1
pin 9	3H18	pin 5	F16A	pin 5	2987	pin 5	UF72	pin 11	P5AØ
pin 1Ø	A426	pin 6	P2U1	pin 6	A96C	pin 6	U66P	pin 15	ØØØØ
pin 11	HCP7	pin 7	U66P	pin 7	68Ø1	pin 7	HUP9	pin 16	3H18
pin 12	3H18	pin 8	ØØØØ	pin 8	ØØØØ	pin 8	ØØØØ		
pin 13	P6UU	pin 9	F13A	pin 9	3944	pin 9	32C4		
pin 14	3H18	pin 11	4C4Ø	pin 1Ø	P1AU	pin 11	7F44		
		pin 12	5UHU	pin 11	654F	pin 12	55F3		
		pin 13	7F44	pin 12	A426	pin 13	5UHU		
		pin 14	68HC	pin 13	24FA	pin 14	7658		
		pin 15	3H18	pin 14	P5AØ	pin 15	3H18		
		pin 16	3H18	pin 15	3H18	pin 16	3H18		
				pin 16	3H18				

A1Ø U31Ø	
pin 5	7F44
pin 6	55F3
pin 7	5UHU
pin 8	7658
pin 9	HUP9
pin 1Ø	U66P
pin 11	UF72
pin 12	H5U5

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SIGNATURE ANALYSIS TABLES
FIRMWARE VERSION 1.02

ADD DEC 1982

FIRMWARE VERSION 1.02 CROSS REFERENCE

(Use in conjunction with Table 7-1
at the beginning of the Signature Analysis Tables).

Circuit Number	IC Part Number
A9U200	160-1164-02
A9U300	160-1165-02
A9U400	160-1163-02
A9U500	160-1162-02
A9U600	160-1676-02
A9U700	160-1757-02

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7D2Ø SIGNATURE TABLE 1.Ø

ADD DEC 1982

Firmware Version: 1.Ø2

Diagnostic Invoked: None (freerun)

For Testing: Address and Control

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-82Ø	_	ØØØ1
Stop	TP-82Ø	_	ØØØ1
Clock	TP-824	_	ØØØ3

Configuration:

MPU Board on extender

Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812

Test Position P9ØØ P9Ø7

Jumper U11Ø-5 to U11Ø-14

+5 Volt Signature: ØØØ3

Ground Signature: ØØØØ

A9 U2ØØ	A9 U3ØØ	A9 U4ØØ	A9 U5ØØ	A9 U6ØØ
pin 1 ØØØ3	pin 1 ØØØ3	pin 1 ØØØ3	pin 1 ØØØ3	pin 1 ØØØ3
pin 2 4FCA	pin 2 4FCA	pin 2 4FCA	pin 2 4FCA	pin 2 4FCA
pin 3 6F9A	pin 3 6F9A	pin 3 6F9A	pin 3 6F9A	pin 3 6F9A
pin 4 U759	pin 4 U759	pin 4 U759	pin 4 U759	pin 4 U759
pin 5 Ø356	pin 5 Ø356	pin 5 Ø356	pin 5 Ø356	pin 5 Ø356
pin 6 1U5P	pin 6 1U5P	pin 6 1U5P	pin 6 1U5P	pin 6 1U5P
pin 7 P763	pin 7 P763	pin 7 P763	pin 7 P763	pin 7 P763
pin 8 8484	pin 8 8484	pin 8 8484	pin 8 8484	pin 8 8484
pin 9 FFFF	pin 9 FFFF	pin 9 FFFF	pin 9 FFFF	pin 9 FFFF
pin 1Ø UUUU	pin 1Ø UUUU	pin 1Ø UUUU	pin 1Ø UUUU	pin 1Ø UUUU
pin 2Ø 64HF	pin 2Ø 29A4	pin 2Ø 5FUA	pin 2Ø 1183	pin 2Ø 2302
pin 21 37C5	pin 21 37C5	pin 21 37C5	pin 21 37C5	pin 21 37C5
pin 22 ØØØØ	pin 22 ØØØØ	pin 22 ØØØØ	pin 22 ØØØØ	pin 22 6Ø81
pin 23 6U28	pin 23 6U28	pin 23 6U28	pin 23 6U28	pin 23 6U28
pin 24 6321	pin 24 6321	pin 24 6321	pin 24 6321	pin 24 6321
pin 25 7791	pin 25 7791	pin 25 7791	pin 25 7791	pin 25 7791
pin 26 ØØØ3	pin 26 ØØØ3	pin 26 ØØØ3	pin 26 ØØØ3	pin 26 ØØØ3
pin 27 ØØØ3	pin 27 ØØØ3	pin 27 ØØØ3	pin 27 ØØØ3	pin 27 ØØØ3
pin 28 ØØØ3	pin 28 ØØØ3	pin 28 ØØØ3	pin 28 ØØØ3	pin 28 ØØØ3

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A9 U7ØØ		A9 U8ØØ		A9 U9ØØ		A9 U1ØØ		A9 U21Ø	
pin	1 ØØØ3	pin	1 6F9A	pin	1 6F9A	pin	1 UUUU	pin	1 FFFF
pin	2 4FCA	pin	2 U759	pin	2 U759	pin	2 FFFF	pin	2 8484
pin	3 6F9A	pin	3 Ø356	pin	3 Ø356	pin	3 8484	pin	3 P763
pin	4 U759	pin	4 1U5P	pin	4 1U5P	pin	4 P763	pin	8 ØØØØ
pin	5 Ø356	pin	5 P763	pin	5 P763	pin	5 1U5P	pin	14 HH69
pin	6 1U5P	pin	6 8484	pin	6 8484	pin	7 ØØØ3	pin	15 ØØØ3
pin	7 P763	pin	7 FFFF	pin	7 FFFF	pin	8 ØØØ3	pin	16 ØØØ3
pin	8 8484	pin	8 UUUU	pin	8 UUUU	pin	9 ØØØØ		
pin	9 FFFF	pin	12 ØØØØ	pin	12 ØØØØ	pin	1Ø APC2		
pin	1Ø UUUU	pin	18 47UA	pin	18 54H4	pin	11 APC2		
pin	2Ø 23Ø2	pin	19 37C5	pin	19 37C5	pin	13 7791		
pin	21 37C5	pin	2Ø ØØØØ	pin	2Ø ØØØØ	pin	14 6321		
pin	22 6Ø82	pin	21 ØØØ3	pin	21 ØØØ3	pin	15 6F9A		
pin	23 6U28	pin	22 6321	pin	22 6321	pin	16 U759		
pin	24 6321	pin	23 7791	pin	23 7791	pin	17 Ø356		
pin	25 7791	pin	24 ØØØ3	pin	24 ØØØ3	pin	18 ØØØ3		
pin	26 ØØØ3								
pin	27 ØØØ3								
pin	28 ØØØ3								

A9 U31Ø		A9 U315		A9 U41Ø		A9 U61Ø		A9 U71Ø	
pin	1 ØØØ3	pin	1 FFFF	pin	1 ØØØ3	pin	1 Ø356	pin	1 4868
pin	8 2246	pin	2 8484	pin	8 8F75	pin	2 U759	pin	2 9UP1
pin	9 ØØØ3	pin	3 P763			pin	3 6F9A	pin	3 ØØØ1
		pin	14 3FF4			pin	4 3Ø2P	pin	6 ØØØ3
		pin	15 ØØØ3			pin	5 7423	pin	7 1183
						pin	6 37C5	pin	8 ØØØØ
						pin	7 HH69	pin	9 64HF
						pin	8 ØØØØ	pin	1Ø 29A4
						pin	9 3FF4	pin	11 5FUA
						pin	1Ø 8F75	pin	12 23Ø2
						pin	11 2246	pin	13 F9CF
						pin	12 H3P5	pin	14 534H
						pin	13 8317	pin	15 C9U1
						pin	14 6Ø81	pin	16 ØØØ3
						pin	15 76C6		
						pin	16 ØØØ3		

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7D2Ø SIGNATURE TABLE 1.Ø

A9 U715		A9 U72Ø		A9 U725		A9 U81Ø		A9 U815	
pin	1 6U2C	pin	1 6Ø81	pin	2 ØØØØ	pin	1 C9U1	pin	1 ØØØ3
pin	2 4FCA	pin	2 6Ø81	pin	3 ØØØ3	pin	2 534H	pin	2 ØØØØ
pin	3 4868	pin	3 6Ø82	pin	4 6U2C	pin	3 PACF	pin	3 APC2
pin	5 ØØØ1	pin	4 6Ø82	pin	5 ØØØØ	pin	4 ØØØ3	pin	4 7423
pin	6 9UP1	pin	5 8317	pin	6 6U28	pin	5 ØØØ3	pin	5 PACU
pin	7 FØ77	pin	6 6Ø81	pin	7 ØØØØ	pin	6 ØØØØ	pin	6 3Ø2H
pin	8 ØØØØ	pin	7 ØØØØ	pin	8 7H7C	pin	7 ØØØØ	pin	7 ØØØØ
pin	9 Ø4HU	pin	8 ØØØ3	pin	9 PACF	pin	8 PACU	pin	8 3Ø2P
pin	1Ø 4P23	pin	9 ØØØØ	pin	1Ø 97F4	pin	9 PACF	pin	9 ØØØ3
pin	11 A98A	pin	1Ø ØØØ3	pin	11 7423	pin	1Ø ØØØ3	pin	1Ø ØØØ3
pin	12 47UA	pin	11 ØØØØ	pin	12 37C5	pin	11 ØØØ3	pin	11 3Ø2H
pin	13 54H4	pin	12 ØØØ3	pin	13 7H7C	pin	12 ØØØØ	pin	12 ØØØ3
pin	14 7423	pin	13 ØØØ3	pin	14 ØØØ3	pin	13 ØØØØ	pin	13 ØØØ3
pin	15 APC2	pin	14 ØØØ3			pin	14 ØØØ3	pin	14 ØØØ3
pin	16 ØØØ3								

A9 U825		A9 U91Ø		A9 U915		A9 U925		A9 U1Ø1Ø	
pin	1 ØØØØ	pin	1 ØØØØ	pin	1 ØØØ3	pin	1 ØØØ3	pin	1 7791
pin	2 3Ø2H	pin	2 ØØØ3	pin	3 Ø356	pin	3 4868	pin	2 6321
pin	3 ØØØ3	pin	3 ØØØ3	pin	4 6F9A	pin	7 6321	pin	3 37C5
pin	4 ØØØ3	pin	4 ØØØ3	pin	7 P763	pin	8 6U28	pin	4 7423
pin	5 ØØØØ	pin	8 UUUU	pin	8 UUUU	pin	1Ø ØØØØ	pin	5 3Ø2P
pin	8 ØØØØ	pin	9 FFFF	pin	1Ø ØØØØ	pin	11 3Ø2H	pin	6 ØØØ3
pin	9 ØØØØ	pin	1Ø 8484	pin	11 3Ø2H	pin	13 37C5	pin	7 95AØ
pin	1Ø 3Ø2H	pin	11 P763	pin	13 8484	pin	14 7791	pin	8 ØØØØ
pin	11 ØØØ3	pin	12 1U5P	pin	14 U759	pin	17 ØØØØ	pin	9 9C6A
pin	12 ØØØ3	pin	13 Ø356	pin	17 FFFF	pin	18 4FCA	pin	1Ø FUØ7
pin	13 ØØØØ	pin	14 U759	pin	18 1U5P	pin	2Ø ØØØ3	pin	11 F896
pin	16 ØØØ3	pin	15 6F9A	pin	2Ø ØØØ3			pin	12 H996
		pin	16 7791					pin	13 3ØØ5
		pin	17 6321					pin	14 72P9
		pin	18 37C5					pin	15 P4Ø1
		pin	19 6U28					pin	16 ØØØ3
		pin	2Ø 4FCA						
		pin	21 4868						
		pin	22 9UP1						
		pin	23 ØØØ1						
		pin	32 ØØØ3						

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7D2Ø SIGNATURE TABLE 1.1

Firmware Version: 1.Ø2

Diagnostic Invoked: None (freerun)

For Testing: U4ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	U4ØØ-2Ø	_	ØØØØ
Stop	U71Ø-11	_/	ØØØØ
Clock	TP-824	_	118Ø

Configuration:

MPU Board on extender

Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812

Test Position P9ØØ P9Ø7

+5 Volt Signature: 118Ø

Ground Signature: ØØØØ

A9 U4ØØ
pin 11 478C
pin 12 3HPH
pin 13 7H59
pin 15 3H2H
pin 16 ØUF3
pin 17 U973
pin 18 Ø4CU
pin 19 FF3F

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7D2Ø SIGNATURE TABLE 1.2

Firmware Version: 1.Ø2

Diagnostic Invoked: None (freerun)

For Testing: U3ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	U3ØØ-2Ø	_	ØØØØ
Stop	U71Ø-1Ø	_/	ØØØØ
Clock	TP-824	_	118Ø

Configuration:

MPU Board on extender

Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812

Test Position P9ØØ P9Ø7

+5 Volt Signature: 118Ø

Ground Signature: ØØØØ

A9 U3ØØ
pin 11 PØH9
pin 12 8P7F
pin 13 4UAF
pin 15 6P17
pin 16 1PH8
pin 17 CU4P
pin 18 7UAU
pin 19 6395

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7D2Ø SIGNATURE TABLE 1.3

Firmware Version: 1.Ø2

Diagnostic Invoked: None (freerun)

For Testing: U2ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	U2ØØ-2Ø	_	ØØØØ
Stop	U71Ø-9	_/	ØØØØ
Clock	TP-824	_	118Ø

Configuration:

MPU Board on extender

Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812

Test Position P9ØØ P9Ø7

+5 Volt Signature: 118Ø

Ground Signature: ØØØØ

A9 U2ØØ
pin 11 3H22
pin 12 587C
pin 13 H89C
pin 15 3P37
pin 16 991H
pin 17 ØAA2
pin 18 A3UF
pin 19 3275

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7D2Ø SIGNATURE TABLE 1.4

Firmware Version: 1.Ø2

Diagnostic Invoked: None (freerun)

For Testing: U5ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	U5ØØ-2Ø	_	ØØØØ
Stop	U71Ø-7	_/	ØØØØ
Clock	TP-824	_	118Ø

Configuration:

MPU Board on extender

Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812

Test Position P9ØØ P9Ø7

+5 Volt Signature: 118Ø

Ground Signature: ØØØØ

A9 U5ØØ
pin 11 19HA
pin 12 4UFH
pin 13 Ø67H
pin 15 542C
pin 16 96C5
pin 17 F6H4
pin 18 FA7P
pin 19 5PFP

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7D2Ø SIGNATURE TABLE 1.5

Firmware Version: 1.Ø2

Diagnostic Invoked: None (freerun)

For Testing: U7ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	U7ØØ-2Ø	_	ØØØØ
Stop	U71Ø-12	_/	ØØØØ
Clock	TP-824	_	118Ø

Configuration:

MPU Board on extender
Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812
Test Position P9ØØ P9Ø7
Jumper U72Ø-1 to U72Ø-14

+5 Volt Signature: 118Ø
Ground Signature: ØØØØ

A9 U7ØØ
pin 11 17F5
pin 12 6UØ4
pin 13 814F
pin 15 1949
pin 16 2H34
pin 17 PP2Ø
pin 18 P54C
pin 19 5UA3

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7D2Ø SIGNATURE TABLE 1.6

Firmware Version: 1.Ø2

Diagnostic Invoked: None (freerun)

For Testing: U6ØØ data

On Assembly: A9 MPU

Board Version: 67Ø-7323-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	U6ØØ-2Ø	_	ØØØØ
Stop	U71Ø-12	_/	ØØØØ
Clock	TP-824	_	118Ø

Configuration:

MPU Board on extender

Remove P215 P72Ø P9Ø1 P9Ø2 P9Ø3 P9Ø4 P9Ø5 P9Ø6 P81Ø P811 P812

Test Position P9ØØ P9Ø7

Jumper U72Ø-5 to U72Ø-14

+5 Volt Signature: 118Ø

Ground Signature: ØØØØ

A9 U6ØØ
pin 11 CA63
pin 12 HA8U
pin 13 7C86
pin 15 H18A
pin 16 1U7A
pin 17 64C4
pin 18 7A5U
pin 19 FØ55

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7D2Ø SIGNATURE TABLE 2.Ø

Firmware Version: 1.Ø2

Diagnostic Invoked: External Bus Exerciser

For Testing: External Bus (data, address)

On Assembly: A9 MPU, A2 LED, A1 Switch

Board Version: 67Ø-7323-ØØ
67Ø-7316-ØØ
67Ø-7315-ØØ

Configuration:
MPU Board on extender
Frontpanel connected by cabling only
Remove P215 P51Ø

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	FU6C
Stop	TP-9Ø1*	_	FU6C
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU

+5 Volt Signature: FU6C
Ground Signature: ØØØØ

A9 U915		A9 U925		A9 U1ØØØ		A9 U1Ø1Ø		A2 U1ØØ	
pin 1	ØØØØ	pin 1	ØØØØ	pin 1	FU14	pin 1	8Ø9P	pin 1	CH33
pin 2	Ø2HØ	pin 2	AA25	pin 2	F7U2	pin 2	3HHA	pin 2	FU6C
pin 3	Ø2HØ	pin 3	AA25	pin 3	CH33	pin 3	795U	pin 7	ØØØØ
pin 4	2C65	pin 6	3HHA	pin 4	5735	pin 4	FFC6	pin 8	F22P
pin 5	2C65	pin 7	3HHA	pin 5	UU2F	pin 5	ØØØØ	pin 9	FU6C
pin 6	496P	pin 8	5AU6	pin 6	U6Ø7	pin 6	FU6C	pin 14	FU6C
pin 7	496P	pin 9	5AU6	pin 7	Ø3Ø4	pin 7	FU6C		
pin 8	A293	pin 1Ø	ØØØØ	pin 8	H7Ø8	pin 8	ØØØØ		
pin 9	A293	pin 11	FU6C	pin 9	873A	pin 9	FU6C		
pin 1Ø	ØØØØ	pin 12	795U	pin 1Ø	ØØØØ	pin 1Ø	FU6C		
pin 11	FU6C	pin 13	795U	pin 11	873A	pin 11	P7C5		
pin 12	Ø419	pin 14	8Ø9P	pin 12	H7Ø8	pin 12	43AC		
pin 13	Ø419	pin 15	8Ø9P	pin 13	Ø3Ø4	pin 13	3253		
pin 14	U7ØH	pin 16	FU14	pin 14	U6Ø7	pin 14	FU6C		
pin 15	U7ØH	pin 17	FU14	pin 15	UU2F	pin 15	9590		
pin 16	9P24	pin 18	PCUA	pin 16	5735	pin 16	FU6C		
pin 17	9P24	pin 19	PCUA	pin 17	CH33				
pin 18	P38F	pin 2Ø	FU6C	pin 18	F7U2				
pin 19	P38F			pin 19	28HP				
pin 2Ø	FU6C			pin 2Ø	FU6C				

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7D2Ø SIGNATURE TABLE 2.Ø

A2 U11Ø		A2 U12Ø		A2 U13Ø		A2 U14Ø		A2 U31Ø	
pin	1 Ø3Ø4	pin	1 5735	pin	1 H7Ø8	pin	1 F7U2	pin	1 UU2F
pin	2 FU6C	pin	2 FU6C	pin	2 FU6C	pin	2 FU6C	pin	2 FU6C
pin	7 ØØØØ	pin	7 ØØØØ	pin	7 ØØØØ	pin	7 ØØØØ	pin	7 ØØØØ
pin	8 F22P	pin	8 F22P	pin	8 F22P	pin	8 F22P	pin	8 F22P
pin	9 FU6C	pin	9 FU6C	pin	9 FU6C	pin	9 FU6C	pin	9 FU6C
pin	14 FU6C	pin	14 FU6C	pin	14 FU6C	pin	14 FU6C	pin	14 FU6C

A2 U335		A2 U43Ø		A2 U5ØØ		A2 U72Ø		A1 U31Ø	
pin	1 FU6C	pin	1 FU14	pin	1 U6Ø7	pin	2 FU6C	pin	1 496P
pin	2 43AC	pin	2 CH33	pin	2 FU6C	pin	3 43AC	pin	4 5735
pin	3 FU14	pin	3 U6Ø7	pin	7 ØØØØ	pin	4 96ØU	pin	6 ØØØØ
pin	4 1AFU	pin	4 Ø3Ø4	pin	8 F22P	pin	5 96ØU	pin	7 H7Ø8
pin	5 96ØU	pin	5 5735	pin	9 FU6C	pin	6 A293	pin	8 ØØØØ
pin	6 FU6C	pin	6 H7Ø8	pin	14 FU6C	pin	7 9P24	pin	9 UU2F
pin	7 FU6C	pin	7 873A			pin	8 Ø419	pin	1Ø ØØØØ
pin	8 ØØØØ	pin	8 UU2F			pin	9 FU6C	pin	12 873A
pin	9 FU6C	pin	9 F7U2			pin	19 3U69	pin	13 ØØØØ
pin	1Ø FU14	pin	1Ø ØØØØ			pin	2Ø ØØØØ	pin	15 FU6C
pin	11 3U69	pin	19 43AC			pin	4Ø FU6C	pin	16 FU6C
pin	12 F22P	pin	2Ø FU6C						
pin	13 P38F								
pin	14 ØØØØ								
pin	15 3253								
pin	16 FU6C								

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A1 U32Ø		A1 U33Ø		A1 U42Ø	
pin 1	Ø419	pin 1	FU14	pin 1	496P
pin 2	FU14	pin 2	FU6C	pin 4	F7U2
pin 3	9P24	pin 3	5735	pin 7	U6Ø7
pin 4	ØØØØ	pin 4	FU6C	pin 8	ØØØØ
pin 5	ØØØØ	pin 5	873A	pin 9	CH33
pin 6	ØØØØ	pin 6	FU6C	pin 12	Ø3Ø4
pin 7	ØØØØ	pin 7	CH33	pin 15	FU6C
pin 8	ØØØØ	pin 8	FU6C	pin 16	FU6C
pin 9	ØØØØ	pin 9	U6Ø7		
pin 1Ø	ØØØØ	pin 1Ø	ØØØØ		
pin 11	ØØØØ	pin 11	F7U2		
pin 12	ØØØØ	pin 12	FU6C		
pin 13	A293	pin 13	UU2F		
pin 14	FU14	pin 14	FU6C		
pin 15	Ø419	pin 15	H7Ø8		
pin 16	FU6C	pin 16	FU6C		
		pin 17	Ø3Ø4		
		pin 18	FU6C		
		pin 19	FU14		
		pin 2Ø	FU6C		

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7D2Ø SIGNATURE TABLE 3.Ø

Firmware Version: 1.Ø2

Diagnostic Invoked: Circuit
Exerciser 432

For Testing: Address Bus &
Last Address Latch

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	7ACC
Stop	TP-9Ø1*	_	7ACC
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 7ACC
Ground Signature: ØØØØ

A8 U2ØØ	A8 U42Ø	A8 U112Ø	A8 U122Ø	A8 U131Ø
pin 1 9616	pin 1 P532	pin 1 ØØØØ	pin 1 7CHC	pin 2 U887
pin 1Ø ØØØØ	pin 2 8C17	pin 8 ØØØØ	pin 2 7UAA	pin 3 5634
pin 2Ø 7ACC	pin 3 9616	pin 9 7ACC	pin 3 71CC	pin 5 P532
	pin 4 U887	pin 11 7ACC	pin 4 7ACC	pin 6 PHA2
	pin 5 1PCF	pin 14 C9C1	pin 5 7ACC	pin 8 ØØØØ
	pin 6 7ACC	pin 16 7ACC	pin 6 C9C1	pin 1Ø H9H9
	pin 7 7ACC		pin 7 ØØØØ	pin 11 8C17
	pin 8 ØØØØ		pin 8 ØØØØ	pin 14 7ACC
	pin 9 7ACC		pin 11 ØØØØ	pin 16 7ACC
	pin 1Ø U211		pin 13 PF7A	
	pin 11 7ACC		pin 14 U211	
	pin 12 7ACC		pin 15 7ACC	
	pin 13 7ACC		pin 16 7ACC	
	pin 14 7ACC			
	pin 15 9616			
	pin 16 7ACC			

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A8 U141Ø	
pin 2	7CHC
pin 3	CH82
pin 5	7UAA
pin 6	2FH6
pin 8	ØØØØ
pin 1Ø	7A75
pin 11	71CC
pin 13	UU96
pin 14	F83A
pin 16	7ACC

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7D2Ø SIGNATURE TABLE 3.1

Firmware Version: 1.Ø2

Diagnostic Invoked: Circuit
Exerciser 432

For Testing: Memory Address Bus
Memory Data Bus

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	3395
Stop	TP-9Ø1*	_	3395
Clock	U112Ø-6	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 3395
Ground Signature: ØØØØ

A8 U2ØØ	A8 U21Ø	A8 U31Ø	A8 U41Ø	A8 U51Ø
pin 3 1H8	pin 2 Ø3PP	pin 2 U27A	pin 2 342A	pin 2 2H6A
pin 4 7832	pin 3 22P6	pin 3 22P6	pin 3 22P6	pin 3 22P6
pin 7 36CC	pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ
pin 8 89P3	pin 5 89P3	pin 5 89P3	pin 5 89P3	pin 5 89P3
pin 11 ØØØØ	pin 6 7832	pin 6 7832	pin 6 7832	pin 6 7832
pin 13 617F	pin 7 1H8	pin 7 1H8	pin 7 1H8	pin 7 1H8
pin 14 272U	pin 9 3395	pin 9 3395	pin 9 3395	pin 9 3395
pin 17 C2HP	pin 1Ø 36CC	pin 1Ø 36CC	pin 1Ø 36CC	pin 1Ø 36CC
pin 18 22P6	pin 11 272U	pin 11 272U	pin 11 272U	pin 11 272U
	pin 12 617F	pin 12 617F	pin 12 617F	pin 12 617F
	pin 13 C2HP	pin 13 C2HP	pin 13 C2HP	pin 13 C2HP
	pin 16 ØØØØ	pin 16 ØØØØ	pin 16 ØØØØ	pin 16 ØØØØ

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7D2Ø SIGNATURE TABLE 3.1

A8 U61Ø	A8 U71Ø	A8 U81Ø	A8 U91Ø	A8 U8ØØ
pin 2 4868	pin 2 HF62	pin 2 8F49	pin 2 FFP5	pin 6 C2HP
pin 3 22P6	pin 3 22P6	pin 3 22P6	pin 3 22P6	pin 7 36CC
pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ	pin 9 272U
pin 5 89P3	pin 5 89P3	pin 5 89P3	pin 5 89P3	pin 1Ø 617F
pin 6 7832	pin 6 7832	pin 6 7832	pin 6 7832	
pin 7 1HØ8	pin 7 1HØ8	pin 7 1HØ8	pin 7 1HØ8	
pin 9 3395	pin 9 3395	pin 9 3395	pin 9 3395	
pin 1Ø 36CC	pin 1Ø 36CC	pin 1Ø 36CC	pin 1Ø 36CC	
pin 11 272U	pin 11 272U	pin 11 272U	pin 11 272U	
pin 12 617F	pin 12 617F	pin 12 617F	pin 12 617F	
pin 13 C2HP	pin 13 C2HP	pin 13 C2HP	pin 13 C2HP	
pin 16 ØØØØ	pin 16 ØØØØ	pin 16 ØØØØ	pin 16 ØØØØ	

A8 U1Ø1Ø	A8 U111Ø	A8 U121Ø	A8 U131Ø	A8 U141Ø
pin 4 89P3	pin 4 272U	pin 4 89P3	pin 4 272U	pin 4 89P3
pin 7 1HØ8	pin 7 36CC	pin 7 1HØ8	pin 7 36CC	pin 7 1HØ8
pin 9 7832	pin 9 C2HP	pin 9 7832	pin 9 C2HP	pin 9 7832
pin 12 22P6	pin 12 22P6	pin 12 617F	pin 12 22P6	pin 12 617F

A8 U16ØØ	A8 U17ØØ
pin 4 FFP5	pin 4 2H6A
pin 7 8F49	pin 7 342A
pin 9 HF62	pin 9 U27A
pin 12 4868	pin 12 Ø3PP

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7D2Ø SIGNATURE TABLE 3.2

Firmware Version: 1.Ø2

Diagnostic Invoked: Circuit
Exerciser 432

For Testing: Data Bus

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	3395
Stop	TP-9Ø1*	_	3395
Clock	J41Ø-21B	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 3395
Ground Signature: ØØØØ

A8 U5ØØ	A8 U6ØØ	A8 U7ØØ	A8 U9ØØ	A8 U1ØØØ
pin 1 8F49	pin 1 342A	pin 1 8F49	pin 1 3395	pin 1 U27A
pin 15 FFP5	pin 9 Ø3PP	pin 9 4868	pin 9 FFP5	pin 9 ØØØØ
	pin 1Ø U27A	pin 1Ø HF62	pin 1Ø 3395	pin 1Ø Ø3PP
	pin 15 2H6A	pin 15 FFP5	pin 15 3395	pin 15 342A

A8 U11ØØ	A8 U8ØØ	A8 U16ØØ	A8 U17ØØ	A8 U2ØØ
pin 1 HF62	pin 1 8F49	pin 3 FFP5	pin 3 2H6A	pin 2 8F49
pin 9 2H6A	pin 2 HF62	pin 6 8F49	pin 6 342A	pin 5 HF62
pin 1Ø 4868	pin 3 4868	pin 1Ø HF62	pin 1Ø U27A	pin 6 342A
pin 15 8F49	pin 15 FFP5	pin 13 4868	pin 13 Ø3PP	pin 9 FFP5
				pin 12 4868
				pin 15 2H6A
				pin 16 U27A
				pin 19 Ø3PP

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A8 U3ØØ		A8 U4ØØ	
pin	2 8F49	pin	2 8F49
pin	5 HF62	pin	5 HF62
pin	6 342A	pin	6 342A
pin	9 FFP5	pin	9 FFP5
pin	12 4868	pin	12 4868
pin	15 2H6A	pin	15 2H6A
pin	16 U27A	pin	16 U27A
pin	19 Ø3PP	pin	19 Ø3PP

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7D2Ø SIGNATURE TABLE 4.Ø

Firmware Version: 1.Ø2

Diagnostic Invoked: Circuit
Exerciser 4321

For Testing: Display Address
Generator

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	6PCP
Stop	TP-9Ø1*	_	6PCP
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 6PCP
Ground Signature: ØØØØ

A8 U5ØØ	A8 U6ØØ	A8 U7ØØ	A8 U42Ø	A8 U62Ø
pin 2 1UFP	pin 2 3H46	pin 2 ØP45	pin 1 HCPH	pin 1 C679
pin 3 H32C	pin 3 H8U8	pin 3 1C84	pin 2 H98U	pin 2 6UH8
pin 4 6PCP	pin 4 6PCP	pin 4 6PCP	pin 3 Ø3Ø4	pin 3 6U05
pin 5 ØØØØ	pin 5 ØØØØ	pin 5 ØØØØ	pin 4 ØØØØ	pin 7 ØØØØ
pin 8 ØØØØ	pin 6 6589	pin 6 C5UØ	pin 5 H98U	pin 14 6PCP
pin 11 6U05	pin 7 98C3	pin 7 1C55	pin 6 6PCP	
pin 13 6PCP	pin 8 ØØØØ	pin 8 ØØØØ	pin 7 6PCP	
pin 14 ØØØØ	pin 11 6UH8	pin 11 6UH8	pin 8 ØØØØ	
pin 16 6PCP	pin 12 ØØØØ	pin 12 ØØØØ	pin 9 6PCP	
	pin 13 6PCP	pin 13 6PCP	pin 1Ø C553	
	pin 14 ØØØØ	pin 14 ØØØØ	pin 11 6UH8	
	pin 16 6PCP	pin 16 6PCP	pin 12 6PCP	
			pin 13 6PCP	
			pin 14 6PCP	
			pin 15 Ø3Ø4	
			pin 16 6PCP	

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A8 U92Ø	A8 U1Ø1Ø	A8 U111Ø	A8 U121Ø	A8 U122Ø
pin 4 6PCP	pin 2 98C3	pin 2 H8U8	pin 2 1C84	pin 1 C679
pin 5 6PCP	pin 5 H32C	pin 5 3H46	pin 5 ØP45	pin 2 6H9F
pin 6 ØØØØ	pin 11 1UFP	pin 11 6589	pin 11 C5UØ	pin 3 H98U
pin 7 ØØØØ			pin 14 1C55	pin 4 6PCP
pin 8 6PCP				pin 5 ØØØØ
pin 1Ø ØØØØ				pin 6 4AØP
pin 14 6PCP				pin 7 6PCP
				pin 8 ØØØØ
				pin 9 ØØØØ
				pin 12 ØØØØ
				pin 13 CC1C
				pin 14 C553
				pin 15 6PCP
				pin 16 6PCP

A8 U132Ø
pin 4 6PCP
pin 5 ØØØØ
pin 6 ØØØØ
pin 7 ØØØØ
pin 14 6PCP

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7D2Ø SIGNATURE TABLE 5.Ø

Firmware Version: 1.Ø2

Diagnostic Invoked: Circuit Exerciser 64

For Testing: Acquire Address Generator

On Assembly: A8 Memory

Board Version: 67Ø-7322-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	6F6P
Stop	TP-9Ø1*	_	6F6P
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:
Memory Board on extender

+5 Volt Signature: 6F6P
Ground Signature: ØØØØ

A8 U42Ø	A8 U122Ø	A8 U9ØØ	A8 U1ØØØ	A8 U11ØØ
pin 1 1F46	pin 1 U43H	pin 1 6F6P	pin 2 491P	pin 2 P16C
pin 2 6884	pin 2 53PC	pin 2 98A7	pin 3 66FU	pin 3 H9ØA
pin 3 C891	pin 3 3F7Ø	pin 3 98A7	pin 4 AA2A	pin 4 U4F9
pin 4 ØØØØ	pin 4 ØØØØ	pin 4 ØØØØ	pin 5 ØØØØ	pin 5 ØØØØ
pin 5 3F7Ø	pin 5 6F6P	pin 5 ØØØØ	pin 6 7F47	pin 6 8P1A
pin 6 6F6P	pin 6 2U4H	pin 6 98A7	pin 7 ØØØØ	pin 7 55P9
pin 7 6F6P	pin 7 6F6P	pin 7 99P4	pin 8 ØØØØ	pin 8 ØØØØ
pin 8 ØØØØ	pin 8 ØØØØ	pin 8 ØØØØ	pin 11 U4F9	pin 11 U4F9
pin 9 U4F9	pin 1Ø ØØØØ	pin 1Ø 6F6P	pin 13 6F6P	pin 13 AA2A
pin 1Ø 7Ø28	pin 13 HUPA	pin 11 U4F9	pin 14 FF53	pin 14 FF53
pin 11 6F6P	pin 14 7Ø28	pin 13 U4F9	pin 16 6F6P	pin 16 6F6P
pin 12 6F6P	pin 15 6F6P	pin 14 FF53		
pin 13 AØ3H	pin 16 6F6P	pin 15 6F6P		
pin 14 6F6P		pin 16 6F6P		
pin 15 74F2				
pin 16 6F6P				

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7D2Ø SIGNATURE TABLE 5.Ø

A8 U1Ø1Ø	A8 U1Ø2Ø	A8 U111Ø	A8 U121Ø
pin 3 55P9	pin 1 A03H	pin 3 H9ØA	pin 3 98A7
pin 6 66FU	pin 2 6F6P	pin 6 P16C	pin 6 98A7
pin 8 ØØØØ	pin 5 ØØØØ	pin 8 ØØØØ	pin 8 ØØØØ
pin 1Ø 491P	pin 6 6F6P	pin 1Ø 8P1A	pin 1Ø 98A7
pin 14 ØØØØ	pin 7 ØØØØ	pin 16 6F6P	pin 13 99P4
pin 16 6F6P	pin 12 FF53		pin 16 6F6P
	pin 13 6F6P		
	pin 14 6F6P		

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7D2Ø SIGNATURE TABLE 6.Ø

Firmware Version: 1.Ø2

Diagnostic Invoked: Circuit
Exerciser 6321

For Testing: Time Base
Data Registers

On Assembly: A11 Time Base

Board Version: 67Ø-7325-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	3H18
Stop	TP-9Ø1*	_	3H18
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:

+5 Volt Signature: 3H18
Ground Signature: ØØØØ

A11 U11Ø	A11 U121Ø	A11 U131Ø	A11 U132Ø	A11 U141Ø
pin 8 ØØØØ	pin 1 H13Ø	pin 1 CUØU	pin 1 H13Ø	pin 1 55F3
pin 15 ACF1	pin 2 ACF1	pin 2 CØ18	pin 2 ACF1	pin 2 68HC
pin 16 3H18	pin 8 ØØØØ	pin 3 ACF1	pin 8 ØØØØ	pin 3 4C4Ø
	pin 15 ØØØØ	pin 4 H5U5	pin 1Ø 4186	pin 4 7658
	pin 16 3H18	pin 5 F16A	pin 15 ØØØØ	pin 5 5UHU
		pin 6 HUP9	pin 16 3H18	pin 6 62F7
		pin 7 FC76		pin 7 ØØØØ
		pin 8 ØØØØ		pin 8 HUP9
		pin 9 4186		pin 9 P2U1
		pin 11 5UHU		pin 1Ø 7F44
		pin 12 4C4Ø		pin 11 415F
		pin 13 55F3		pin 12 415F
		pin 14 415F		pin 13 7F44
		pin 15 3H18		pin 14 3H18
		pin 16 3H18		

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A11 U151Ø		A11 U161Ø		A11 U171Ø		A11 U13ØØ		A11 U14ØØ	
pin 1	CU0U	pin 1	CU0U	pin 1	CU0U	pin 3	H8C8	pin 3	2987
pin 2	59P5	pin 2	FCF3	pin 2	3494	pin 4	5519	pin 4	4C4Ø
pin 3	ACF1	pin 3	ACF1	pin 3	ACF1	pin 7	ØØØØ	pin 7	ØØØØ
pin 4	P8PH	pin 4	H5U5	pin 4	P8PH	pin 1Ø	19H2	pin 1Ø	P8PH
pin 5	2987	pin 5	UF72	pin 5	149U	pin 11	ØØØØ	pin 11	9473
pin 6	9473	pin 6	FC76	pin 6	5519	pin 14	3H18	pin 14	3H18
pin 7	5519	pin 7	P2U1	pin 7	A96C				
pin 8	ØØØØ	pin 8	ØØØØ	pin 8	ØØØØ				
pin 9	CØ18	pin 9	59P5	pin 9	FCF3				
pin 11	A426	pin 11	55F3	pin 11	H8C8				
pin 12	654F	pin 12	7F44	pin 12	24FA				
pin 13	H8C8	pin 13	4C4Ø	pin 13	654F				
pin 14	19H2	pin 14	62F7	pin 14	993P				
pin 15	3H18	pin 15	3H18	pin 15	3H18				
pin 16	3H18	pin 16	3H18	pin 16	3H18				

A11 U15ØØ		A11 U16ØØ		A11 U17ØØ	
pin 3	FC76	pin 3	24FA	pin 3	5519
pin 4	H5U5	pin 4	993P	pin 4	P8PH
pin 7	ØØØØ	pin 7	ØØØØ	pin 7	ØØØØ
pin 1Ø	UF72	pin 1Ø	654F	pin 1Ø	149U
pin 11	62F7	pin 11	H8C8	pin 11	A96C
pin 14	3H18	pin 14	3H18	pin 14	3H18

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7D2Ø SIGNATURE TABLE 7.Ø

Firmware Version: 1.Ø2

Diagnostic Invoked: Circuit
Exerciser 641

For Testing: INS, SO, EOA
(flip-flops)

On Assembly: A11 Time Base

Board Version: 67Ø-7325-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	99FA
Stop	TP-9Ø1*	_	99FA
Clock	U132Ø-1	_/	ØØØØ

* on A9 MPU Board

Configuration:

+5 Volt Signature: 99FA
Ground Signature: ØØØØ

A11 U31Ø	A11 U41Ø	A11 U71Ø	A11 U91Ø	A11 U1Ø1Ø
pin 7 ØØØØ	pin 7 ØØØØ	pin 7 ØØØØ	pin 2 ØØØØ	pin 1 Ø7U3
pin 11 3172	pin 8 99FA	pin 8 A5UA	pin 3 Ø43H	pin 2 3172
pin 12 Ø7U3	pin 9 ØØØØ	pin 9 99FA	pin 4 6Ø4A	pin 3 Ø43H
pin 13 AC76	pin 1Ø 99FA	pin 1Ø 3F3Ø	pin 5 A892	pin 7 ØØØØ
pin 14 99FA	pin 14 99FA	pin 14 99FA	pin 6 3158	pin 11 A5UA
			pin 7 A97C	pin 12 A5UA
			pin 8 ØØØØ	pin 13 A5UA
			pin 9 32CF	pin 14 99FA
			pin 1Ø 9P39	
			pin 11 3172	
			pin 12 ØØØØ	
			pin 14 A5UA	
			pin 15 A5UA	
			pin 16 99FA	

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7D2Ø SIGNATURE TABLE 7.Ø

A11 U11ØØ		A11 U112Ø		A11 U12ØØ		A11 U141Ø		A11 U13ØØ	
pin 1	U98Ø	pin 1	3172	pin 2	ØØØØ	pin 7	ØØØØ	pin 1	99FA
pin 2	9P39	pin 2	A8C8	pin 3	ØØØØ	pin 1Ø	Ø7U3	pin 7	ØØØØ
pin 3	6Ø4A	pin 3	99FA	pin 4	99FA	pin 11	9P39	pin 12	3172
pin 7	ØØØØ	pin 7	ØØØØ	pin 5	3172	pin 12	9P39	pin 13	A5UA
pin 14	99FA	pin 14	99FA	pin 6	A8C8	pin 13	Ø7U3	pin 14	99FA
				pin 7	A8C8	pin 14	99FA		
				pin 8	ØØØØ				
				pin 9	3172				
				pin 1Ø	99FA				
				pin 11	3172				
				pin 12	ØØØØ				
				pin 14	A5UA				
				pin 15	A5UA				
				pin 16	99FA				

A11 U14ØØ		A11 U15ØØ		A11 U16ØØ		A11 U17ØØ	
pin 1	99FA	pin 1	99FA	pin 1	99FA	pin 1	99FA
pin 7	ØØØØ	pin 7	ØØØØ	pin 7	ØØØØ	pin 7	ØØØØ
pin 13	A5UA	pin 13	A5UA	pin 13	A5UA	pin 13	A5UA
pin 14	99FA	pin 14	99FA	pin 14	99FA	pin 14	99FA

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7D2Ø SIGNATURE TABLE 8.Ø

Firmware Version: 1.Ø1

Diagnostic Invoked: Circuit Exerciser 6431

For Testing: Preamplifier Data Registers

On Assembly: A4 Preamplifier

Board Version: 67Ø-7318-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	3H18
Stop	TP-9Ø1*	_	3H18
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:

+5 Volt Signature: 3H18
Ground Signature: ØØØØ

A4 U3ØØ		A4 U123Ø		A4 U34Ø		A4 U91Ø		A4 U93Ø	
pin 1	CUØU	pin 1	CUØU	pin 9	H8C8	pin 3	F16A	pin 3	FC76
pin 2	46A2	pin 2	3494	pin 1Ø	A426	pin 5	H5U5	pin 5	HUP9
pin 3	8HF9	pin 3	8HF9	pin 11	5854				
pin 4	P8PH	pin 4	H5U5						
pin 5	149U	pin 5	F16A						
pin 6	68Ø1	pin 6	HUP9						
pin 7	9473	pin 7	FC76						
pin 8	ØØØØ	pin 8	ØØØØ						
pin 9	8C29	pin 9	46A2						
pin 11	24FA	pin 11	5UHU						
pin 12	H8C8	pin 12	4C4Ø						
pin 13	A426	pin 13	55F3						
pin 14	5854	pin 14	415F						
pin 15	3H18	pin 15	3H18						
pin 16	3H18	pin 16	3H18						

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7D2Ø SIGNATURE TABLE 9.Ø

Firmware Version: 1.Ø1

Diagnostic Invoked: Circuit Exerciser 6431

For Testing: Trigger Data Registers

On Assembly: AlØ Trigger

Board Version: 67Ø-7324-ØØ

Signature Analyzer Setup:

	connect	edge	signature
Start	TP-9ØØ*	_/	3H18
Stop	TP-9Ø1*	_	3H18
Clock	TP-9Ø2*	_/	ØØØØ

* on A9 MPU Board

Configuration:
Trigger Board on extender

+5 Volt Signature: 3H18
Ground Signature: ØØØØ

A1Ø U1Ø1	A1Ø U2ØØ	A1Ø U2Ø1	A1Ø U21Ø	A1Ø U3ØØ
pin 4 HCP7	pin 1 CUØU	pin 1 CUØU	pin 1 CUØU	pin 6 A96C
pin 5 F13A	pin 2 3944	pin 2 32C4	pin 2 3494	pin 8 ØØØØ
pin 7 ØØØØ	pin 3 P6UU	pin 3 P6UU	pin 3 P6UU	pin 9 ØØØØ
pin 8 993P	pin 4 H5U5	pin 4 P8PH	pin 4 H5U5	pin 1Ø 68Ø1
pin 9 3H18	pin 5 F16A	pin 5 2987	pin 5 UF72	pin 11 P5AØ
pin 1Ø A426	pin 6 P2U1	pin 6 A96C	pin 6 U66P	pin 15 ØØØØ
pin 11 HCP7	pin 7 U66P	pin 7 68Ø1	pin 7 HUP9	pin 16 3H18
pin 12 3H18	pin 8 ØØØØ	pin 8 ØØØØ	pin 8 ØØØØ	
pin 13 P6UU	pin 9 F13A	pin 9 3944	pin 9 32C4	
pin 14 3H18	pin 11 4C4Ø	pin 1Ø P1AU	pin 11 7F44	
	pin 12 5UHU	pin 11 654F	pin 12 55F3	
	pin 13 7F44	pin 12 A426	pin 13 5UHU	
	pin 14 68HC	pin 13 24FA	pin 14 7658	
	pin 15 3H18	pin 14 P5AØ	pin 15 3H18	
	pin 16 3H18	pin 15 3H18	pin 16 3H18	
		pin 16 3H18		

A1Ø U31Ø
pin 5 7F44
pin 6 55F3
pin 7 5UHU
pin 8 7658
pin 9 HUP9
pin 1Ø U66P
pin 11 UF72
pin 12 H5U5

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REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 *Name & Description*

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

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CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000CX	N W SPRING AND MANUFACTURING COMPANY	5525 ROSEWOOD STREET	LAKE OSWEGO, OR 97034
000EN	EDWIN B. STIMPSON CO.	1515 S.W. 13TH COURT	POMPANO BEACH, FLA 33060
000EO	ZEPHER ELECTRONIC SALES CORP.	647 INDUSTRY DRIVE	SEATTLE, WA 98188
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
05820	WAKEFIELD ENGINEERING, INC.	AUDUBON ROAD	WAKEFIELD, MA 01880
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
13511	AMPHENOL CARDRE DIV., BUNKER RAMO CORP.		LOS GATOS, CA 95030
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
24931	SPECIALITY CONNECTOR CO., INC.	2620 ENDRESS PLACE	GREENWOOD, IN 46142
26365	GRIES REPRODUCER CO., DIV. OF COATS AND CLARK, INC.	125 BEECHWOOD AVE.	NEW ROCHELLE, NY 10802
29587	BUNKER-RAMO CORP., AMPHENOL INDUSTRIAL DIV.	1830 S. 54TH AVE.	CHICAGO, IL 60650
49671	RCA CORPORATION	30 ROCKEFELLER PLAZA	NEW YORK, NY 10020
71159	BRISTOL SOCKET SCREW, DIV. OF AMERICAN CHAIN AND CABLE CO., INC.	P O BOX 2244, 40 BRISTOL ST.	WATERBURY, CT 06720
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
77900	SHAKEPROOF DIV OF ILLINOIS TOOL WORKS	SAINT CHARLES RD	ELGIN, IL 60120
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
86928	SEASTROM MFG. COMPANY, INC.	701 SONORA AVENUE	GLENDALE, CA 91201
92101	SCHULZE MFG, 50 INGOLD RD BURLINGAME, CA 94010		
93907	TEXTRON INC. CAMCAR DIV	600 18TH AVE	ROCKFORD, IL 61101
95238	CONTINENTAL CONNECTOR CORP.	34-63 56TH ST.	WOODSIDE, NY 11377
95987	WECKESSER CO., INC.	4444 WEST IRVING PARK RD.	CHICAGO, IL 60641
T0435	LEWIS SCREW CO.	4114 SOUTH PERORIA AVE.	CHICAGO, IL 60609

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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
1-1	337-1064-04	B010100	B050799	2	SHIELD,ELEC:SIDE PLUG-IN UNITS	80009	337-1064-00
	337-1064-12	B050800		2	SHIELD,ELEC:SIDE FOR PLUG-IN UNIT	80009	337-1064-12
-2	366-1189-05			3	KNOB:FLINT GRAY	80009	366-1189-05
	213-0246-00			3	.SETSCREW:5-40 X 0.093 ITL BK OXD,HEX	71159	ORD BY DESCR
-3	366-1189-04			2	KNOB:FLINT GRAY,CAL	80009	366-1189-04
	213-0246-00			2	.SETSCREW:5-40 X 0.093 ITL BK OXD,HEX	71159	ORD BY DESCR
-4	366-2024-00			2	KNOB:GRAY,VOLTS DIVISION	80009	366-2024-00
	213-0246-00			2	.SETSCREW:5-40 X 0.093 ITL BK OXD,HEX	71159	ORD BY DESCR
-5	366-1023-12			1	KNOB:FLINT GRAY	80009	366-1023-12
	213-0246-00			1	.SETSCREW:5-40 X 0.093 ITL BK OXD,HEX	71159	ORD BY DESCR
-6	366-2025-00			1	KNOB:GRAY,TIME DIVISION	80009	366-2025-00
	213-0246-00			2	.SETSCREW:5-40 X 0.093 ITL BK OXD,HEX	71159	ORD BY DESCR
-7	358-0301-02			7	BUSHING,SLEEVE:GRAY PLASTIC	80009	358-0301-02
-8	200-2803-00			1	COVER,GPIB:POLYCARBONATE	80009	200-2803-00
-9	333-2841-00			1	PANEL,FRONT::	80009	333-2841-00
					**********(ATTACHING PARTS)**********		
-10	210-0586-00			6	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	T0435	ORD BY DESCR
					**********(END ATTACHING PARTS)*********		
-11	386-4733-01			1	SUBPANEL,FRONT:	80009	386-4733-01
					**********(ATTACHING PARTS)**********		
-12	211-0541-00			8	SCREW,MACHINE:6-32 X 0.25"100 DEG,FLH STL	83385	ORD BY DESCR
-13	210-0457-00			1	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)*********		
-14	348-0235-00			2	SHLD GSKT,ELEC:4.734 INCH LONG	92101	ORD BY DESCR
-15	131-1315-01			1	CONN,RCPT,ELEC:BNC,FEMALE	24931	28JR 306-1
-16	210-0012-00			1	WASHER,LOCK:INTL,0.384 ID,INTL,0.022 TH	78189	1220-02-00-0541C
-17	131-0955-00			1	CONN,RCPT,ELEC:BNC,FEMALE	13511	31-279
-18	210-0255-00			1	TERMINAL,LUG:0.391 ID,LOCKING,BRS CD PL	80009	210-0255-00
-19	105-0922-00			1	RELEASE,LATCH:PLUG-IN UNIT	80009	105-0922-00
-20	366-2023-01			1	KNOB:GRAY	80009	366-2023-01
-21	----- -----			1	RESISTOR,VAR:(SEE R10,R20 REPL)		
					**********(ATTACHING PARTS)**********		
-22	210-0583-00			2	NUT,PLAIN,HEX:0.25-32 X 0.312 INCH,BRS	73743	2X20317-402
-23	210-0046-00			2	WASHER,LOCK:0.261 ID,INTL,0.018 THK,BRS	77900	1214-05-00-0541C
					**********(END ATTACHING PARTS)*********		
-24	214-3386-00			1	SPRING,HLEXT:2.4 INCH LONG,,MUSIC WIRE	000CX	ORD BY DESCR
-25	214-3369-00			3	SPRING,GROUND:	80009	214-3369-00
	210-0773-00			2	EYELET,METALLIC:0.152 OD X 0.125 LONG	000EN	ORD BY DESCR
-27	----- -----			1	CKT BOARD ASSY:LED(SEE A2 REPL)		
					**********(ATTACHING PARTS)**********		
-28	211-0017-00			4	SCREW,MACHINE:4-40 X 0.750 PNH,STL CD PL	83385	ORD BY DESCR
-29	211-0008-00			2	SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)*********		
	----- -----			-	CKT BOARD ASSY INCLUDES:		
-30	131-0589-00			13	.TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
-31	131-0787-00			38	.TERMINAL,PIN:0.64LX0.025SQ PH BRZ,GOLD	22526	47359-000
-32	131-0608-00			40	.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
-33	175-7287-00			2	CA ASSY,SP,ASSY:12 COND,0.425 INCH LONG	80009	175-7287-00
-34	131-0346-00			1	CONNECTOR,RCPT,:	29587	57-20240 398
					**********(ATTACHING PARTS)**********		
-35	129-0922-00	B010100	B019999	2	.SPACER,POST:0.71,W/6-32 THD ONE END,AL	80009	129-0922-00
	129-1003-00	B020000		2	.SPACER,POST:0.705 L,6-32 EXT THD ONE		ORD BY DESCR
					.**********(END ATTACHING PARTS)*********		
-36	361-0146-00			2	.SPACER,SLEEVE:0.148 L X 0.18 ID,BRS CU-SN	80009	361-0146-00
-37	407-2855-00			1	.BRACKET,CONN:GPIB	80009	407-2855-00
-38	----- -----			2	.RESISTOR,VAR:(SEE A2R100,A2R130 REPL)		
					.**********(ATTACHING PARTS)**********		
-39	210-0583-00			2	.NUT,PLAIN,HEX:0.25-32 X 0.312 INCH,BRS	73743	2X20317-402
-40	210-0046-00			2	.WASHER,LOCK:0.261 ID,INTL,0.018 THK,BRS	77900	1214-05-00-0541C
					.**********(END ATTACHING PARTS)*********		
-41	----- -----			2	.RESISTOR,VAR:(SEE A2R600,A2R630 REPL)		
					.**********(ATTACHING PARTS)**********		
-42	210-0583-00			2	.NUT,PLAIN,HEX:0.25-32 X 0.312 INCH,BRS	73743	2X20317-402
-43	210-0046-00			2	.WASHER,LOCK:0.261 ID,INTL,0.018 THK,BRS	77900	1214-05-00-0541C
					.**********(END ATTACHING PARTS)*********		

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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
1-44	214-3398-00			1	SPRING,GROUND:POTS	80009	214-3398-00
					**********(ATTACHING PARTS)**********		
-45	210-0583-00			5	NUT,PLAIN,HEX:0.25-32 X 0.312 INCH,BRS	73743	2X20317-402
-46	210-0046-00			5	WASHER,LOCK:0.261 ID,INTL,0.018 THK,BRS	77900	1214-05-00-0541C
					**********(END ATTACHING PARTS)**********		
-47	175-4548-00			1	CA ASSY,SP,ELEC:40,28 AWG,6.0 L,RIBBON	000EO	ORD BY DESCR
-48	214-3418-00			2	SPRING,GROUND:VARIABLE RESISTOR	80009	214-3418-00
-49	210-1098-00			1	WASHER,FLAT:0.219 ID X 0.01 THK,NYL	80009	210-1098-00
-50	----- -----			1	CKT BOARD ASSY:SWITCH(SEE A1 REPL)		
					**********(ATTACHING PARTS)**********		
-51	211-0008-00			1	SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
	----- -----			-	CKT BOARD ASSY INCLUDES:		
	----- -----			1	.SWITCH,ROTARY:TIME/DIV(SEE A1S430 REPL)		
-52	213-0759-00			3	..SCR,TPG,THD FOR:2-28 X 0.437 INCH,PNH,ST	93907	ORD BY DESCR
-53	401-0340-01			1	..BEARING,RTRY SW:FRONT,0.375 DIA	80009	401-0340-01
-54	214-1127-00			2	..ROLLER,DETENT:0.125 DIA X 0.125,SST	80009	214-1127-00
-55	214-1126-01			2	..SPRING,FLAT:0.7 X 0.125,CU BE GRN CLR	80009	214-1126-01
-56	384-1623-01			1	..SHAFT,ROTARY SW:28 POSN,1.44 INCH LONG	80009	384-1623-01
-57	352-0457-21			1	..HOLDER,CONTACT:PANCAKE SW,4 CONTACT	80009	352-0457-21
-58	352-0457-44			1	..HOLDER,CONTACT:PANCAKE SW,1 CONTACT	80009	352-0457-44
-59	401-0341-01			1	..BEARING,RTRY SW:REAR,0.252 ID	80009	401-0341-01
-60	136-0263-04			25	.SOCKET,PIN TERM:FOR 0.025 INCH SQ PIN	22526	75377-001
	----- -----			2	.SWITCH,ROTARY:CHAN 1 & 2(SEE A1S100,		
	----- -----			-	.A1S130 REPL)		
-61	213-0759-00			6	..SCR,TPG,THD FOR:2-28 X 0.437 INCH,PNH,ST	93907	ORD BY DESCR
-62	401-0340-01			2	..BEARING,RTRY SW:FRONT,0.375 DIA	80009	401-0340-01
-63	214-1127-00			4	..ROLLER,DETENT:0.125 DIA X 0.125,SST	80009	214-1127-00
-64	214-1126-01			4	..SPRING,FLAT:0.7 X 0.125,CU BE GRN CLR	80009	214-1126-01
-65	384-1623-02			2	..SHAFT,ROTARY SW:16/10 POSN,1.44 INCH LON	80009	384-1623-02
-66	352-0457-36			4	..HOLDER,CONTACT:1 CONTACT,GRAY PC	80009	352-0457-36
-67	401-0341-01			2	..BEARING,RTRY SW:REAR,0.252 ID	80009	401-0341-01
-68	131-0787-00			38	.TERMINAL,PIN:0.64LX0.025SQ PH BRZ,GOLD	22526	47359-000
-69	----- -----			1	CKT BOARD ASSY:INTERCONNECT(SEE A3 REPL)		
					**********(ATTACHING PARTS)**********		
-70	211-0008-00			1	SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
	----- -----			-	CKT BOARD ASSY INCLUDES:		
-71	131-2724-00			2	.CONN,RCPT,ELEC:CKT BOD,2 X 5.0	22526	67117-005
-72	131-1633-00			1	.CONNECTOR,RCPT,:CKT CARD MTG	22526	65001-009
-73	131-2843-00			7	.CONN,RCPT,ELEC:EDGECARD,2 X 36,0.1 SPACIN	95238	K60012172DD1630N
-74	131-0608-00			48	.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
-75	343-0003-00			2	CLAMP,LOOP:0.25 ID,PLASTIC	95987	1-4-6B
					**********(ATTACHING PARTS)**********		
-76	210-0586-00			2	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	T0435	ORD BY DESCR
-77	210-0863-00			2	WSHR,LOOP CLAMP:0.187 ID U/W 0.5 W CLP,STL	95987	C191
-78	211-0102-00			2	SCREW,MACHINE:4-40 X 0.50,FLH,100 DEG STL	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
-79	210-0202-00			4	TERMINAL,LUG:0.146 ID,LOCKING,BRZ,TIN PL	86928	A-373-158-2
					**********(ATTACHING PARTS)**********		
-80	210-0586-00			4	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	T0435	ORD BY DESCR
-81	211-0025-00			4	SCREW,MACHINE:4-40 X 0.375 100 DEG,FLH ST	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
-82	214-3286-00			1	CATCH,LEVER:PLASTIC	80009	214-3286-00
-83	214-1054-00			2	SPRING,FLAT:0.825 X 0.322,SST	80009	214-1054-00
-84	214-1061-00			1	SPRING,GROUND:FLAT	80009	214-1061-00
-85	337-2955-00			1	SHIELD,ELEC:PREAMP	80009	337-2955-00
					**********(ATTACHING PARTS)**********		
-86	211-0292-00			2	SCR,ASSEM WSHR:4-40 X 0.29,BRS NI PL	78189	51-040445-01
					**********(END ATTACHING PARTS)**********		
	----- -----			-	SHIELD INCLUDES:		
-87	344-0132-00			2	.CLIP,ELECTRICAL:MOLDED PLSTC	80009	344-0132-00

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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-88	----- -----			-		ATTENUATOR,VAR:(SEE A12,A13 REPL)		
						**********(ATTACHING PARTS)**********		
-89	211-0016-00			4		SCREW,MACHINE:4-40 X 0.625 INCH,PNH STL	83385	ORD BY DESCR
-90	361-0154-00			4		SPACER,SLEEVE:	80009	361-0154-00
-91	129-0940-00			4		SPACER,POST:0.490 L X 0.188 HEX	80009	129-0940-00
-92	210-0994-00			2		WASHER,FLAT:0.125 ID X 0.25" OD,STL	86928	5702-201-20
-93	210-0586-00			4		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	T0435	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
	----- -----			-		ATTENUATOR ASSY INCLUDES:		
-94	200-2695-00			2		.COVER,ATTEN:	80009	200-2695-00
-95	407-2891-00			1		BRACKET,ANGLE:ATTENUATORS	80009	407-2891-00
-96	386-4750-00			3		SUPPPRT,CKT BD:UPPER	80009	386-4750-00
						**********(ATTACHING PARTS)**********		
-97	211-0025-00	B010100	B020189	3		SCREW,MACHINE:4-40 X 0.375 100 DEG,FLH ST	83385	ORD BY DESCR
	213-0012-00	B020190		3		SCREW,MACHINE:4-40 X 0.375 INCH,FLH STL	83385	ORD BY DESCR
-98	213-0107-00			3		SCR,TPG,THD FOR:4-40 X 0.25 INCH,FLH STL	93907	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-99	----- -----			1		CKT BOARD ASSY:VERT PRE-AMP(SEE A4 REPL)		
						**********(ATTACHING PARTS)**********		
-100	211-0008-00			1		SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
-101	136-0263-04			4		.SOCKET,PIN TERM:FOR 0.025 INCH SQ PIN	22526	75377-001
-102	131-0589-00			32		.TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
-103	136-0727-00			2		.SKT,PL-IN ELEK:MICROCKT,8 CONTACT	09922	DILB8P-108
-104	136-0729-00			2		.SKT,PL-IN ELEK:MICROCKT,16 CONTACT	09922	DILB16P-108T
-105	131-0608-00			6		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
-106	131-1003-00			6		.CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
-107	136-0252-07			44		.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-108	214-0579-00			11		.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
	200-1673-00			2		.COVER,XSTR:TEMP STAB,S-SHAPED	05820	ORD BY DESCR
-109	386-1556-00			22		SUPPORT,CKT BD:0.215 H,ACETAL	80009	386-1556-00
-110	337-2988-00			1		SHIELD,ELEC:CIRCUIT BOARD	80009	337-2988-00
-111	----- -----			1		CKT BOARD ASSY:CCD(SEE A5 REPL)		
						**********(ATTACHING PARTS)**********		
-112	211-0008-00			2		SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
-113	214-0579-00			12		.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-114	136-0756-00			1		.SKT,PL-IN ELEK:MICROCIRCUIT,18 DIP	09922	DILB18P-108
-115	136-0729-00			2		.SKT,PL-IN ELEK:MICROCKT,16 CONTACT	09922	DILB16P-108T
-116	131-1003-00			4		.CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
-117	136-0252-07			4		.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-118	----- -----			16		.TERMINAL,PIN:(SEE J100,1051,		
	----- -----			-		.(P420,P480,P510 REPL)		
	131-0993-00	B050484		2		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-119	214-3335-00			1		.HT SK,MICROCKT:	80009	214-3335-00
						.**********(ATTACHING PARTS)**********		
-120	211-0036-00			1		.SCREW,MACHINE:4-40 X 0.500,BDGH,NYL,SLOT	26365	ORD BY DESCR
						.**********(END ATTACHING PARTS)*********		
-121	337-2987-00			1		.SHIELD,ELEC:CIRCUIT BOARD	80009	337-2987-00
-122	----- -----			1		CKT BOARD ASSY:DISPLAY(SEE A6 REPL)		
-123	214-0579-00			11		.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-124	337-2954-00			1		SHIELD,ELEC:POWER SUPPLY	80009	337-2954-00
						**********(ATTACHING PARTS)**********		
-125	211-0008-00			3		SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-126	----- -----			1		CKT BOARD ASSY:POWER SUPPLY(SEE A7 REPL)		
-127	131-0608-00			2		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
-128	214-0579-00			6		.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-129	----- -----			1		.TRANSISTOR:(SEE A7Q330 REPL)		
						.**********(ATTACHING PARTS)**********		
-130	210-0406-00			1		.NUT,PLAIN,HEX:4-40 X 0.188,BRS,CD PL	73743	12161-50
-131	211-0008-00			1		.SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
-132	210-1178-00			1		.WASHER,SHLDR:U/W T0-220 TRANSISTOR	49671	DF 137A
						.**********(END ATTACHING PARTS)*********		

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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-133	361-0105-00			3		.SPACER,POST:0.188 OD X 0.775 INCH LONG	80009	361-0105-00
						.**********(ATTACHING PARTS)**********		
-134	211-0008-00			3		.SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
						.**********(END ATTACHING PARTS)*********		
-135	----- -----			-		.TRANSISTOR:(SEE A7Q650 REPL)		
						.**********(ATTACHING PARTS)**********		
-136	210-0406-00			1		.NUT,PLAIN,HEX:4-40 X 0.188,BRS,CD PL	73743	12161-50
-137	211-0008-00			3		.SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
-138	210-1178-00			1		.WASHER,SHLDR:U/W T0-220 TRANSISTOR	49671	DF 137A
						.**********(END ATTACHING PARTS)*********		
-139	----- -----			1		.MICROCIRCUIT:(SEE A7U220 REPL)		
						.**********(ATTACHING PARTS)**********		
-140	210-0406-00			1		.NUT,PLAIN,HEX:4-40 X 0.188,BRS,CD PL	73743	12161-50
-141	211-0008-00			1		.SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
-142	210-1178-00			1		.WASHER,SHLDR:U/W T0-220 TRANSISTOR	49671	DF 137A
						.**********(END ATTACHING PARTS)*********		
-143	----- -----			1		CKT BOARD ASSY:MEMORY(SEE A8 REPL)		
-144	214-0579-00			12		.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-145	----- -----			1		CKT BOARD ASSY:M.P.U.(SEE A9 REPL)		
						**********(ATTACHING PARTS)**********		
-146	211-0008-00			2		SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
	----- -----			-		.CKT BOARD ASSY INCLUDES:		
-147	214-0579-00			14		.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-148	136-0757-00			1		.SKT,PL-IN ELEK:MICROCKT,40 PIN	09922	DILB40P-108
-149	136-0751-00			3		.SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
-150	136-0755-00			6		.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-151	131-0993-00			16		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-152	131-0608-00			34		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
-153	136-0756-00			1		.SKT,PL-IN ELEK:MICROCIRCUIT,18 DIP	09922	DILB18P-108
-154	337-3043-00			1		SHIELD,ELEC:CIRCUIT BOARD	80009	337-3043-00
-155	----- -----			1		CKT BOARD ASSY:TRIGGER(SEE A10 REPL)		
-156	214-0579-00			6		.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-157	131-1003-00			3		.CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
-158	136-0252-07			3		.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-159	136-0752-00			1		.SKT,PL-IN ELEK:MICROCIRCUIT,20 DIP	09922	DILB20P-108
-160	131-0993-00			1		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-161	131-0608-00			29		TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
-162	131-0589-00			8		.TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
-163	----- -----			1		CKT BOARD ASSY:TIME BASE(SEE A11 REPL)		
						**********(ATTACHING PARTS)**********		
-164	211-0292-00			2		SCR,ASSEM WSHR:4-40 X 0.29,BRS NI PL	78189	51-040445-01
						**********(END ATTACHING PARTS)*********		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
-165	136-0252-07			3		.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-166	214-0579-00			22		.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
	131-0993-00	B050596		2		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-167	351-0217-00			3		GUIDE,CKT CARD:PLASTIC	80009	351-0217-00
						**********(ATTACHING PARTS)**********		
-168	220-0557-00			12		NUT,SLEEVE:6-32 X 0.204 OD X 0.118 L B	80009	220-0557-00
-169	211-0507-00			12		SCREW,MACHINE:6-32 X 0.312,PNH STL,CD PL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-170	343-0213-00			1		CLAMP,LOOP:0.2 ID,PLASTIC	80009	343-0213-00
-171	333-2847-00			1		PANEL,REAR:	80009	333-2847-00
						**********(ATTACHING PARTS)**********		
-172	213-0793-00			8		SCREW,TPG,TF:6-32 X 0.4375,TAPTITE,FIL	93907	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-173	361-0326-00			1		SPACER,SLEEVE:0.18 ID X 0.25 OD X 0.10"L	80009	361-0326-00
-174	210-0202-00			1		TERMINAL,LUG:0.146 ID,LOCKING,BRZ,TIN PL	86928	A-373-158-2
						**********(ATTACHING PARTS)**********		
-175	210-0586-00			1		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	T0435	ORD BY DESCR
-176	211-0106-00			1		SCREW,MACHINE:4-40 X 0.625"100 DEG,FLH,ST	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		

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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
1-177	426-1874-00			1	FR SECT,PLUG-IN:UPPER LEFT	80009	426-1874-00
-178	210-0202-00			1	TERMINAL,LUG:0.146 ID,LOCKING,BRZ,TIN PL	86928	A-373-158-2
					**********(ATTACHING PARTS)**********		
-179	211-0007-00			1	SCREW,MACHINE:4-40 X 0.188,PNH STL,CD PL	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)*********		
-180	426-1873-00			1	FR SECT,PLUG-IN:UPPER RIGHT	80009	426-1873-00
-181	220-0912-00			1	NUT BLOCK:0.56 X 0.312,4-40 THD THRU	80009	220-0912-00
-182	386-4751-00			1	SUPPORT,CKT BD:LOWER	80009	386-4751-00
					**********(ATTACHING PARTS)**********		
-183	211-0101-00			2	SCREW,MACHINE:4-40 X 0.25,FLH,100 DEG,STL	83385	ORD BY DESCR
-184	211-0025-00	B010100	B020189	3	SCREW,MACHINE:4-40 X 0.375 100 DEG,FLH ST	83385	ORD BY DESCR
	213-0012-00	B020190		3	SCREW,MACHINE:4-40 X 0.375 INCH,FLH STL	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)*********		
-185	426-1875-00			1	FR SECT,PLUG-IN:LOWER LEFT	80009	426-1875-00
-186	426-1876-00			1	FR SECT,PLUG-IN:LOWER RIGHT	80009	426-1876-00
	198-4665-00			1	WIRE SET,ELEC:	80009	198-4665-00
	175-4979-00			1	.CA ASSY,SP,ELEC:RIBBON,11.0 INCH LONG	80009	175-4979-00
	----- -----			-	.(TIME BASE CKT BD TO CH1 POSITION POT)		
	352-0161-02			1	..CONN BODY,PL,EL:3 WIRE RED	80009	352-0161-02
	175-4980-00			1	.CA ASSY,SP,ELEC:RIBBON,10.0 INCH LONG	80009	175-4980-00
	----- -----			-	.(TIME BASE CKT BOARD TO CH2 POSITION POT)		
	352-0163-03			1	..HLDR,TERM CONN:5 WIRE,ORANGE	80009	352-0163-03
	175-4477-00			1	.CA ASSY,SP,ELEC:2,26 AWG,7.0 L,RIBBON	80009	175-4477-00
	----- -----			-	.(TIME BASE CKT BD TO FRONT PANEL EXTERNAL		
	----- -----			-	.CLOCK BNC)		
	352-0161-01			1	..CONN BODY,PL,EL:3 WIRE BROWN	80009	352-0161-01
	198-4666-00			1	WIRE SET,ELEC:	80009	198-4666-00
	175-2929-00			1	.CABLE ASSY,RF:50 OHM COAX,18.0 INCH LONG	80009	175-2929-00
	----- -----			-	.(TRIGGER BD TO PRE AMP BD)		
	175-4329-00			1	.CABLE ASSY,RF:50 OHM COAX,7.0 L,9-2	80009	175-4329-00
	----- -----			-	.(CCD CKT BD TO PREAMP BD)		
	175-4974-00			1	.CABLE ASSY,RF:50 OHM COAX,7.0 INCH LONG	80009	175-4974-00
	----- -----			-	.(CCD CKT BD TO PREAMP BD)		
	175-4975-00			1	.CABLE ASSY,RF:50 OHM COAX,7.0 INCH LONG	80009	175-4975-00
	----- -----			-	.(CCD CKT BD TO PREAMP BD)		
	175-4976-00			1	.CABLE ASSY,RF:50 OHM COAX,7.0 INCH LONG	80009	175-4976-00
	----- -----			-	.(CCD CKT BD TO PREAMP BD)		
	175-4977-00			1	.CABLE ASSY,RF:50 OHM COAX,18.0 INCH LONG	80009	175-4977-00
	----- -----			-	.(TRIGGER BD TO PREAMP BD)		
	175-4978-00			1	.CABLE ASSY,RF:50 OHM COAX,4.0 INCH LONG	80009	175-4978-00
	----- -----			-	.(FRONT PANEL EXTERNAL TRIGGER BNC		
	----- -----			-	.TO TRIGGER BD)		

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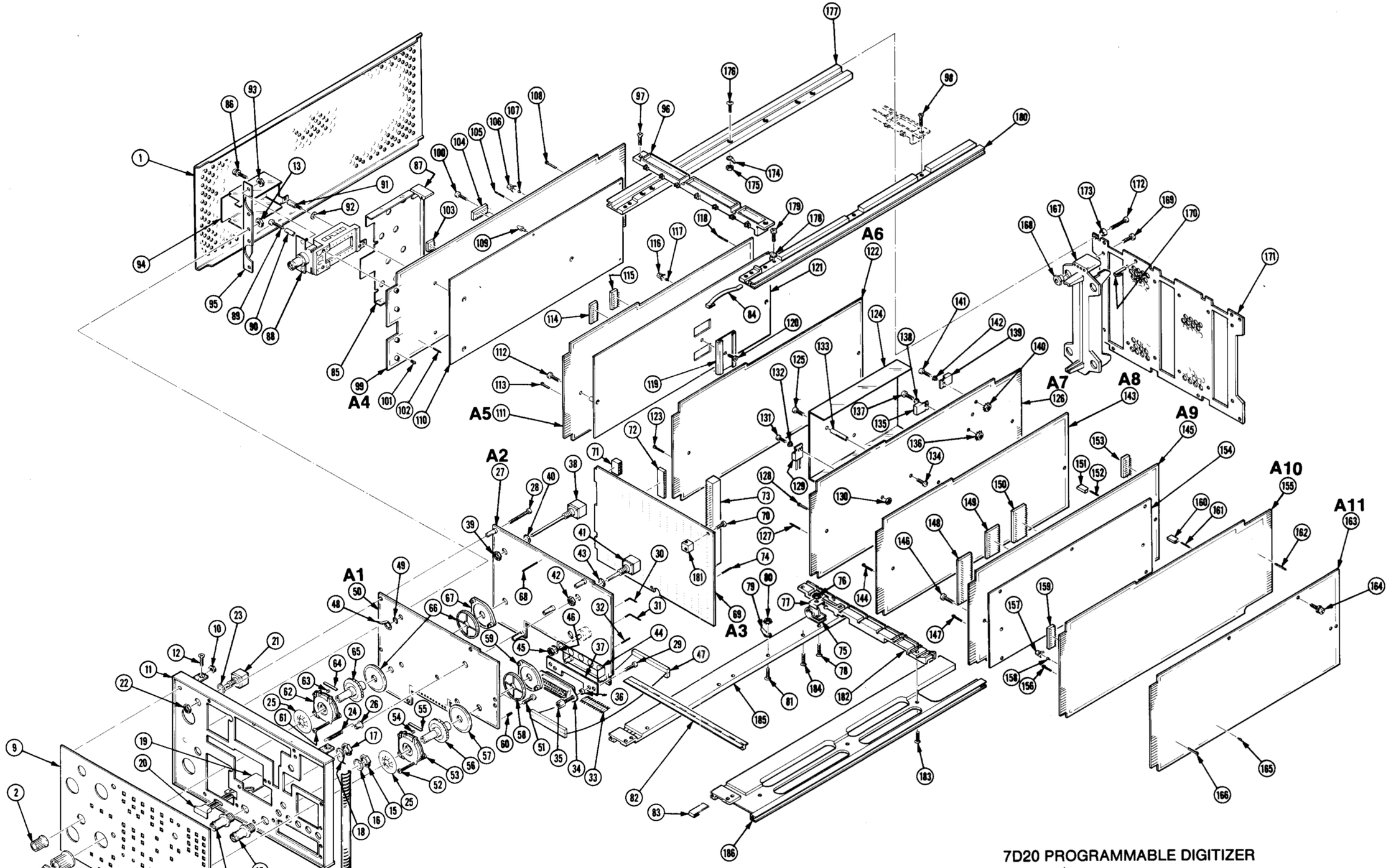

7D20 PROGRAMMABLE DIGITIZER

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Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
					STANDARD ACCESSORIES		
070-3857-01			1		MANUAL,TECH:OPERATORS	80009	070-3857-01
070-3858-01			1		MANUAL,TECH:SERVICE	80009	070-3858-01
070-1728-00			4		MANUAL,TECH:GUIDE	80009	070-1728-00
070-3205-01			1		MANUAL,TECH:REF,7D20	80009	070-3205-01
					OPTIONAL ACCESSORIES		
067-0616-00			1		FIXTURE,CAL:PLUG-IN EXTENDER	80009	067-0616-00
067-1051-00			1		FIXTURE,CAL:EXTENDER BOARD	80009	067-1051-00
020-0903-00			1		ACCESSORY KIT:	80009	020-0903-00

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MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

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MANUAL CHANGE INFORMATION

Date: 8/5/85 **Change Reference:** M56091

Product: 7D20 Programmable Digitizer **Manual Part No.:** 070-3858-01

DESCRIPTION Manual Insert for Product Group 42

These changes are effective at serial number B063949.

REPLACEABLE ELECTRICAL PARTS LIST CHANGES

CHANGE TO:

A5	670-7319-03	CKT BOARD ASSY:CCD
A5CR520	152-0322-00	SEMICOND DEVICE:SILICON,15V,HOT CARRIER
A5CR530	152-0322-00	SEMICOND DEVICE:SILICON,15V,HOT CARRIER
A5CR531	152-0322-00	SEMICOND DEVICE:SILICON,15V,HOT CARRIER
A5CR541	152-0322-00	SEMICOND DEVICE:SILICON,15V,HOT CARRIER
A5CR571	152-0322-00	SEMICOND DEVICE:SILICON,15V,HOT CARRIER
A5CR572	152-0322-00	SEMICOND DEVICE:SILICON,15V,HOT CARRIER
A5CR583	152-0322-00	SEMICOND DEVICE:SILICON,15V,HOT CARRIER
A5CR584	152-0322-00	SEMICOND DEVICE:SILICON,15V,HOT CARRIER

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MANUAL CHANGE INFORMATION

Date: 8/1/85 **Change Reference:** M58546

Product: 7D20 Programmable Digitizer **Manual Part No.:** 070-3858-01

DESCRIPTION Manual Insert for Product Group 42

These changes are effective at serial number B064051.

The following information details changes to the manual made necessary by modifications to the A5 CCD Circuit Board Assembly. Two fixed capacitors have been replaced with variable capacitors and a new procedure for their adjustment has been created.

REPLACEABLE ELECTRICAL PARTS LIST CHANGES

CHANGE TO:

A5C850	281-0158-00	CAP.,VAR,CER DI:7-45PF,50V
A5C851	281-0158-00	CAP.,VAR,CER DI:7-45PF,50V

TEXT CHANGES

Make the following corrections to **TABLE 4-2 Test Equipment**.

2. Test Oscilloscope - Example of Applicable Test Equipment

Change **P6008** to **P6106A**.

Add the following new item.

17. Calibration Fixture; L-shaped circuit board extender; used to extend A5 for component adjustment access; Tektronix part 067-1051-00.

Add the following new step to the **Adjustment Procedure between steps A5 and A6**.

ADJUST INPUT SAMPLING CLOCK (C850, C851)

NOTE

Steps A1, A3, A4, and A5 must be performed before performing this step. This step should be repeated after replacement of either CCD (A5U440 or A5U460).

a. Perform step A2 Initialization procedure, then proceed.

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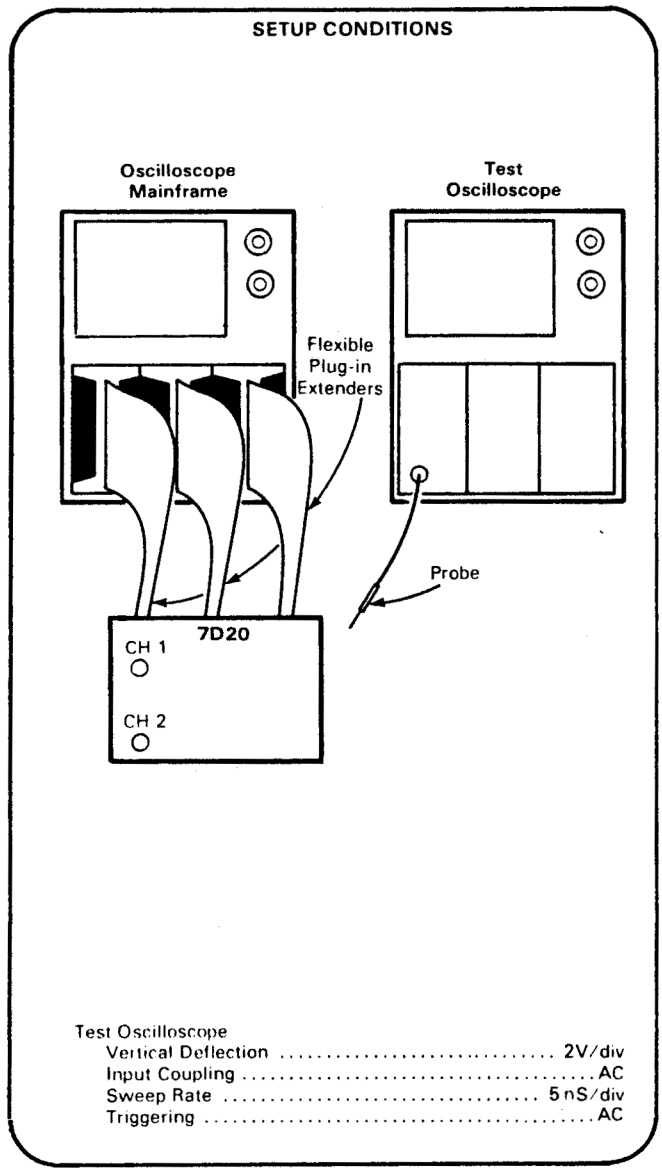
DESCRIPTION



b. Set 7D20 Power to OFF. Remove the upper circuit board supports from the 7D20. Remove the A5 CCD Circuit Board Assembly from the 7D20 and install the 067-1051-00 Circuit Board Extender in its place. Plug A5 into the extender and set 7D20 Power to ON.

c. Position the test oscilloscope trace to the third graticule line below graticule center.

d. Connect the test-oscilloscope probe ground to the A5 CCD circuit board ground.

e. Connect the test oscilloscope probe to pin 5 of U440 on A5.

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DESCRIPTION

f. **EXAMINE** – the test oscilloscope for a pulse width of 5.5 nS to 6.5 nS at graticule center.

g. **ADJUST** – C850 on A5 for a pulse width of 5.5 nS to 6.5 nS at graticule center on the test oscilloscope.

h. Move the test oscilloscope probe to pin 11 of U440.

i. **EXAMINE** – the test oscilloscope for a pulse width of 5.5 nS to 6.5 nS and equal to the measurement at pin 5.

j. **ADJUST** – C851 on A5 for the same pulse width as that measured at pin 5.

k. Repeat steps e, f, and g to correct any change due to adjustment interaction.

NOTE

The pulse-width measurements at pins 5 and 11 of U440 must match each other, so any adjustment interaction must be compensated for.

l. Set 7D20 Power to OFF. Remove the A5 CCD Circuit Board Assembly from the 067-1051-00 Circuit Board Extender and remove the extender from the 7D20. Install A5 in the 7D20 and re-attach the upper circuit board supports. Set the 7D20 Power to ON.

Add the following note at the **beginning of step A9**.

NOTE

If difficulty is experienced making the following ERD adjustments, ***ADJUST INPUT SAMPLING CLOCK (C850, C851)*** *should be repeated. The pulse-width measurements at pins 5 and 11 of U440 can be adjusted by C850 and C851 for any pulse width between 5.5 nS and 6.5 nS that will enable proper ERD adjustment. It must be remembered, however, that the pulse-width measurements at pin 5 and pin 11 are to match one another.*

DIAGRAM CHANGES

6 CCD Drivers

Change C850 and C851 from fixed 33 pF capacitors to variable 7 - 45 pF capacitors (schematic location D2).

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